TEGRATED CIRCUITS

Semiconductors for Wireless Communications

Data Handbook IC17
1999
Part 1

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Semiconductors for Wireless Communications

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PREFACE

Semiconductors for Wireless Communications

Welcome to the latest edition of our Data Handbook/CD-ROM "Semiconductors for Wireless Communications". Wireless communications is one of the fastest growing market segments in the electronics business today. And no one has more to offer in this area than Philips Semiconductors. We supply semiconductor components for everything from cordless, cellular and paging products to exciting new applications, like wireless LAN, Personal Communications Systems (PCS), Global Positioning System (GPS), audio products, industrial control, security systems, and more.

What better place to start, therefore, with your search of wireless communication devices than with this Data Handbook/CD-ROM, where you'll find IC selection charts, wireless system solutions and all our current wireless semiconductor data sheets.

For more information on how we can help with your wireless designs, contact your local sales representative. See the addresses of our local sales organisations at the back of the data handbook, on the CD-ROM or on our Internet site at http://www.semiconductors.philips.com

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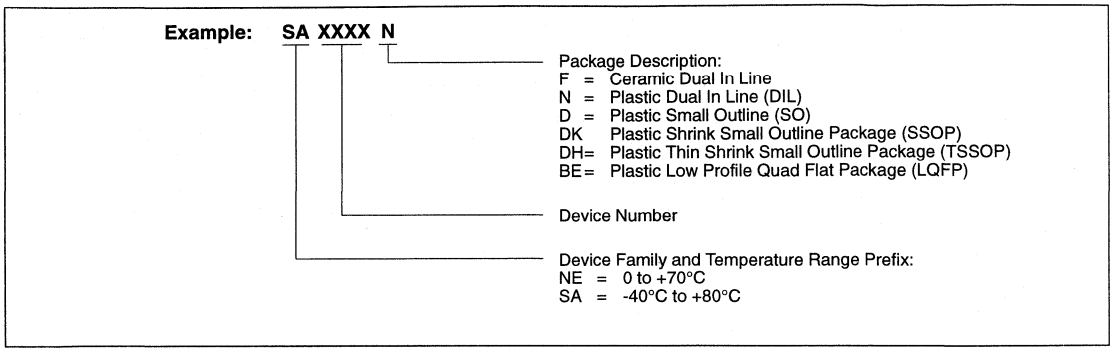
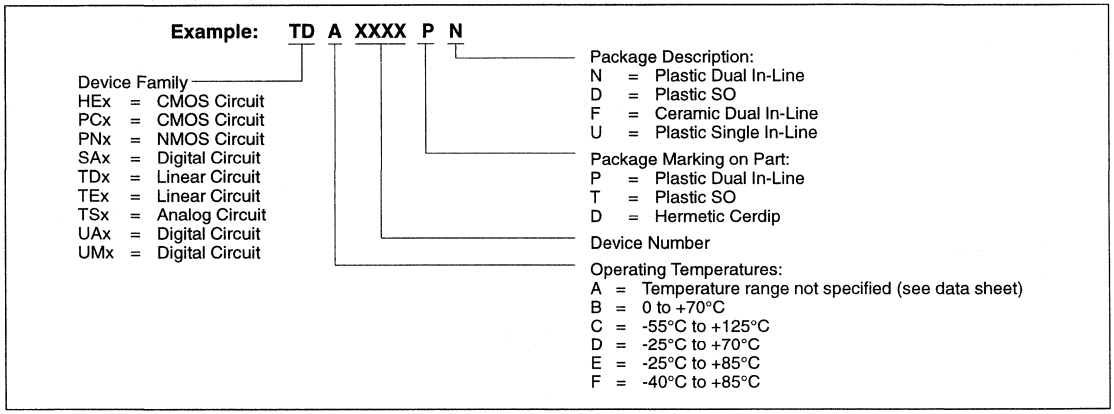
COMMUNICATION PRODUCT GROUP RF PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



INTEGRATED FRONT-END SYSTEMS/MIXERS/AMPLIFIERS

TYPE	DESCRIPTION	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg	INPUT FREQUENCY (GHz)
Image Reject Front-End Systems						
SA1920	dual-band 800/1900 MHz LNA + IRM + IFamp.	3.6 - 3.9	HB Rx: 41.1 HB Tx: 21.3 at 3.75 V	48	BE	0.869 - 0.96 or 1.93 - 1.99
SA1921	dual-band 800/1550 MHz LNA + IRM +IFamp.	3.6 - 3.9	HB Rx: 38.6 HB Tx: 18.8 at 3.75 V	48	BE	0.869 - 0.960 or 1.515 - 1.600
SA3600	low & high-band LNAs + mixers	2.7 - 4.0	LB:15 at 3 V HB: 20 at 3 V	24	DH	LB LNA: 0.8 - 1.0 HB LNA: 1.9 - 2.0
						LB mixer: 0.8 - 1.0 HB mixer: 1.9 - 2.0
UAA2067G	LNA + IRM + mod. + VCO	3 - 3.5	Rx: 24 at 3.6 V Tx: 42 at 3.6 V	32	BE	1.8 - 1.9
UAA2068G	TX + synthe + integrated RFVCO for DECT	3 - 5.2	Rx: 35 at 3.6 V Tx: 55 at 3.6 V	32	BE	output: 1.88 - 1.92
UAA2077AM	LNA + IRM	3.15 - 5.3	27 at 4 V	20	DK	1.8 - 1.9
UAA2077BM	LNA + IRM + Tx down-convert mixer	3.6 - 5.3	Rx: 27 at 4 V Tx: 14 at 4 V	20	DK	1.8 - 2
UAA2077CM	LNA + IRM + Tx down-convert mixer	3.6 - 5.4	Rx: 36 at 3.75 V Tx: 14 at 3.75 V	20	DK	1.8 - 2
Image-Reject Front-End Systems						
UAA2073M	LNA + IRM + Tx down-convert mixer	3.6 - 5.3	Rx: 26 at 3.75 V Tx: 12 at 3.75 V	20	DK	0.925 - 0.960
UAA2073AM	LNA + IRM + Tx down-convert mixer	3.6 - 5.3	Rx: 26 at 3.75 V Tx: 12 at 3.75 V	20	DK	0.925 - 0.960
Integrated Front-End Systems						
SA611	LNA + mixer	2.7 - 5.5	8.3/5.2[1] at 3 V	20	DK	LNA 1.2
						mixer 1.2
SA621	LNA + mixer + VCO	2.7 - 5.5	13.3/10[1] at 3 V	20	DK	LNA 1.2
						mixer 1.2
SA631	LNA + mixer	2.7 - 5.5	8.3/5.2[1] at 3 V	20	DK	LNA 1.2
						mixer 1.2

GAIN POWER (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1 dB COMP. (dBm)	IMAGE REJECTION (dB)	INPUT IMPED. (Ω)	OUTPUT IMPED. (Ω)	FEATURES
f_{RF} = 2 GHz							
22	LB: 2.6 HB: 4.1	LB: 9 HB: 12	24 - 25	35	50	50	dual-band 800 MHz & 1.9 GHz; triple-mode AMPS/DAMPS/PCS
22	LB: 2.6 HB: 3.9	LB:9 HB:13	24 - 25	35	50	50	dual-band 900 MHz & 1.5 GHz
30	5.8	–25	–33	34	190 0.8 pF diff.	50 asym.	RF to IF DECT transceiver (DSH)
20	4.3	–17	–22	32	60 1 pF diff.	1 k diff.	3.15 V, 4.3 dB DECT front-end (DSH)
20	4.3 DCS	–17	–23	32	60 1 pF diff.	1 k diff.	DCS1800 front-end
22	3.8 DCS 4.0 PCS	–17	–24	38	60 0.8 pF diff.	1 k diff.	PCS1900/DCS1800 front-end
f_{RF} = 900 MHz							
23	3.25	–15	–23	37	150 1 pF diff.	1 k diff.	3.6 V phase 2 GSM receiver
22	3.6	–15	–23	45	150 1 pF diff.	1 k diff.	GSM high IF
f_{RF} = 900 MHz							
15/–28[1]	1.7	–7	–20		50	50	Low-voltage; excellent noise figure; LNA overload mode
8.7	9.5	+7	–14.5		50	high	
15/–28[1]	1.7	–7	–20		50	50	Low-voltage; excellent noise figure; LNA overload mode; low phase-noise; interval VCO
8.7	9.5	+4.5	–10		50	high	
15/–28[1]	1.7	–7	–20		50	50	Low voltage; excellent noise figure; LNA overload mode; excellent gain stability
9.6	9.5	+3.3	–14.5		50	high	
17/–15[1] 16/–15[1]	1.7 2.2	–7 –6	–17 –15		50	50	Low voltage; excellent noise figure; LNA overload mode; low current; excellent gain stability
10 9.5	10 8.5	+6 +4	–4 –6		50	high	

TYPE NUMBER	DESCRIPTION	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg[2]	INPUT FREQUENCY (GHz)
Mixer Systems						
SA9500	dual-band; CDMA/AMPS down-converters	2.7 - 3.3	PCS: 20; CDMA: 20; FM: 7.7	20	DH	HB: 1.99 LB: 0.894
SA9502	dual-band; CDMA/AMPS down-convertor	2.7 - 4.0	PCS: 15 CDMA: 18; FM: 6	20	DH	HB: 1.99 LB: 0.894
SA602A	mixer + oscillator	4.5 - 8.0	2.4 at 6 V	8	D	0.500
SA612A	mixer + oscillator	4.5 - 8.0	2.4 at 6 V	8	D	0.500
RF Amplifiers						
SA5200	dual gain stage	4.0 - 9.0	4.2/95 μA[1] at 5 V (per amplif.)	8	D	DC - 1.2
SA5204A	wideband amp	5.0 - 8.0	25 at 6 V	8	D	DC - 0.350
SA5205A	wideband amp	5.0 - 8.0	25 at 6 V	8	D	DC - 0.550
SA5209	variable gain amp	4.5 - 7.0	43 at 5 V	16	D	DC - 0.850
SA5219	variable gain amp	4.5 - 7.0	43 at 5 V	16	D	DC - 0.700

GAIN POWER (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1dB COMP. (dBm)	INPUT IMPED. (Ω)	OUTPUT IMPED. (Ω)	FEATURES
Mixer (f_{RF} = 45 MHz)						
11 7(FM)	9 9	LB: 6 HB: 1		should be matched to 50	open collector 1 k	Ideal mixer for dual-band triple-mode phones LO PCS freq.doubler
11 7(FM)	9 9	LB: 6 HB: 1		should be matched to 50	open collector 1 k	Ideal mixer for dual-band triple-mode phones Direct PCS LO in
17	5.0	–13	–25	1.5 k	1.5 k	Excellent noise figure; high gain
17	5.0	–13	–25	1.5 k	1.5 k	Excellent noise figure; high gain
RF (F_{RG} = 900 MHz for SA5200, 100 MHz for others)						
7.5/13.5(1) (per amplif.)	3.6	–1.8	+3.2	50	50	DC to 1.2 GHz; power-down mode
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4	50	50	DC to 350 MHz
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4	50	50	DC to 550 MHz
25 (voltage)	9.3	+13 (output)	–3	1.2	60	DC to 850 MHz; gain control pin
25 (voltage)	9.3	+13 (output)	–3	1.2	60	DC to 700 MHz; gain control pin

Notes

1. Amplifier: Enabled/Disabled.
2. Package Descriptions:
   D: = Small Outline (SO14/16/20)
   DK: = Shrink Small Outline Package (SSOP)
   BE: = Low Quad Flat Package (LQFP)
   DH: = Thin Shrink Small Outline Package (TSSOP).
3. Abbreviations:
   IRM: Image Reject Mixer
   LNA: Low Noise Amplifier
   DSH: Double Superheterodyne
   ZIF: zero IF
   diff: differential
   asym: asymmetrical.
4. Temperature range:
   SA types: –40 to +85 °C.

DISCRETE FRONT-END SYSTEMS/MIXERS/AMPLIFIERS

SOCKET	SYSTEM FREQ. (MHz)	I_C (mA)	V_{CE} (V)	F_T (GHz)	GAIN (dB) AT 900 MHz(dB)	NOISE AT 900 MHz (dB)	GAIN (dB) AT 1.9 GHz (dB)	NOISE AT 1.9 GHz (dB)	PACKAGE				
									SOT23	SOT323	SOT343[1]	SOT353	SOT363
LNA	900	3	4,5	17	20	1	22	1.6			BFG403W		
	900 & 1900	2 - 5	3 - 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 - 30	3 - 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 - 10	2 - 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 - 25	2 - 4.5	22	20	1.2	28	0.8			BFG425W		
	900; 1900 & 2400	250	4.5	21		1.2		1.8			BFG480W		
PA	900 & 1800	200	4.5	18			10				BFG21W		
Mixer	900	5 - 30	3 - 10	6	13	1.9			BFR93A	BFR93AW	BFG93AW		
	900 & 1900	2 - 5	3 - 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFE505	BFM505
	900 & 1900	3 - 30	3 - 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFE520	BFM520
	900 & 1900	1 - 10	2 - 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 - 25	2 - 4.5	22	20	1.2	28	0.8			BFG425W		
Buffer & VCO	900	3 - 20	3 - 10	6	14	2.1			BFR92A	BFR92AW			
	900	5 - 30	3 - 10	6	13	1.9			BFR93A	BFR93AW			
	900 & 1900	2 - 5	3 - 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 - 30	3 - 12	8	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 - 10	2 - 4.5	22	21	0.9	29	1.2			BFG410W		
	900 & 1900	3 - 25	2 - 4.5	22	20	0.8	28	1.2			BFG425W		
IF	40 - 100	3 - 20	3 - 12	1.2	20 dB gain at 100 MHz				BF547	BF547W			
	100 - 250	3 - 20	3 - 8	2.8	25 dB gain at 250 MHz				BFS17A	BFS17W			
	>250	3 - 20	3 - 10	5	25 dB gain at 500 MHz				BFR92A	BFR92AW			

Note

1. Typically the gain is 2 - 3 dB higher in SOT343 packages.

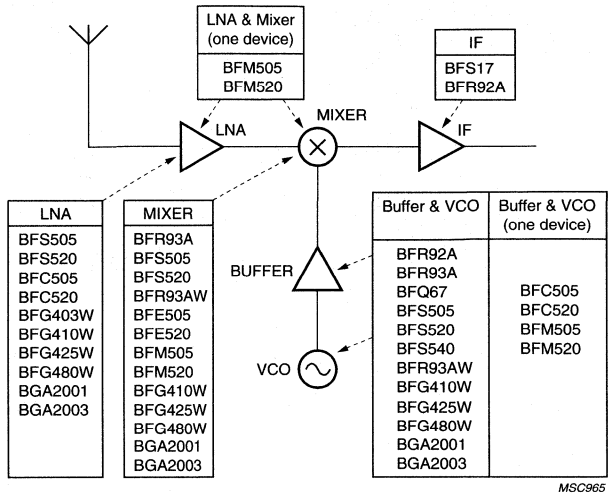


Fig.1 Wireless receiver solutions.

PIN DIODES

TYPE	MAXIMUM RATINGS		CHARACTERISTICS						PACKAGE	CONFIG
	Vr (V)	I_f (mA)	R_d I_f = 0.5 mA f = 100 MHz (Ω)	R_d I_f = 10 mA f = 100 MHz (Ω)	C_d V_r = 0 V f = 1 MHz (pF)	C_d V_r = 5 V f = 1 MHz (pF)	C_d V_r = 20 V f = 1 MHz (pF)	I I_f = 10 mA I_r = 6 mA (μs)		
BAP50-03	50	50	25	3	0.45	0.3	0.25	1.04	SOD323	single
BAP50-04	50	50	25	3	0.45	0.3	0.25	1.04	SOT23	series
BAP50-05	50	50	25	3	0.45	0.3	0.25	1.04	SOT23	common cathode
BAP51-03	60	60	5.5	1.5	0.40	0.2	0.16	0.55	SOD323	single
BAP64-02	200	100	20	2	0.52	0.27	0.23	1.55	SOD523	single
BAP64-03	200	100	20	2	0.52	0.27	0.23	1.55	SOD323	single
BAP64-04	200	100	20	2	0.52	0.27	0.23	1.55	SOT23	series
BAP64-05	200	100	20	2	0.52	0.27	0.23	1.55	SOT23	common cathode

FRONT-END MMICs

TYPE	REMARKS	V_S (V)	I_S (mA)	NF (dB)	GAIN (dB)	IP3 (dBm)	@ (GHz)	P_1 (dB)	ENABLE[1]	PACKAGE
BGA2001	amp	2.5	4	1.5	19[2]		2	-		SOT 343R
BGA2003	amp	2.5	10	1.9	19[2]	+5	2	-	x	SOT 343R
BGA2022[3]	mixer (30 dB LO-RF isolation)	3	7	9	5[4]	+5	0.8 to 1.9	-		SOT363
BGA2031	variable-gain (55 dB) amp	3	50	-	25[5]	–48[6]	1.9	12.5	x + control	SOT551

Notes

1. On/off switch.
2. MSG.
3. Preliminary specification.
4. GC.
5. GP.
6. ACRP or DBc.

IF SYSTEMS

TYPE	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg	INPUT FREQ. (GHz)	IF FREQ. (MHz)	f_{RF} = 45 MHz		
							INPUT SENSITIVITY (μV)	MIXER GAIN (dB)	INPUT IP_3 (dBm)
FM IF									
SA604A	4.5 - 8	3.3 mA at 6 V	16	D	25	25	0.22(1)	–	–
SA614A	4.5 - 8	3.3 mA at 6 V	16	D	25	25	0.22(1)	–	–
SA624	4.5 - 8	3.4 mA at 6 V	16	D	25	25	0.22(1)	–	–
Mixer/FM IF									
SA605	4.5 - 8	5.7 mA at 6 V	20	D,DK	500	25	0.22	13	–10
SA615	4.5 - 8	5.7 mA at 6 V	20	D,DK	500	25	0.22	13	–10
SA625	4.5 - 8	5.8 mA at 6 V	20	D,DK	500	25	0.22	13	–10
Low-voltage mixer/FM IF									
SA606	2.7 - 7	3.5 mA at 3 V	20	D,DK	150	2	0.31	17	–9
SA616	2.7 - 7	3.5 mA at 3 V	20	D,DK	150	2	0.31	17	–9
SA676	2.7 - 5.5	3.5 mA at 3 V	20	D,DK	100	2	0.45	17	–10
SA608	2.7 - 7	3.5 mA at 3 V	20	D,DK	150	2	0.31	17	–9
SA626	2.7 - 5.5	6.5 mA at 3 V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA636	2.7 - 5.5	6.5 mA at 3 V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA639	2.7 - 5.5	8.5 mA at 3 V	24	DH	500	25	2.24(3)	12(3)	–12.5(4)
Low Voltage mixer/Digital IF									
SA647	2.7 - 5.5	5.9 at 3 V	20	DK	200	2	–112 dBm	–	–28
SA1630	2.7 - 5.5	Tx: 26.5; Rx: 33.5 at 3 V	48	BE	400	–	–	–	–
SA1638	2.7 - 5.5	Tx: 22; Rx: 18 at 3 V	48	BE	400	–	–	–	–

RSSI RANGE (dB)	FAST RSSI	FREQ. CHECK PIN	IF FILTER MATCH (kHz)	OUTPUT OP AMPS	FEATURES
FM IF					
90	–	–	455	–	High Sensitivity
80	–	–	455	–	Wide IF BW
90	x	–	455	–	
Mixer/FM IF					
90	–	–	455	–	High Sensitivity
80	–	–	455	–	High Input Frequency
90	x	–	455	–	
Low-voltage mixer/FM IF					
90	–	–	455	Audio op amp RSSI op amp	High Sensitivity
80	–	–	455	Audio op amp RSSI op amp	Low Power
70	–	–	455	Audio op amp RSSI op amp	Audio op amp RSSI buffered
90	–	x	455	Audio Buffered RSSI op amp	Power-down mode (SA626/636/639)
90	x	–	10700	Audio Buffered RSSI op amp	
90	x	–	10700	RSSI op amp	
90	x	–	10700	Audio buffered RSSI op amp Post-detect amp Data switch	
Low Voltage mixer/Digital IF					
90	x	–	455	RSSI op amp	
90	x	–	455	RSSI op amp	
–	–	–	–	–	Wireless LAN using DSSS modulation; digital IF gain control of 70 dB in steps of 2 dB
–	–	–	–	–	GSM 900 MHz, DCS 1.8 GHz, quadrature up & down mixer stage

Notes

1. Measured with a Philips MESA602A mixer prior to the IF input.
2. Measured at f_{RF} = 240 MHz.
3. Measured at f_{RF} = 110 MHz.
4. Represents the –3 dB input limiting point (dBm), Also shown in μV units into a 50 Ω matching network.

Temperature range

SA types: –40 to +85 °C.

Package description

D: small outline.
DK: shrink small outline package (SSOP).
BE: low quad flat package (LQFP).

IF filter match

455 kHz = 1.5k Ω.
10.7 MHz = 330 Ω.

SYNTHESIZERS/PRESCALERS

TYPE	V_{CC} (V)	I_{CC} (mA)	PINS	PACKAGE	MAX RF/INPUT FREQ.	CHANNEL SPACING (GHz)	FRACTIONAL-N DIVIDER (kHz)	AUXILIARY SYNTHE-SIZER	APPLICATIONS
Fractional-N frequency synthesizers									
SA7016DH (new)	2.7 - 5.5	6.2 at 3 V	16	TSSOP16	1.3	–	x	–	IS-54/-136, IS-95, PDC, GSM digital cellular
SA7025DK	2.7 - 5.5	7.5 at 3 V	20	SSOP20	1.0 (main) 0.150 (aux)	–	x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA7026DH (new)	2.7 - 5.5	7.5 at 3 V	20	TSSOP20	1.3 (main) 0.550 (aux)	–	x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA8016DH (new)	2.7 - 5.5	8 at 3 V	16	TSSOP16	2.5	–	x	–	ISM-band, IS-54/-136, IS-95, PDC, GSM digital cellular
SA8025ADK	2.7 - 5.5	11 at 3 V	20	SSOP20	1.8 (main) 0.150 (aux)	–	x	x	PHS digital cordless, US PCS, PDC digital cellular
SA8026DH (new)	2.7 - 5.5	10 at 3 V	20	TSSOP20	2.5 (main) 0.550 (aux)	–	x	x	ISM-band, IS-54/-136, IS-95, PDC, GSM digital cellular
Frequency synthesizers									
UMA1015AM	2.7 - 5.5	at 3 V	20	SSOP20	1.1	5 - 1000	–	x (dual)	AMPS, CT1, CT2, TACS
UMA1021M	2.7 - 5.5	at 5.5 V	20	SSOP20	2.200	10 - 2000	–	–	GSM, DCS, PCS, DECT, PHS, WLL, WLAN
UMA1021AM	2.7 - 5.5	at 5.5 V	16	SSOP16	2.200	10 - 2000	–	–	GSM, DCS, PCS, DECT, PHS, WLL, WLAN
UMA1022M	2.7 - 5.5	at 5.5 V	20	SSOP20	2.100 (main) 0.550 (aux)	10 - 2000	–	x	GSM, DCS, DECT, PHS, WLL, WLAN
Prescalers									
	V_{CC} (V)	**I_{CC} (mA)**	**Pins**	**Package**	**Max input frequency**	**Max. compare freq. (kHz)**	**Input sensitivity (dBm)**	**Divide ratio**	
SA701D	2.7 - 6	4.5 at 3 V	8	SO8	1.1	65/270	–35	128/129, 64/65	
SA702D	2.7 - 6	4.5 at 3 V	8	SO8	1.1	1000	–35	64/66/72	

TRANSMITTER ICs

TYPE	FREQUENCY RANGE: OUTPUT (MHz)	FREQUENCY RANGE: SYNTHESIZER (MHz)	SUPPLY VOLTAGE (V)	I_{CC} AT FULL POWER (mA)	DIFFERENTIAL OUTPUT (dBm)	TRANSMIT OFFSET FREQ. (MHz)	PACKAGE	FEATURES
Cellular								
SA900	820 - 860 (AMPS) 820 - 920 (cellular)	N/A	4.5 - 5.1	42 (AMPS) 68 (dual)	2	90 - 140	LQFP48	I/Q transmit RF modulator with on-chip crystal osc. and VCO
SA9025	824 - 849 (cellular) 1840 - 1920 (PCS) with ext. up-conv.	500 - 2500	3.6 - 3.9	115 (analog) 125 (digital)	10	90 - 180	LQFP48	Highly integrated I/Q transmit RF-modulator with 2.5 GHz dual synth. for 800 & 1900 triple-mode TDMA

MMICS AMPLIFIERS

TYPE NUMBER	FREQUENCY BAND (GHz)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	OUTPUT POWER (dBm)	MIN. POWER GAIN (dB)	EFFICIENCY (%)	PACKAGE	FEATURES
Cellular								
CGY2021G	1.71 - 1.785 1.85 - 1.91	4.8	3.2	34	34	55	LQFP48	GaAs MMIC, 2W DCS/PCS power amplifier
CGY2013	0.880 - 0.915	3.6	3.5	34.5	34	50	LQFP48	GaAs MMIC, GSM 4W power amplifier
SA910	0.820 - 0.905	2.7 - 5.5	0.5	24	32	35	SSOP20	BiCMOS low-voltage, 900 MHz variable gain pre-amplifier
Cordless								
CGY2030M	1.88 - 1.90	3.6	0.5	27	27	40	SSOP16	GaAs MMIC 500 mW amplifier
CGY2032TS	1.88 - 1.90	3.6	0.5	27	27	50	SSOP16	GaAs MMIC 500 mW amplifier
WLAN (ISM band)								
SA2410	2.4 - 2.5	3.0 - 5.5		18.5	29	25	TQFP32	2.5 GHz power amplifier and T/R switch for WLAN (ISM-band)

POWER AMPLIFIER MODULES

TYPE NUMBER	FREQUENCY BAND (MHz)	SUPPLY VOLTAGE (V)	MIN. LOAD POWER (W)	DRIVE POWER (mW)	MIN. POWER GAIN (dB)	EFFICIENCY MIN./TYP. (%)	PACKAGE	PACKAGE THICKNESS (mm)
Digital cellular-GSM								
BGY241	880 - 915	3.5	3	1	35	45 (min.)	SOT482B	2
Digital cellular-DCS								
BGY212A[1]	1710 - 1785	3.5	2.4 (typ.)	10	33	45 (min.)	SOT482B	1.6
BGY212B[2]	1850 - 1910	3.5	2.4 (typ.)	10	33	45 (min.)	SOT482B	1.6
Dual band digital cellular (GSM900/DCS1800)								
BGY280[2]	880 - 915	3.5	4	10	35.5	50	SOT559	1.6
	1710 - 1785	3.5	3	10	33	45	SOT559	1.6

Notes

1. Preliminary specification.
2. Objective specification.

POWER TRANSISTORS

TYPE NUMBER	FREQUENCY (GHz)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	MIN. POWER GAIN (dB)	EFFICIENCY MIN./TYP. (%)	THERMAL RESISTANCE (K/W)[1]	PACKAGE
Analog cellular							
BLT80	900	7.5	0.8	6	60/67	22[2]	SOT223
BLT81	900	7.5 6.0	1.2	6 6.5 (typ.)	60/70 70	32[3]	SOT223
BLT70	900	4.8	0.6	6	60	55[4]	SOT223
BLT71	900	4.8	1.2	6	60	24[5]	SOT223
BLT71/8	900	4.8	1.2	11	55/63	40[6]	SOT96
Digital cellular/cordless							
BFG21W	1900	3.6	0.4	11	50		SOT343
BFG540W	900	6	18 dBm	18			SOT343
BFG540W	1900	3.6	14 dBm	11			SOT343
BFG10W/x	900	6	28 dBm	10			SOT343
BFG10W/x	1900	3.6	20 dBm	6			SOT343
BFG11W/x	1900	3.6	26 dBm	6			SOT343

Recommended line-ups

Application	Supply voltage (V)	Load power (W)	1st stage	2nd stage	3rd stage
Analog	6.0	1.2	BFG540W/x	BLT80	BLT81
	4.8	1.2	BFG540W/x	BLT70	BLT71
	4.8	1.2	BFG10W/x	BLT71/8	
DECT, PHS	3.6	0.4	BFG540/x BFG540W/x BFG425W	BFG10/x BFG10W/x BFG21W	BFG11/x BFG11W/x

Notes

1. Junction to soldering joint.
2. P_{tot} = 2W, Ts = 131 °C.
3. P_{tot} = 2W, Ts = 60 °C.
4. P_{tot} = 2.1W, Ts = 60 °C.
5. P_{tot} = 3.5W, Ts = 90 °C.
6. P_{tot} = 2.9W, Ts = 60 °C.

BASEBAND PROCESSORS

TYPE	PART TYPE	APPLICATION	V_{DD} (V)	I_{DD} (mA)	PACKAGE
PCF50731	baseband & audio interface	GSM/DCS/PCS	1.5 - 3.0	--	LQFP64
P90CL301	16-bit low voltage microcontroller	digital cellular	2.7 - 3.6	--	LQFP80
PCF5077	power amplifier controller	digital cellular	2.7 - 5.5	--	SSOP16
PCF5078	power amplifier controller	digital cellular	2.4 - 5.5	--	TSSOP8
SFZ2003	baseband processor with PMU	AMPS	2.7 - 3.3	10 typ. 0.7 (down mode)	LQFP128
SFZ2002	8-bit low-voltage microcontroller	AMPS	2.7 - 3.3	0.22mA/MHz active; 83 µA/MHz idle	LQFP80
PCD509XY	baseband processor, ABC-pro	DECT, ISDN	1.8 - 3.6	--	LQFP80
PCD5096	universal codec	DECT, ISDN	2.7 - 3.6	--	QFP44
P8XCL883/4/6/7	TELX microcontroller	CT0/900 MHz	2.7 - 3.6	--	SO28
PCF5001	POCSAG decoder	Paging	1.5 - 6.0	60 µA typ.	SO28L, LQFP32
PCD5002A	APOC1/POCSAG decoder	Paging	1.5 - 6.0	25 µA typ. (OFF); 50 µA typ. (ON)	LQFP32
PCD5003A	advanced POCSAG paging decoder	Paging	1.5 - 6.0	25 µA typ. (OFF); 50 µA typ. (ON)	LQFP32
PCA5007	pager baseband controller for all signal standards	Paging	0.9 - 1.6	50 µA typ. (stby); 200 µA typ. (operating)	LQFP48
PCD5008	FLEX decoder	Paging	1.8 - 3.3	6.8 µA typ.	LQFP32
PCD5013	FLEX decoder with roaming capability	Paging	1.8 - 3.3	6.5 µA typ.	LQFP32
PCA5010	pager baseband controller for all signal standards	Paging	0.9 - 1.6	50 µA typ. (stby); 200 µA typ. (operating)	LQFP48

CALLER IDENTIFICATION

TYPE	DTMF-STANDARD	FSK-STANDARD	OPERATING VOLTAGE (V)	SPECIAL FEATURES	PACKAGE	MAX. SPEED (MHz)	CATEGORY
PCD3316	no	yes	2.5 - 3.6	Caller-ID decoder (level 2)	SO16L	3.58	CIDCW
PCD6002	see Table "DSP-based solutions for cordless"						

DSP-BASED SOLUTIONS FOR CORDLESS

TYPE	DESCRIPTIONS	FEATURES/SPECIFICATIONS	PACKAGE	AM	TAM	MULTI-LINE TAM
Digital telephone answering machine (DTAM) and Universal Codec						
PCD6002	DTAM production IC	80CL51 microcontroller, DSP, dual codecs, 32 kb microcontroller memory, caller-ID, full duplex speakerphone, IOM-2 bus interface	QFP80	x	x	x
PCD5096	Universal Codec	Dual codecs, IOM-2 bus interface. Direct connection to PCD6002.	QFP44	–	–	x

TYPE	DESCRIPTIONS	TYP. V_{LN} AT 15 mA (V)	PARALLEL OPERATION	TYP. I_{CC} (mA)	PD[1]	$G_{V(TX)}$ (dB)	$G_{V(RX)}$ (dB)	LOUD-SPEAKER AMP.	TYP. $\Delta G_{V(AGC)}$ (dB)	PACKAGE	AM	TAM	MULTI-LINE TAM
Programmable speech/transmission circuit													
PCA1070	fully programmable line interface	4.83 (at 12 mA)	x	2.3	x	30 - 51	–25 - 11	–	via software	DIP24, SO24	x	x	x
Line-interface ICs with improved EMC performance													
TEA1097	see Table "Line-interface ICs for cordless base stations"										–	x	x
UBA1707											x	–	–

Note

1. PD = Power Down input; AM = Stand-alone Answering Machine; TAM = Telephone/Answering Machine.

LINE-INTERFACE ICS FOR CORDLESS BASE STATIONS

TYPE	DETAILS	SUPPLY VOLTAGE (V)	LINE-POWERED	CURRENT CONSUMPTION (mA)	PD[1]	LOUD-SPEAKER AMPLIFIER	Rx_{OUT}[2]	HANDS-FREE	CORDED HANDSET	PACKAGE
TEA1097	Speech and loudspeaker amplifier IC with auxiliary I/Os & switches	3.0 to 5.3[3]; 3.0 to 6.0[4]	x	3.5[5]; 5.5[6]	x	x	SEL	–	x	VSO40 QFP44
TEA1099	Speech and hands-free IC with auxiliary I/Os & switches	3.0 to 5.3[3]; 3.0 to 6.0[4]	x	4.0[5]; 6.0[6]	x	x	SEL	x	x	QFP44
UBA1706	Programmable line-interface IC with electronic hook switch	3.0 to 5.5	–	2.2	x	–		–	–	SSOP24
UBA1707	UBA1706 with loudspeaker and microphone amplifiers	3.0 to 5.5	–	2.2	x	x	SEL	–	–	SO28, SSOP28

Notes

1. Power Down input.
2. SEL = Single-Ended load.
3. Line-powered.
4. Mains-powered.
5. In speech mode.
6. In hands-free mode.

FUNCTION	PRODUCT OVERVIEW
LNAs	CGY2105/2106
Switches (synthesizers/gain)	SWT0102
Synthesizers/VCOs	UMA1021, SA8016
IF amplifiers	SA5209
AD/DA converters	TDA8768, TDA9901
Gain-controlled amplifiers	SA5209, TDA9901
Modulators/upconverters	MOD1327
PA drivers	Double Polysilicon MMIC, CGY series
PA controllers	PCF5075
PA transistors/modules	LDMOS BLF, BGY, BLV families
Circulators/isolators	Complete range for cellular and paging

LDMOS POWER TRANSISTORS FOR BASE STATIONS

TYPE	FREQUENCY (MHz)	V_{DS} (V)	PL (PED) (W)	MIN. G_P (dB)	MIN. EFFICIENCY (%)	IMD3 (dBc)
BLF1043	960	26	10	16	35	≤30
BLF1046	960	26	45	13	35	≤28
BLF1047	960	26	70	13	35	≤28
BLF1048	960	26	90	13	35	≤28
BLF2043	2000	26	10	13	30	≤30
BLF2045	2000	26	30	10	30	≤30
BLF2047	2000	26	70	10	30	≤30
BLF2048	2000	26	140	10	30	≤30

RF POWER TRANSISTORS AND AMPLIFIERS FOR BASE STATIONS

TYPE	CLASS AB LOAD POWER V_{CE} = 26 V (W)	CLASS AB POWER GAIN AT GIVEN V_{CE} (dB)	INPUT POWER AT GIVEN V_{CE} (W)	CLASS AB EFFICIENCY (CW) (%)	THERMAL RESISTANCE (j – mb) (K/W)	PACKAGE
900 - 960 MHz bipolar RF power transistors						
BLV904	5	12	0.3	>50	14.6 (j – h)	SOT409
BLV909	9	12	0.6	57	5.85	SOT409
BLV910	10	>11	0.8	>55	5.85	SOT171
BLV920	20	>10	2.0	>55	3.5	SOT171
BLV934	30	>9	3.8	>55	2.57	SOT171
BLV946	40	11	3.2	60	1.894	SOT273
BLV958	75	9.5	8.4	55	1.21	SOT391
BLV950	150	9	18.9	50	0.52	SOT262
1800 - 2000 MHz bipolar RF power transistors						
BLV2042	4	12	0.25	45	14.6 (j – h)	SOT409B
BLV2044	15	8	2.4	45	3.5	SOT437A
BLV2045N	35	9.5	3.9	43	1.4	SOT390A
BLV2046	50	≥7.5	8.9	≥40	0.9	SOT460A
BLV2047	60	≥8.5	8.5	≥40	0.73	SOT468A
BLV2048	120	>8	19.0	>40	0.35	SOT494A

TYPE	LOAD POWER V_S = 26 V (W)	POWER GAIN AT GIVEN V_S (dB)	INPUT POWER AT GIVEN V_S (mW)	EFFICIENCY (CW) (%)	LOAD IMPEDANCE (Ω)	PACKAGE
920 - 960 MHz RF base-station amplifier modulus						
BGY916	16	>28	25	>35	50	SOT365
BGY925	25	>28	50	>35	50	SOT365
1805 - 1881 MHz RF base station amplifier modulus						
BGY1816	16	>24	63	>35	50	SOT365A
BGY1816S	16	>29	20	>35	50	SOT501A
1930 - 1990 MHz RF base-station amplifier modulus						
BGY1916	16	≥24	63	>33	50	SOT365A

I²C-BUS I/O EXPANDERS FOR BASE STATIONS

TYPE	FUNCTION	SUPPLY VOLTAGE (V)	STANDBY CURRENT (μA)	I²C-BUS (kHz)	INTERRUPT	CONFIGURATION	ADDRESS	POWER-ON RESET	PACKAGE
PCF8574	Remote 8 bit I/O expansion via I²C-bus	2.5 - 6.0	10	100	yes	slave	8 devices addressable	internal	DIP16, SO16 or SSOP20
PCF8575	Remote 16 bit I/O expansion via I²C-bus	2.5 - 5.5		400	yes	slave	8 devices addressable	internal	SSOP24
PCF8584	Parallel bus to I²C-bus protocol converter and interface	4.5 - 5.5	2.5	100	yes	master/slave	7-bit address register written in during initialisation	external	DIP20, SO20

GSM/DCS/PCS ICs

TYPE	FUNCTION
UAA2075	single-chip GSM transceiver
UAA3520	single-chip 3 V GSM transceiver
UAA3521	single-chip GSM closed-loop transceiver
UAA3522 & UAA2077	GSM dual band with UAA2077 Tx modulation loop
UAA3525	single-chip DCS/PCS transceiver
TDA8002/03	SIM card interface
TDA8004/05 TDA8006	SIM card interface
UBA8070/71	power management unit (PMU)
UBA8073	PMU with SIM card interface DC/DC converter
UMA1021M	low-voltage frequency synthesizer
BGY240S	power amplifier module
CGY2013	MMIC power amplifier
CGY2021	MMIC power amplifier
UBA1710	modulator for GaAs power amplifier
PCF5078	power amplifier controller for GSM
P90CL301	low-voltage microcontroller
PCF50731	GSM baseband and audio interface
PCF50862	GSM baseband controller
TEA1095	hands-free IC
SA8026/16; SA7026/16	low-voltage 2.5 and 1.3 GHz fractional-N dual and single synthesizers

TDMA RF ICs

TYPE	FUNCTION
SA3600	dual-band RF front-end, low-voltage
SA1920	dual-band RF front-end
SA9025	dual-band RF transmitter/modulator with fractional-N dual synthesizer
SA647	IF digital receiver, low-voltage
SA611/631	low-voltage LNA and mixer - 1 GHz
SA621	low-voltage LNA mixer and VCO
SA8026/16; SA7026/16	low-voltage 2.5 and 1.3 GHz fractional-N dual and single synthesizers
SA900	I/Q transmit modulator
UBA8070/71	power management unit (PMU)

CDMA ICs

TYPE	FUNCTION
SA9500	low-voltage dual-band down converter for CDMA/AMPS
SA9502	low-voltage dual-band down converter for CDMA/AMPS
SA8026/16; SA7026/16	low-voltage 2.5 and 1.3 GHz fractional-N dual and single synthesizers

AMPS/(E)TACS ICs

TYPE	FUNCTION
SA611	low-voltage LNA and mixer - 1 GHz
SA616	low-voltage high-performance mixer FM IF system
SA621	low-voltage LNA mixer and VCO
SA910	pre-driver
UMA1015AM	low-power dual frequency synthesizer
SZF2003	low-voltage baseband processor with PMU and DTMF detection
SZF2002	8-bit low-voltage microcontroller with embedded RAM
UMA1002	low-voltage data processor (DPROC)
TDA7050	audio amplifier

DECT ICs

TYPE	FUNCTION
UAA2067G	low-voltage 2 GHz RF transceiver
UAA2068G	PLL/VCO/doubler/modulator
UAA3540TS	fully integrated DECT receiver
UAA2078	Zero-IF front-end
UAA2079	Zero-IF filter/demodulator
SA639	low-voltage mixer FM IF system with filter amplifier and data switch
UMA1022M	low-voltage frequency synthesizer
CGY2032	low-voltage MMIC power amplifiers
PCD5091/2/3/4	single-chip baseband processor
PCD50912 PCD50917	ABC-Pro handset baseband controller
PCD50922 PCD50927	ABC-Pro base unit baseband controller
PCD50937	ABC-Pro baseband controller for ISDN base units
PCD5096	universal CODEC
TEA1097/99	featurephone ICs (base unit)
UBA1706/07	programmable speech/transmission ICs

TELX MICROCONTROLLERS (80CL51 CORE-BASED, OPTIMIZED FOR TELECOM)

TYPE	ROM (kB)	RAM (B)	EEPROM (B)	I/O	OPERATING VOLTAGE (V)	SPECIAL FEATURES	PACKAGE	MAX.	CATEGORY SPEED (MHz)
P83CL881	63	2048		32	2.7 - 3.6	UART, 400 kbits/s I^2C-bus, low-voltage detection	LQFP44	10[1]	TELX
P87CL881	63 (OTP)	2048		32	2.7 - 3.6	OTP version of P83CL881	LQFP44	10[1]	TELX
P83CL883	8	256		18	2.7 - 3.6	UART, MSK modem, 400 kbits/s I^2C-bus, DTMF, low-voltage det., In-System programming	SO28	3.58[1][2]	TELX
P87CL883	8 (OTP)	256		18	2.7 - 3.6	OTP version of P83CL883	SO28	3.58[1][2]	TELX
P83CL884	8	256	128	18	2.7 - 3.6	Same as P83CL883 but with additional 256 bytes EEPROM	SO28	3.58[1][2]	TELX
P87CL884	8 (OTP)	256	128	18	2.7 - 3.6	OTP version of P83CL884	SO28	3.58[1][2]	TELX
P83CL886	16	512		18	2.7 - 3.6	Same as P83CL883 but larger program memory size	SO28	3.58[1][2]	TELX
P87CL886	16 (OTP)	512		18	2.7 - 3.6	OTP version of P83CL886	SO28	3.58[1][2]	TELX
P83CL887	12	512		18	2.7 - 3.6	Same as P83CL883 but larger program memory size	SO28	3.58[1][2]	TELX
P87CL887	12 (OTP)	512		18	2.7 - 3.6	OTP version of P83CL887	SO28	3.58[1][2]	TELX
PCD6002	32 (OTP)	768		34	2.7 - 3.6	DTAM chip includes µC, DTMF, DSP and MSK modem,	QFP80	3.58	DTAM
PCD3316					2.5 - 3.6	CIDCW receiver	SO16L	3.58 M/ 32 k[3]	CID

Notes

1. TELX core is twice as fast as standard 80C51, i.e. 10 MHz clock corresponds to 20 MHz clock on standard 80C51 with same performance.
2. For DTMF.
3. 2 crystals are required: one for RTC, the other to be shared with the microcontroller for DTMF generation.

CT0 ICs

TYPE	FUNCTION
UAA206x	transceiver
TELX microcontroller	See Chapter "TELX microcontrollers (80CL51 core-based, optimized for telecom)"
PCD3316	See Chapter "Caller identification"
PCD6002	See Chapter "DSP-based solutions for cordless"
TEA1118A	Speech/transmission IC (base unit)
TEA1097/99	Featurephone ICs (base unit)
UBA1706/07	Programmable speech/transmission ICs (base unit)
TDA7052A/AT	1 W low-voltage audio power amp with DC volume control

PAGING ICs

TYPE	FUNCTION
UAA2080	Advanced pager receiver
UAA2082	Advanced pager receiver
PCD5003A	Advanced POCSAG paging decoder
PCD5002A	APOC1/POCSAG decoder
PCF5001	POCSAG paging decoder
P87CL881	Low-voltage microcontroller
PCD5013	FLEX™ decoder
PCA5007	Baseband decoder for all pager standards
PCA5010	Baseband decoder for all pager standards
UAA3500HL[1]	Pager receiver for all bands (130 to 930 MHz)

Note

1. Compatible with high- (FLEX™, ERMES) and low-speed standards; available Q3, 1999.

WLAN ICs

TYPE	FUNCTION
SA2410	GaAs power amplifier with transmit/receive switch
SA2420	2.4 GHz transceiver RF front-end
DSSS	
SA8016	Low-voltage 2.5 GHz fractional-N synthesizer with phase-detector comparison 5 - 8 x channel spacing
UMA1021M	Low-voltage conventional synthesizer with prescalers, programmable dividers and phase comparators
SA1630	70 to 400 MHz IF I/Q transceiver
FDSS	
SA8026	Dual low-voltage 2.5 GHz fractional-N synthesizer with phase-detector comparison 5 - 8 x channel spacing
UMA1022M	Dual low-voltage conventional synthesizer with prescalers, programmable dividers and phase comparators
SA639	Low-voltage mixer FM IF system with filter amplifier

GPS ICs

TYPE	FUNCTION
UAA1570	Low-voltage, double-conversion, spread-spectrum radio receiver
SAA1575	Baseband processor with embedded controller and GPS correlator

DC/DC CONVERTER ICs

TYPE NUMBER	TEA1204T		TEA1205AT		TEA1206T		TEA1207T		TEA1210TS	
	V_{in}	V_{out}	V_{in}	V_{out}	V_{in}	V_{out}	V_{in}	V_{out}	V_{in}	V_{out}
Up conversion (V)	2.0 to 4.3 2.0 to 3.0	5.0 3.3	2.0 to 4.3 2.0 to 3.0	5.5 3.3	1.6 to 5	2.8 to 5.5	1.6 to 5	2.8 to 5.5	1.6 to 5	2.8 to 5.5
Down conversion (V)	3.6 to 5.0 3.3 to 5.0	3.6 3.3	not applicable		2.8 to 5.5	1.25 to 5.5	2.8 to 5.5	1.25 to 5.5	2.8 to 5.5	1.25 to 5.5
Synchronisation (MHz)	not applicable		13		9 to 20		4 to 20		9 to 20	
Max. output power (W): continuous/pulsed	3.25/8		3.25/8		3.25/12		2.75/7		5.75/14	
Switches' resistance (Ω)	0.15		0.15		0.15		0.22		0.055	
Switch frequency (kHz)	200		200		560		275		590	
Quiescent current (μA)	60		60		75		65		75	
Package	SO8		SO8		SO8		SO8		SSOP16	

INTELLIGENT FAST-CHARGE ICs

TYPE NUMBER	TEA1104(T)	TEA1100(T)	TEA1101(T)	TEA1103(T)	TEA1102(T)
Cell type	NiCd, NiMH	NiCd	NiCd, NiMH	NiCd, NiMH	NiCd, NiMH, SLA, Li-Ion
Fast charge termination	–dV: <3 mV/cell	–dV: <3 mV/cell	–dV: <3 mV/cell	–dV: <3 mV/cell, dT/dt	–dV: <3 mV/cell, dT/dt
Currentless sensing	yes	yes	yes	yes	yes
Charge profile	fast charge, pulsating trickle	fast charge, pulsating trickle	fast charge, pulsating trickle	fast, top-off, pulsating trickle	NiCd, NiMH: fast, top-off pulsating trickle SLA, Li-Ion: fast, fill-up
Charge current control	digital drive	analog drive, PWM drive, digital drive	analog drive, PWM drive, digital drive	analog drive, PWM drive, voltage regulation	analog drive, PWM drive, voltage regulation
Poss. fast charge rates	0.2 CA to 5 CA	0.2 CA to 5 CA	0.2 CA to 5 CA	0.2 CA to 5 CA	0.2 CA to 5 CA
Possible trickle charge rates	fast charge/40	CA/10 to CA/100	CA/10 to CA/100	0.15 CA (top-off) 0.03 CA (trickle)	0.15 CA (top-off) 0.03 CA (trickle)
Charge with load	no	no	no	yes	yes
Refresh	external circuitry	external circuitry	external circuitry	integrated (manually activated) regulated discharge current	integrated (manually activated) regulated discharge current
User interface	LEDs	LEDs	LEDs	LEDs, buzzer, supports charge gauge function	LEDs, buzzer, supports charge gauge function
Protection	open/short circuit, time-out, max. temp., min. temp.	open/short circuit, time-out, max. temp., min. temp.	open/short circuit, time-out, max. temp., min. temp.	open/short circuit, time-out, max. temp., min. temp.	open/short circuit, time-out, max. temp., min. temp.
Package options	DIL/SO8	DIL/SO16	DIL/SO16	DIL/SO/SSOP20	DIL/SO/SSOP20

LITHIUM-ION CELL PROTECTION IC

SAA1502A operating range (battery voltage)	3.6 to 4.3 V
Max. charge voltage	17.5 V
Integrated MOS transistors	60 mΩ
Power-down current	0.1 μA
Operating temp. range	−25 to +80 °C
Package	SSOP16
Battery disconnection on: over discharge, over-charge, over-current (charge & discharge), high temperatures	

KEY TRANSISTORS FOR POWER MANAGEMENT

TYPE	$R_{DS(ON)}$ (Ω)	at V_{GS} (V)	V_{DS} (V)	VT (V)	ID (A)	PACKAGE
N-channel PowerMOS - small SMD						
BHS110	0.017	2.5	20	>1.0	tbf	TSSOP8
BHS109	0.04	2.5	20	>1.0	tbf	TSOP6/SC74 (SOT457)
BHS108	0.085	2.5	20	>1.0	tbf	SOT23
BHS107	0.09	2.5	20	>0.4	2.50	TSOP6/SC74 (SOT457)
BHS106	0.25	2.5	20	>0.4	1.43	SOT363/SC88
BHS105	0.25	2.5	20	>0.4	1.21	SOT23
BHS103	0.50	2.5	30	>0.4	0.86	SOT23
BHS102	0.40	10	30	>1.0	0.86	SOT23
BHS101	0.60	10	60	>1.0	0.70	SOT23
2N7002	4.0	10	60	>0.8	0.18	SOT23
N-channel PowerMOS - small SMD, dual channel						
BSH301	0.04	2.5	20	>0.4	5.0	TSSOP8
BSH302	0.2	2.5	20	>0.4	tbf	TSOP6/SC74 (SOT457)
BSH303	4	10	60	>1.0	tbf	TSOP6/SC74 (SOT457)
P-channel PowerMOS - Small SMD						
BSH209	0.04	2.5	12	>0.4	tbf	TSSOP8
BSH207	0.15	2.5	12	>0.4	1.98	TSOP6/SC74 (SOT457)
BSH208	0.175	2.5	12	>0.4	tbf	SOT23
BSH205	0.5	2.5	12	>0.4	0.86	SOT23
BSH206	0.5	2.5	12	>0.4	1.01	SOT363/SC88
BSH203	1.1	2.5	30	>0.4	0.57	SOT23
BSH202	0.9	10	30	>1.0	0.57	SOT23
BSH201	2.5	10	60	>1.0	0.34	SOT23
BSS84	10	10	50	>0.8	0.13	SOT23
P-channel PowerMOS - Small SMD, dual channel						
BSH402	0.5	2.5	12	>0.4	tbf	TSOP6/SC74 (SOT457)
BSH403	0.01	10	50	>0.8	tbf	TSOP6/SC74 (SOT457)

TYPE	$R_{DS(ON)}$ (Ω)	at V_{GS} (V)	V_{DS} (V)	VT (V)	ID (A)	PACKAGE
N-channel PowerMOS - larger SMD						
PHN1011	0.011	10	25	>1.0	11.0	SO8
PHN1013	0.0135	10	30	>1.0	10.0	SO8
PHN1015	0.014	10	25	>1.0	9.0	SO8
PHN1018	0.016	10	25	>1.0	8.7	SO8
PHN103	0.03	10	30	>1.0	8.5	SO8
N-channel PowerMOS - larger SMD, dual channel						
PHN203	0.03	10	25	>1.0	8.28	SO8
PHN205	0.05	10	30	>1.0	6.4	SO8
PHN210	0.1	10	30	>1.0	3.5	SO8
P-channel PowerMos - larger SMD						
PHP1025	0.025	2.5	12	>0.4	tbf	SO8
PHP1035	0.035	10	25	>1.0	8.0	SO8
PHP109	0.09	10	30	>1.0	5.0	SO8
P-channel PowerMOS - larger SMD, dual channel						
PHP222	0.22	2.5	30	>0.4	1.93	SO8
PHP206	0.06	10	25	>1.0	5.6	SO8
PHP212	0.12	10	30	>1.0	4.0	SO8
PHP225	0.25	10	30	>1.0	2.3	SO8
N/P-channel PowerMOS - complementary pairs						
PHC20306	0.03/0.06	10	25	>1.0	8.2	SO8
PHC20512	0.05/0.12	10	30	>1.0	6.4	SO8
PHC21025	0.1/0.25	10	30	>1.0	3.5	SO8
N-channel PowerMOS with Schottky diode						
PHN103S	0.03	10	25	>1.0	6.0	SO8

OVERVIEW OF LCD GRAPHIC AND CHARACTER DRIVERS

TYPE	ROWS	COL	MATRIX SIZE (LINES × CHARS OR MATRIX SIZE)	LOGIC VOLTAGE RANGE (V)	LCD VOLTAGE $V_{OP(MAX)}$ (V)	ON-CHIP BIAS GEN.	ON-CHIP VOLTAGE MULTIPLIER	INTERFACE	TEMP. COMP.	PACKAGES	XTAL/ BUMPS
Character drivers											
PCF2116	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5 - 6.0	9	x	x	I²C-bus and parallel 4/8bit		LQFP128	x/x
PCF2104	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5 - 6.0	9	x		I²C-bus and parallel 4/8bit			x/x
PCF2105	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5 - 6.0	9	x		400 kbits/s I²C-bus and parallel 4/8bit			x/x
PCF2113	18	60	2 lines by 12 + icons or 1 line by 24 + icons	1.8 - 5.5	6.5	x	x	400 kbits/s I²C-bus and parallel 4/8bit	x	LQFP100	x/x
PCF2103	18	60	2 lines by 12 + icons or 1 line by 24 + icons	1.8 - 5.5	6.5	x		400 kbits/s I²C-bus and parallel 4/8bit			x/x
PCF2119 slim chip	9, 18	80	1 line by 32 or 2 lines by 16 + icons	1.5 - 4.0	6.5	x	x	400 kbits/s I²C-bus and parallel 4/8bit	x		-/x
Graphic drivers											
PCF8531(1)	33	128	33 × 128	1.5 - 5.5	9	x	x		x	tray	/x
PCF8548(1)	65	102	65 × 102	1.5 - 5.5	9	x	x		x	tray	/x
PCF8558 slim chip	40	101	40 × 101	2.5 - 6.0	9	x		400 kbits/s I²C-bus			/x
PCF8578	8, 16, 24, 32	32, 24, 16, 8	any	2.5 - 6.0	9			I²C-bus		VSO56, LQFP64	x/x
PCF8579		40	any	2.5 - 6.0	9			I²C-bus		VSO56, LQFP64	x/x
OM6202	65	102	65 × 102	2.5 - 3.3	16	x	x	parallel	x	TCP	/x
PCF8549	65	102	65 × 102	1.5 - 6.0	16	x	x	400 kbits/s; I²C-bus	x	tray	/x
OM6204	65	102	65 × 102	1.5 - 6.0	16	x	x	400 kbits/s; I²C-bus	x	TCP	/x

Note

1. New.

OVERVIEW OF LCD SEGMENT DRIVERS

TYPE	SEGMENTS AT MULTIPLEX RATE						LOGIC VOLTAGE RANGE (V)	LCD VOLTAGE $V_{OP(MAX)}$ (V)	ON-CHIP BIAS VOLTAGE GENERATOR	INTERFACE	SPECIAL FEATURES	PACKAGES	XTAL/BUMPS
	1 : 1	1 : 2	1 : 3	1 : 4	1 : 8	1 : 16							
PCF8566 (OM4085[1])	24	48	72	96			2.5 - 6.0	6.0	x	I²C-bus	cascadable with PCF8566/76(C)	DIL40, VSO40	/x
PCF8576 PCF8576C	40	80	120	160			2.5 - 9.0 2.5 - 6.0	9.0 6.0	x	I²C-bus	cascadable with PCF8566/76(C)	VSO56, LQFP64	x/x
PCF8578					256	384	2.5 - 6.0	9.0		I²C-bus	easy blinking, scratch pad RAM	VSO56, LQFP64	x/x
OM4068	32	64	96				2.5 - 5.5	6.5		2 MHz serial	cascadable	QFP44, DIP40	x/
PCF8533[2] slim chip	80	160	240	320			2.5 - 5.5	6.5	x	400 Kbits/s I²C-bus	cascadable up to 5120		/x

Notes

1. V_{DD} = 2.00 V.
2. New.

OVERVIEW OF REAL-TIME CLOCK ICs

TYPE	I²C	1/100th SEC & SEC TIMING	M:h, D:m	YRS/ LEAP YRS	PROG. ALARM	PROG. TIMER	SUPPLY VOLTAGE I²C-BUS (V)	SUPPLY VOLTAGE CLOCK (V)	TYP. POWER CONSUMPTION (STANDBY)	PACKAGE
PCF8573	x		x		x		2.5 - 6.0	1.1 - 6.0	3 µA at 1.5 V	DIL16, SO16
PCF8583	x	x	x	x	x	x	2.5 - 6.0	1.1 - 6.0	2 µA at 1.0 V	DIL8, SO8L
PCF8593	x	x	x	x	x	x	2.5 - 6.0	1.1 - 6.0	1 µA at 2.0 V	DIL8, SO8L
PCF8563(1)	x		x	x	x	x	1.8 - 5.5	1.0 - 5.5	0.25 µA at 1 V	DIL8, SO8, TSSOP8

Note

1. New - samples available.

TYPE	INTERRUPT OUTPUT	SCRATCHPAD RAM (1 V RET)	POWER FAIL DETECTOR	EVENT COUNTER MODE	POWER-ON RESET (V)	SUPPLY VOLTAGE I²C-BUS (V)	SUPPLY VOLTAGE CLOCK (V)	TYP. POWER CONSUMPTION (STANDBY)	PACKAGE
PCF8573			x		x	2.5 - 6.0	1.1 - 6.0	3 µA at 1.5 V	DIL16, SO16
PCF8583	x	248 bytes		x	x	2.5 - 6.0	1.1 - 6.0	2 µA at 1.0 V	DIL8, SO8L
PCF8593	x			x	ext.	2.5 - 6.0	1.1 - 6.0	1 µA at 2.0 V	DIL8, SO8L
PCF8563(1)	x		x		x	1.8 - 5.5	1.0 - 5.5	0.25 µA at 1 V	DIL8, SO8, TSSOP8

Note

1. New - samples available.

DIODES FOR WIRELESS TELEPHONY

SPECIFICATION	DESCRIP-TION	TYPE RANGE - SORTED BY PACKAGE TYPE									
		SOT23	SOD80	SC59/ SOT346	SC70/ SOT323	SC74/ SOT457	SC75/ SOT416	SC76/ SOD323	SC79/ SOD523	SC88/ SOT490	SC89/ SOT490
Zener diodes											
P_{ZSM} max. 40 W P_{tot} max. 250 - 400 mW	Zener diode	BZX84 PMBZ series	BZV55	PZM-N series				PDZ-B series			
V_z max 5.6 V	ESD protection array					BZA456A					
V_z max. 6.2 V	ESD protection array					BZA462A					

SPECIFICATION	DESCRIP-TION	TYPE RANGE - SORTED BY PACKAGE TYPE									
		SOT23	SOD80	SC59/ SOT346	SC70/ SOT323	SC74/ SOT457	SC75/ SOT416	SC76/ SOD323	SC79/ SOD523	SC88/ SOT490	SC89/ SOT490
V_z max. 6 - 8 V	ESD protection array					BZA408B					
V_z max. 20 V	ESD protection array					BZA420A					
Schottky diodes											
25 V, 1000 mA	medium power					1PS74SB23					
30 V, 200 mA	small signal	BAT54						1PS76SB10	1PS79SB10		1PS89SB14 1PS89SB15 1PS89SB16
40 V, 120 mA	small signal	BAS40					1PS75SB45	1PS76SB40		1PS88SB45	
40 V, 200 mA	small signal	BAT721		1PS59SB21				1PS76SB21			
40 V, 500 mA	small signal	BAT720		1PS59SB20							
40 V, 1000 mA	medium power		PRLL5819								
70 V, 70 mA	small signal	BAS70						1PS76SB70	1PS79SB70		
Switching diodes											
200 - 215 mA, 70 - 80 V	high speed switching	BAS16	BAS32L	1PS193	BAS16W		BAS16T	BAS316	BAS516		
	series connected	BAV99		1PS226	BAV99W BAV199 W1PS302						
	common cathode (BAV756S is CA/CC)	BAV70		1PS184	BAV70W 1PS301		BAV70T			BAV70S BAV756S	
	common anode	BAW56		1PS181	BAW56 1PS300		BAW56T			BAW56S	

LOW-FREQUENCY SMALL-SIGNAL TRANSISTORS FOR WIRELESS TELEPHONY

MAX. V_{CEO} & I_C	POL.	POLARITY TYPE RANGE - SORTED BY PACKAGE TYPE AND POWER (P_{TOT}) RATING									
		SOT23 250 mW	SOT89/ SC-62 1.2 W	SOT143/ SC-61 250 mW	SOT223/ SC-73 1.3 W	SOT323/ SC-70 200 mW	SOT346/ SC-59 250 mW	SOT363/ SC-88 200 mW	SOT416/ SC-75 150 mW	SOT490/ SC-89 250 mW	OTHER FEATURES
Breakthrough in small-signal transistors for extended battery life (very low V_{CEsat})											
10 V, 3 A	npn				BDL31						Very low V_{CEsat} = 180 mV (I_C = 1 A; I_B = 20 mA)
10 V, 3 A	pnp				BDL32						Very low V_{CEsat} = 250 mV (I_C = 1 A; I_B = 20 mA)
40 V, 1 A	npn	PMMT491A									Very low V_{CEsat} < 300 mV (I_C = 500 mA; I_B = 50 mA)
40 V, 1 A	pnp	PMMT591A									Very low V_{CEsat} < 350 mV (I_C = 500 mA; I_B = 50 mA)
40 V, 5 A	npn pnp				PBSS4540Z PBSS5540Z						in development
50 V, 2 A	pnp		PBSS5250X								in development
50 V, 3 A	npn		PBSS4350X								in development
High speed switching transistors											
15 V, 100 mA	npn	PMBT2369			PZT2369A	PMST2369					t_{on}: 10 ns (at 10 mA/3 mA/ −1.5 mA)
40 V, 800 mA	npn	PMBT2222A	PXT2222A		PZT2222A	PMST2222A					t_{on}: 35 ns (at 150 mA/ 15 mA/−15 mA)
60 V, 600 mA	pnp	PMBT2907A	PXT2907A		PZT2907A	PMST2907A					t_{on}: 40 ns (at −150 mA/ −15 mA/15 mA)
Resistor-equipped transistors											
50 V, 100 mA	pnp npn	PDTA123ET PDTC123ET									R1/R2: 2.2 kΩ/2.2 kΩ
50 V, 100 mA	pnp npn	PDTA143ET PDTC143ET				PDTA143EU PDTC143EU	PDTA143EK PDTC143EK		PDTA143EE PDTC143EE		R1/R2: 4.7 kΩ/4.7 kΩ

MAX. V_{CEO} & I_C	POL.	POLARITY TYPE RANGE - SORTED BY PACKAGE TYPE AND POWER (P_{TOT}) RATING									
		SOT23 250 mW	SOT89/ SC-62 1.2 W	SOT143/ SC-61 250 mW	SOT223/ SC-73 1.3 W	SOT323/ SC-70 200 mW	SOT346/ SC-59 250 mW	SOT363/ SC-88 200 mW	SOT416/ SC-75 150 mW	SOT490/ SC-89 250 mW	OTHER FEATURES
50 V, 100 mA	pnp	PDTA114ET				PDTA114EU	PDTA114EK		PDTA114EE	PDTA114EEF[2]	R1/R2: 10 kΩ/10 kΩ
	npnp							PUMD3			
	npn	PDTC114ET				PDTC114EU	PDTC114EK	PUMH11	PDTC114EE	PDTC114EEF[2]	
50 V, 100 mA	pnp	PDTA124ET				PDTA124EU	PDTA124EK		PDTA124EE		R1/R2: 22 kΩ/22 kΩ
	npnp							PUMD2			
	npn	PDTC124ET				PDTC124EU	PDTC124EK	PUMH1	PDTC124EE		
50 V, 100 mA	pnp	PDTA144ET				PDTA144EU	PDTA144EK	PUMB2[2]	PDTA144EE	PDTA144EEF[2]	R1/R2: 47 kΩ/47 kΩ
	npnp							PUMD12			
	npn	PDTC144ET				PDTC144EU	PDTC144EK	PUMH6[2]	PDTC144EE	PDTC144EEF[2]	
50 V, 100 mA	pnp	PDTA123JT							PDTA123JE	PDTA123JEF[2]	R1/R2: 2.2 kΩ/47 kΩ
	npnp							PUMD10			
	npn	PDTC123JT							PDTC123JE	PDTC123JEF[2]	
50 V, 100 mA	pnp										R1/R2: 4.7 kΩ/open
	npnp							PUMD6			
	npn	PDTC143TT						PUMH7			
50 V, 100 mA	pnp	PDTA143XT							PDTA143XE		R1/R2: 4.7 kΩ/10 kΩ
	npn	PDTC143XT							PDTC143XE		
50 V, 100 mA	pnp	PDTA143ZT					PDTA143ZK				R1/R2: 4.7 kΩ/47 kΩ
	npn	PDTC143ZT					PDTC143ZK				
50 V, 100 mA	pnp	PDTA114TT				PDTA114TU	PDTA114TK	PUMB4			R1/R2: 10 kΩ/open
	npn	PDTC114TT				PDTC114TU	PDTA114TK	PUMH4	PDTC114TE		
50 V, 100 mA	pnp	PDTA114YT				PDTC114YU			PDTC114YE		R1/R2: 10 kΩ/47 kΩ
	npnp							PUMD9			
	npn	PDTC114YT						PUMH9[2]			
50 V, 100 mA	pnp								PDTA124XE	PDTA124XEF[2]	R1/R2: 22 kΩ/47 kΩ
	npn								PDTC124XE	PDTC124XEF[2]	
50 V, 100 mA	pnp					PDTA144WU					R1/R2: 47 kΩ/22 kΩ
	npn	PDTC114WT				PDTC144WU					

MAX. V_{CEO} & I_C	POL.	POLARITY TYPE RANGE - SORTED BY PACKAGE TYPE AND POWER (P_{TOT}) RATING									
		SOT23 250 mW	SOT89/ SC-62 1.2 W	SOT143/ SC-61 250 mW	SOT223/ SC-73 1.3 W	SOT323/ SC-70 200 mW	SOT346/ SC-59 250 mW	SOT363/ SC-88 200 mW	SOT416/ SC-75 150 mW	SOT490/ SC-89 250 mW	OTHER FEATURES
Resistor-equipped transistor with two different resistor combinations											
50 V, 100 mA	npnp							PUMD48			For npn R1/R2: 47 kΩ/47 kΩ For pnp R1/R2: 2.2 kΩ/47 kΩ
High current transistors											
20 V, 1 A	pnp		BC869		BCP69						
	npn		BC868		BCP68						
45 V, 1 A	pnp				BCP51					BCX51	
	npn				BCP54					BCX54	
60 V 1 A	pnp				BCP52					BCX52	
	npn				BCP55					BCX55	
80 V, 1 A	pnp				BCP53					BCX53	
	npn				BCP56					BCX56	
High-voltage transistors											
150 V, 300 mA	pnp	PMBT5401			PZT5401	PMST5401					low capacitance: C_C < 6 pF
160 V, 300 mA	npn	PMBT5550			PZT5551	PMST5550					low capacitance: C_C < 6 pF
300 V, 500 mA	pnp	PMBTA92	PXTA92		PZTA92	PMSTA92					
300 V, 500 mA	npn	PMBTA42	PXTA42		PZTA42	PMSTA42					
350 V, 300 mA	npn				PZTA44						
General purpose transistors											
40 V, 100 mA	npn					2PC4081[1]					
40 V, 500 mA	pnp					2PA1576[1]			2PA1774[1]		high amplifications at high currents
45 V, 100 mA	pnp	BC857				BC857W	2PB709A[1]		BC857T	BC857F	
45 V, 100 mA	npn									BC847F	

MAX. V_{CEO} & I_C	POL.	POLARITY TYPE RANGE - SORTED BY PACKAGE TYPE AND POWER (P_{TOT}) RATING									
		SOT23 250 mW	SOT89/ SC-62 1.2 W	SOT143/ SC-61 250 mW	SOT223/ SC-73 1.3 W	SOT323/ SC-70 200 mW	SOT346/ SC-59 250 mW	SOT363/ SC-88 200 mW	SOT416/ SC-75 150 mW	SOT490/ SC-89 250 mW	OTHER FEATURES
45 V, 500 mA	pnp	BC807				BC807W					high amplifications at high currents
45 V, 500 mA	npn	BC817				BC817W					high amplifications at high currents
50 V, 100 mA	npn						2PD601A[1]		2PC4617[1]		
50 V, 500 mA	pnp						2PD602A				high amplifications at high currents
50 V, 500 mA	npn						2PB710A				high amplifications at high currents
65 V, 100 mA	pnp	BC856				BC856W			BC856T		
65 V, 100 mA	npn	BC846				BC846W			BC846T		
General purpose transistor arrays											
T1/T2: 30 V/6 V, 100 mA	pnp			BCV62 BCV64							current mirror Schmitt trigger
T1/T2: 30 V/6 V, 100 mA	npn			BCV61 BCV63							current mirror Schmidt trigger
T1/T2: 40 V, 100 mA	npn							PUMX1			
T1/T2: 40 V, 100 mA	pnp							PUMT1			
T1/T2: 40 V, 100 mA	pnpn							PUMZ1			
T1/T2: 45 V, 100 mA	pnp							BC857BS			tight h_{FE} matching

MAX. V_{CEO} & I_C	POL.	POLARITY TYPE RANGE - SORTED BY PACKAGE TYPE AND POWER (P_{TOT}) RATING									
		SOT23 250 mW	SOT89/ SC-62 1.2 W	SOT143/ SC-61 250 mW	SOT223/ SC-73 1.3 W	SOT323/ SC-70 200 mW	SOT346/ SC-59 250 mW	SOT363/ SC-88 200 mW	SOT416/ SC-75 150 mW	SOT490/ SC-89 250 mW	OTHER FEATURES
T1/T2: 45 V, 100 mA	npn							BC847BS			tight h_{FE} matching
T1/T2: 45 V, 100 mA	npnp							BC847BPN			tight h_{FE} matching
T1/T2: 65 V, 100 mA	pnp							BC846S BC856S			in development

Notes

1. Only available in tight DC current gain groups.
2. Release planned for Q2/1999.

POWER MOSFETs, 20 V to 300 V N- and P-channel complementary multi-chip

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@V_{GS} (V)	I_{DS} (A)	PACKAGE (SURFACE MOUNT)					TYPICAL APPLICATION (see notes)
				TSOP6 (SOT457)	TSSOP8 (SOT530)	SO8 (SOT96)	SO24 (SOT137)	SSOP24 (SOT340)	
20	2 x 0.04 (N) + ESD	2.5	5		BSH301[6]				4
25	1 x 0.03/ 6 x 0.08 (N)	10	5					PHN70308	2
25	6 x 0.035 (MOS), 6 x 5A Schottky	10	8.3				PHN603S		5
30	2 x 0.03 (N)	10	5.2			PHN203			2, 3
30	0.05 (N)/ 0.12 (P)	10	6.4 (N) / 4 (P)			PHC20512			2, 4
30	0.1 (N)/ 0.25 (P)	10	3.5 (N) / 2.3 (P)			PHC21025			2, 4
30	2 x 0.05(N)	10	6.4			PHN205			2, 4
30	2 x 0.1 (N)	10	3.5			PHN210			2, 4
30	2 x 0.12(P)	10	4			PHP212			2, 4
30	2 x 0.25(P)	10	2.3			PHP225			2, 4
50	2 x 10 (P)	10	0.19	BSH403					4
60	2 x 4 (N)	10	0.29	BSH303					4
300	8 (N)/ 17 (P)	10	0.3 (N) / 0.2 (P)			PHC2300			1

Notes

1. Telecom line switching protection.
2. Telecom power conversion.
3. Telecom DC-DC conversion.
4. Telecom power (battery) management.
5. Universal Serial Bus (USB).
6. In development.

POWER MOSFETs, 12 V to 300 V P-channel single chip

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@V_{GS} (V)	I_{DS} (A)	PACKAGE						TYPICAL APPLICATION (see notes)
				SURFACE MOUNT					LEADED	
				SOT223	SO8 (SOT96)	SOT23	SOT363	TSOP6 (SOT457)	TO-92 (SOT54)	
12	0.15	2.5	1.98					BSH207		4
12	0.5	2.5	1.01				BSH206			4
12	0.5	2.5	0.86			BSH205				4
30	0.09	10	5.7	BSP090						2, 4
30	0.09	10	5		PHP109					2, 4
30	0.25	10	3	BSP250						2, 4
30	0.25	10	2.5		PHP125					2, 4
30	0.9	10	0.57			BSH202				4
30	1.1	2.5	0.57			BSH203				4
45	14	10	0.25							1, 2
50	10	10	0.13			BSS84				1, 2
60	2.5	10	0.34			BSH201				4
200	12	10	0.225	BSP220						1, 2
250	15	10	0.225	BSP225						1, 2
250	15	10	0.2						BSP254A	1, 2
300	17	10	0.21	BSP230						1, 2
300	17	10	0.17						BSP304A	1, 2

Notes

1. Telecom line switching protection.
2. Telecom power conversion.
3. Telecom DC-DC conversion.
4. Telecom power (battery) management.

REPLACED/WITHDRAWN TYPES

The following type numbers were included in the previous issue of this data handbook, but are not in the current edition.

TYPE NUMBER	REASON FOR DELETION
BGY204	To be discontinued soon
BSH104	Moved to other handbook
BSH105	Moved to other handbook
BSH106	Moved to other handbook
BSH107	Moved to other handbook
BSH203	Moved to other handbook
BSH204	Moved to other handbook
BSH205	Moved to other handbook
BSH206	Moved to other handbook
BSH207	Moved to other handbook
BSN20W	Moved to other handbook
BSP030	To be discontinued soon
BSP090	Moved to other handbook
OM4031T	Discontinued
P83CL886; P87CL886	Family will be replaced by VTELX early 2000
P83CL887; P87CL887	Family will be replaced by VTELX early 2000
PCD5041	Low production volume. No new design-in
PCD5042	Low production volume. No new design-in
PCD5043	Low production volume. No new design-in
PCD5094	No product
PCF5073	Replaced by PCF50731
PCF5083	Replaced by PCF5085
PHC20512	Moved to other handbook
PHC21025	Moved to other handbook
PHN205	Moved to other handbook
PHP212	Moved to other handbook
PHP212L	Discontinued
PHP225	Moved to other handbook
SA576	Moved to other handbook
SA577	To be discontinued soon
SA578	To be discontinued soon
SA617	To be discontinued soon
SA627	To be discontinued soon
SA637	To be discontinued soon
SA703	Removed from handbook

TYPE NUMBER	REASON FOR DELETION
SA5200	To be discontinued soon
SA5752	Discontinued
SA5753	Discontinued
SA9024	Not released from Development
SA9025	Not released from Development
TDA7050T	Moved to other handbook
UBA1710M	Discontinued
UMA1014	Replaced byUMA1015AM
UMA1015M	Replaced byUMA1015AM
UMA1018M	Not widely promoted
UMA1020M	Discontinued

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INTRODUCTION

Semiconductors for cellular phones

digital cellular

GSM/DCS/PCS digital cellular ICs

Philips Semiconductors' latest low-voltage, highly-integrated chipset is now in production, covering all functions – from antenna to microphone.

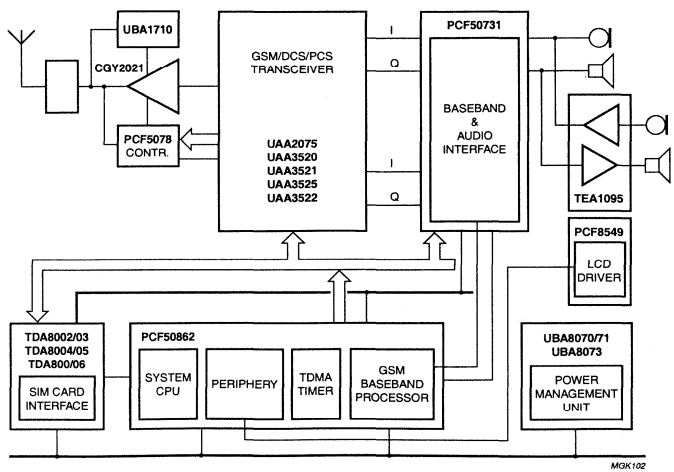
Overview

- Several fully integrated transceiver ICs are available for GSM900 DCS1800 and PCS1900. The UAA2075/UAA3520/3521/3525 have integrated front-end LNAs, reject-image mixers, modulators, demodulators and PLLs. They are all available in small LQFP 48-pin packages. The UAA3521HL is designed with the Tx modulation loop technique since other transceivers use up-mixer modulation.
- The UAA3522HL transceiver allows a highly-integrated GSM dual-band solution with the UAA2077DM front-end
- The BGY240S power amplifier module provides an off-the-shelf solution for 2 W GSM transmitters. The CGY2013 is an alternative MMIC solution for 3.6 V powered sets.
- The PCF5078 power amplifier controller ensures that power amplifier on/off and output characteristics meet GSM/DCS1800 requirements, Phase II.
- The baseband and audio interface IC, the PCF50731, is a single-chip interface between the RF transceiver, the microphone and earpiece, and the baseband processor. It integrates an audio codec and auxiliary AD/DA converter for AGC, AFC and power management.
- The highly-integrated single-chip controller IC, the PCF50862, incorporates a high-performance DSP (R.E.A.L.) and system controller in a very small BGA144 package.

GSM/DCS/PCS ICs

Type	Function
UAA2075	single-chip GSM transceiver
UAA3520	single-chip 3V GSM transceiver
UAA3521	single-chip GSM closed-loop transceiver
UAA3522 &	GSM dual band with UAA2077 Tx
UAA2077	modulation loop
UAA3525	single-chip DCS/PCS transceiver
TDA8002/03	SIM card interface
TDA8004/05	SIM card interface
TDA8006	
UBA8070/71	power management unit (PMU)
UBA8073	PMU with SIM card interface
	DC/DC converter
UMA1021M	low-voltage frequency synthesizer
BGY240S	power amplifier module
CGY2021	MMIC power amplifier
UBA1710	modulator for GaAs power amplifier
PCF5078	power amplifier controller for GSM
P90CL301	low-voltage microcontroller
PCF50731	GSM baseband and audio interface
PCF50862	GSM baseband controller
TEA1095	hands-free IC

GSM/DCS/PCS block diagram



Power management units (PMUs) for digital cellular phones

The UBA8070/71 are well optimized PMUs that come in small SSOP20 packages. Regulator performances can be adapted to phone standard specifications. On top of the PMU functions, the UBA8073 offers an integrated SIM card interface as well as a DC-DC converter.

IS-54/136(TDMA) digital cellular RF transceiver chipset

North American IS-54/136 is a time-division multiple-access (TDMA) system that increases the number of users from one to three per channel. The system must also support the analog AMPS system. Thanks to our experience with the low power AMPS chipset and input from customers, we have been able to produce a 3-chip solution for a dual-band or single-band IS-54/136 RF/IF section.

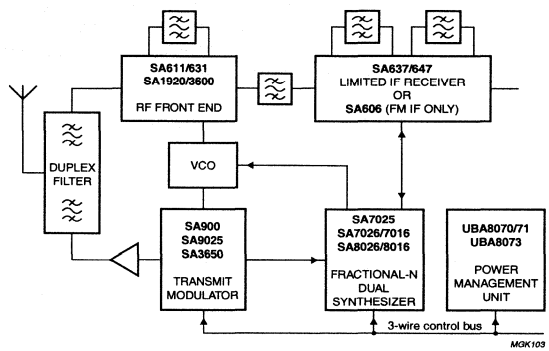
Overview

- A low-power, cost effective solution for single- and dual-band applications.
- Combines all the necessary RF and IF functions.
- A common high-speed serial interface makes addressing the devices simpler.
- The frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop.

TDMA RF ICs

Type	Function
SA3600	dual-band RF front-end
SA1920	dual-band RF front-end
SA9025	dual-band RF transmitter/modulator
SA647	IF digital receiver
SA611/631	low-voltage LNA and mixer – 1 GHz
SA621	low-voltage LNA mixer and VCO
SA637	low-voltage digital IF receiver
SA7026	low-voltage 1.3 GHz fractional-N synthesizer
SA900	I/Q transmit modulator
UBA8070/71	power management unit (PMU)

IS-54/136 block diagram



IS-95 CDMA RF ICs

Also trademarked under the "cdmaOne" logo, IS-95 is a code-division multiple access (CDMA) standard that uses spread-spectrum technology previously developed for military use. Intrinsically, the system is highly immune to interference whilst using the bandwidth in the available spectrum very efficiently.
This allows CDMA the largest number of users compared to other cellular systems. IS-95 also supports the analog AMPS standard.
Philips Semiconductors has been a key IS-95 IC supplier, providing custom solutions to the pioneering CDMA phone manufacturers using our vast experience in low-power AMPS ICs. We are now developing the SA95XX chipset to provide an attractive solution for building IS-95 dual-band, multi-mode radios.

Overview

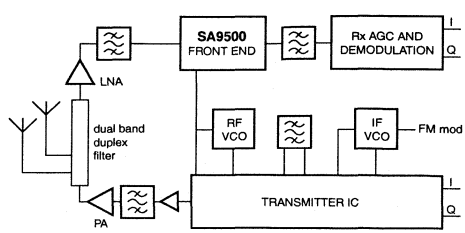
- A low-power, cost-effective solution for a dual-band CDMA/AMPS radio
- The SA95XX family provides a compact, highly-integrated approach for managing the RF and IF functions.

Currently, the family comprises:
- SA9500/SA9502 RF front-ends with dual-mode down-converter mixers
- transmitter ICs including dual synthesizers, I/Q modulator, variable gain amplifiers for Tx IF, up-converter mixers and RF pre-drivers.

- The frequency plan with either a common Rx IF or Tx IF may be selected to eliminate the need for an additional synthesizer and VCO loop in dual-band radios.

CDMA ICs

Type	Function
SA9500	low-voltage dual-band down converter for CDMA/AMPS
SA9502	low-voltage dual-band down converter for CDMA/AMPS



American Digital Cellular RF transceiver chip–sets (TDMA)

North American Digital Cellular (NADC) IS-54/-136 PCS TDMA RF Transceiver Chipsets

1st generation TDMA RF transceiver chip-set (Single-band 800MHz, Dual-mode AMPS/DAMPS)

The chip-set combines all of the necessary RF and IF functions into **four integrated devices**: the SA621 RF front end, the SA7025 dual frequency synthesizer, the SA900 I/Q transmit modulator and the SA637 digital IF receiver or SA606 FM IF receiver + external I/Q demodulator. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. There is also a common high speed serial interface bus, making addressing the devices simpler. Additionally the frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop. All of these features dramatically reduces the cost and size while improving the performance of the overall system.

Although this is our first IS-54/-136 solution, our 4-chip configuration is one of the most integrated and easy to use chip-set available. For example, the SA900 provides I/Q modulators, the phase shifter, the VGA, a filter, control logic, clock distribution and more in a single IC. The need for two RF synthesizers was eliminated by closely coupling the SA7025 and the SA900 so it is possible to use the main synthesizer to simultaneously generate receive and transmit signals. The integration and connectivity of the chip-set promote significant cost reduction. In addition this integrated solution reduces the time to a final product by simplifying the design effort.

Philips 1st generation TDMA RF transceiver chipset consists of the following ICs:

SA611/631	1GHz low voltage LNA and mixer
SA621	1GHz low voltage LNA, mixer and VCO
SA606	Low voltage high performance mixer FM/IF system
SA637	Low-voltage digital IF receiver
SA7025/SA7026	Low-voltage 1GHz and 1.3GHz fractional-N synthesizers
SA900	I/Q transmit modulator

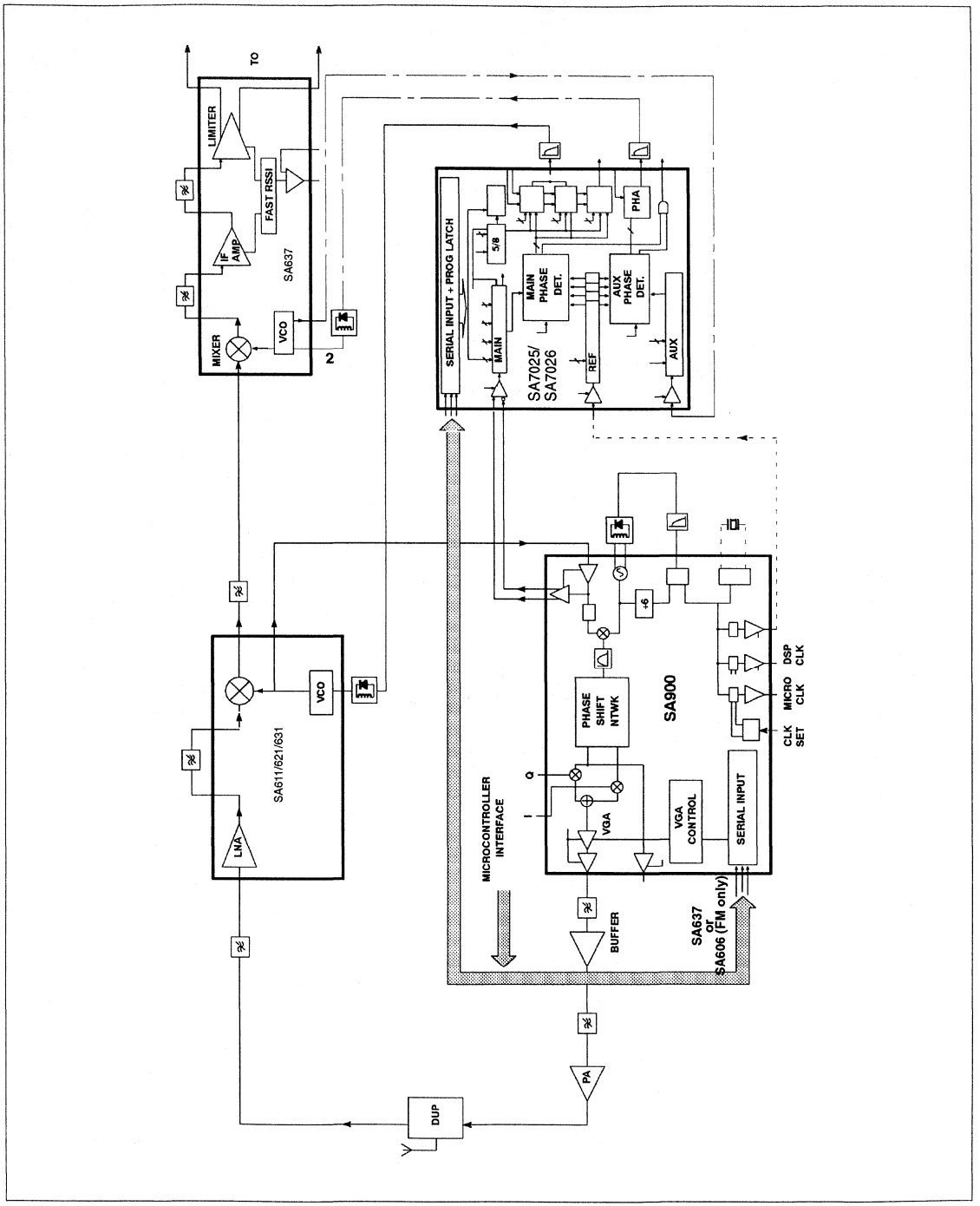
2nd generation TDMA RF transceiver chip-set (Dual-band 800/1900MHz, Triple-mode AMPS/DAMPS/PCS)

This chip-set combines all the necessary RF and IF functions into **three integrated devices**: the SA1920 RF dual-band front end, the SA647 Low power digital IF system receiver and the SA9025 I/Q transmit modulator with integrated dual fractional-N frequency synthesizer. This is the most highly integrated dual-band, triple-mode PCS chip-set available on the market. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. Additionally the frequency plan was designed to eliminate the need for any additional synthesizer and VCO loop. The result is a smaller, cost effective, low-power phone that is ultimately more attractive to the end users.

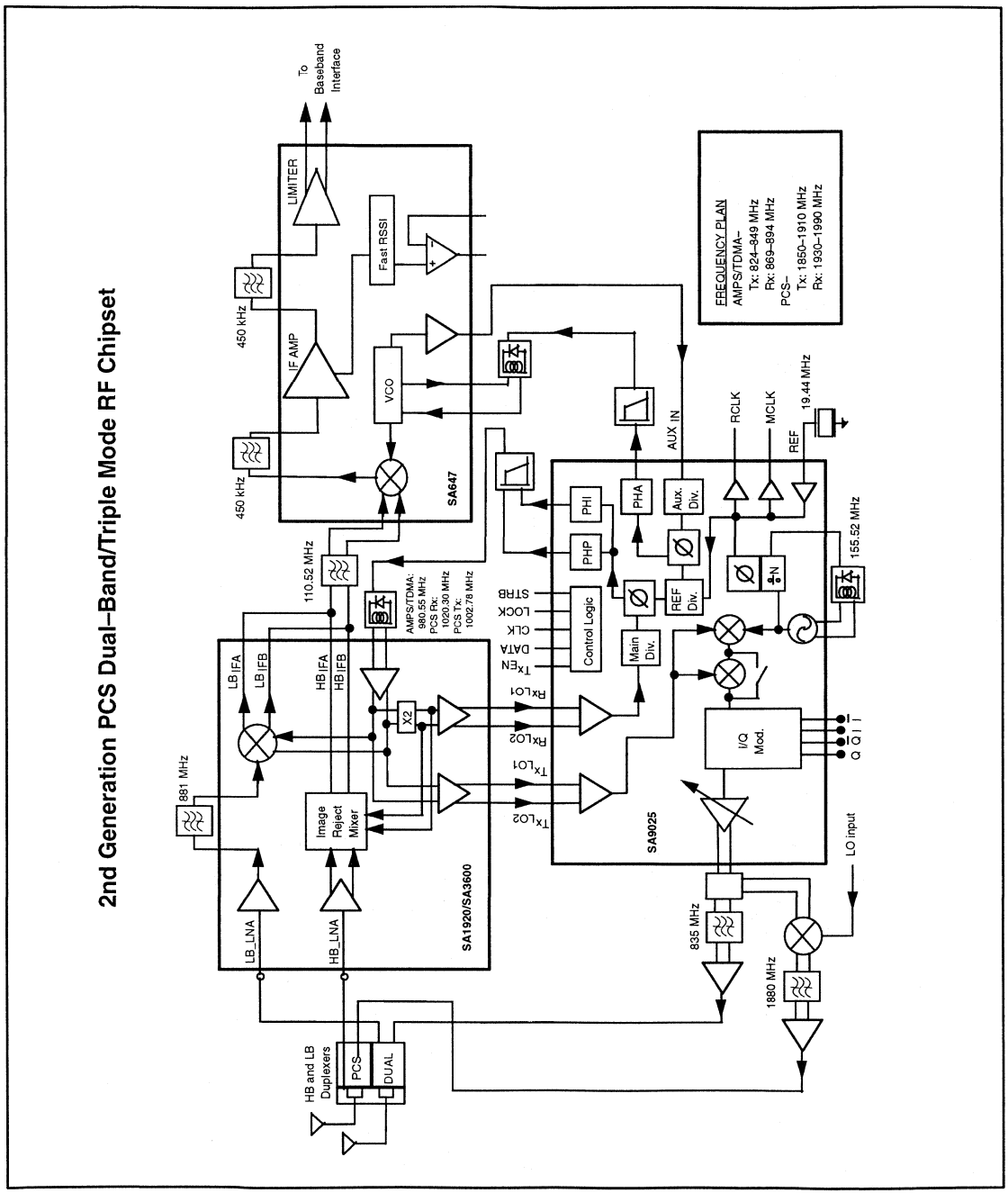
Philips 2nd generation TDMA (PCS) RF transceiver chipset consists of the following ICs:

SA3600	Low voltage dual-band 800/1900MHz RF front-end
SA1920	Dual-band 800/1900MHz RF Front-End
SA647	Low-Power FM IF System
SA9025	Transmit Modulator with integrated Dual Fractional-N synthesizer

1st generation TDMA RF transceiver chip–set (AMPS/DAMPS)



2nd generation TDMA RF transceiver chip-set (AMPS/DAMP/PCS)



Chipsets for cordless

digital cordless

DECT

Philips Semiconductors offers very competitive and complete DECT (Digital Enhanced Cordless Telecommunications) solutions including hardware, software and support for applications ranging from residential to 2-line business systems. Both off-the-shelf and customized solutions are available.

Residential and 2-line business systems

We offer several complete radio transceiver solutions. A dual-conversion 4-IC solution based on the UAA2067, UMA1022, SA639 and CGY2032 offers the designer maximum flexibility. Our first-generation zero-IF radio (based on the UAA2068, UAA2078/79) has now been replaced by a second generation, fully-integrated radio, using the UAA3540 and UAA2068 as key components.

The PCD509xy (ABC-Pro) family is a range of versatile low-power GAP-compliant single-chip baseband processor ICs designed to allow flexibility in the design of residential/small PBX systems and data applications. They enable a high degree of customization of the MMI, for example, speaker phone and conference calling. New OTP versions of the ABC-Pro expand the memory range to 128 kB OTP program memory to offer a fast market entry for new DECT products.

For digital answering machines, we offer the PCD6002 DTAM IC with an embedded R.E.A.L. DSP, which also connects to the ABC-Pro.

The PCD5096 (universal codec) integrates two audio codecs, a DSP (performs echo cancellation, conference call, DTMF, dial tone generation) and two PSTN interfaces onto one chip. Together with the ABC-Pro family, the universal codec meets all the requirements to create two-line PSTN low-cost digital cordless systems; it also adds functionality to high-end corded phones. In addition, the IOM-2 interface can provide analog line extensions for ISDN.

We offer a complete range of line-interface ICs, from the basic UBA1706 to highly featured ICs such as the UBA1707 for group listening and the TEA1099 for hands-free operation.

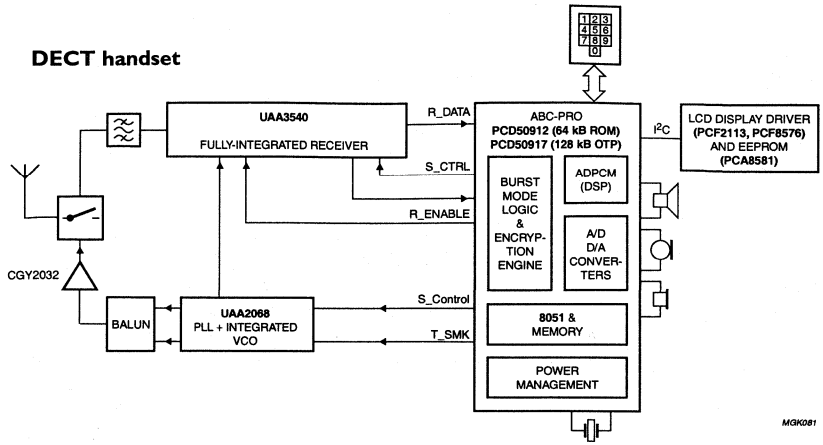
Philips Semiconductors also provides a full range of software to help you build your DECT products. All our software products are TBR22 compliant, where appropriate.
We also offer a fully featured user interface, which you can customise and enrich. We have software for residential, ISDN, CAP, small business and PBX systems. And we also offer our unique product for data applications - the "Virtual cable".

The Virtual Cable provides a simple way to communicate between computers and other industrial devices using DECT, at rates up to 56.6 kbits/s. With a range of 50-300 m, it offers a low-cost solution for many applications such as wireless point-of-sale terminals and stock control systems. The OM5878 software implements all data communications tasks and V.24 UART interfacing.

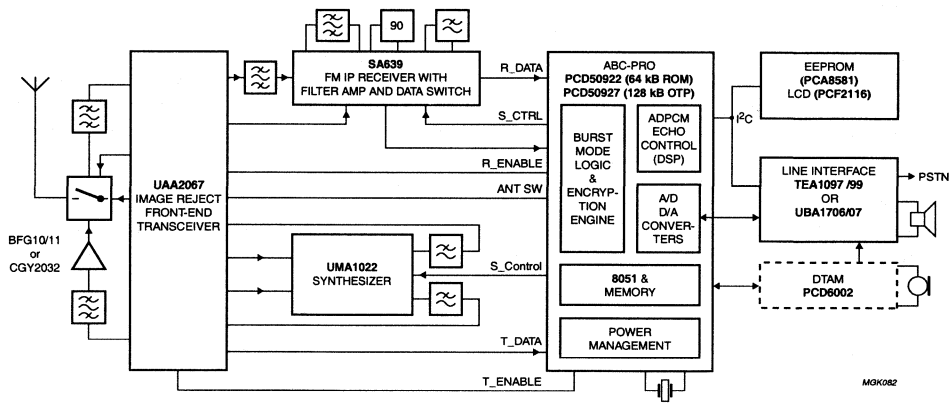
DECT ICs

Type	Function
UAA2067G	low-voltage 2 GHz RF transceiver
UAA2068G	PLL/VCO/doubler/modulator
UAA3540TS	fully integrated DECT receiver
UAA2078	Zero-IF front-end
UAA2079	Zero-IF filter/demodulator
SA639	low-voltage mixer FM IF system with filter amplifier and data switch
UMA1022M	low-voltage frequency synthesizer
CGY2032	low-voltage MMIC power amplifiers
PCD5091/2/3/4	single-chip baseband processor
PCD50912 PCD50917	ABC-Pro handset baseband controller
PCD50922 PCD50927	ABC-Pro base unit baseband controller
PCD50937	ABC-Pro baseband controller for ISDN base units
PCD5096	universal CODEC
TEA1097/99	featurephone ICs (base unit)
UBA1706/07	programmable speech/transmission ICs

DECT handset



DECT base unit (classic dual-conversion radio solution)

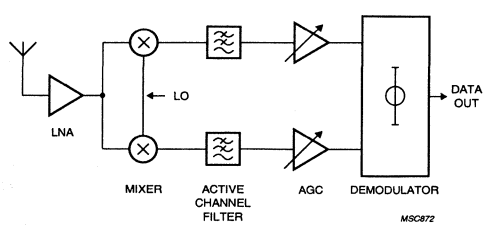


Radio receiver architectures

In our wide range of DECT RF ICs, we offer a choice of architectures for low-cost and high-end applications:

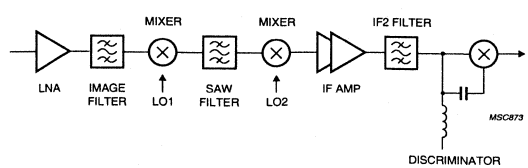
Zero-IF direct conversion

- Complete RF to data path on silicon
- Needs only one RF VCO, minimum tuning range
- Fully integrated solution is possible.



Superheterodyne RF

- Optimize material technology to function
- Designer free to choose best compromise
- Production line tuning can compensate cheap components.



AMPS/(E)TACS analog cellular

The transformation from a business-only to consumer market has driven the rapid growth of AMPS(E)TACS analog cellular phones. This growth continues in the United States and United Kingdom (where the standard originated) as well as mainland Europe, Asia and Latin America.

Our current AMPS/(E)TACS chipset employs 3 V technology to improve power consumption, standby and talktime in today's hand-held phones. 1998 saw the introduction of the SZF2002 baseband processor. This is a low voltage 8-bit microcontroller with embedded 6 k + 256 bytes low power RAM data memory, expandable externally to 32 kbytes. It also contains 6 kbytes ROM program memory, expandable externally to 256 kbytes. The internal AUX RAM can be used for program execution. The SZF2002 has three 8-bit ports and 24 I/O lines. Furthermore, it has internal demultiplexing and latching of address/data bus to reduce system component count. The SZF2002 also includes an interface for up 256 kbytes of flash memory (banked).

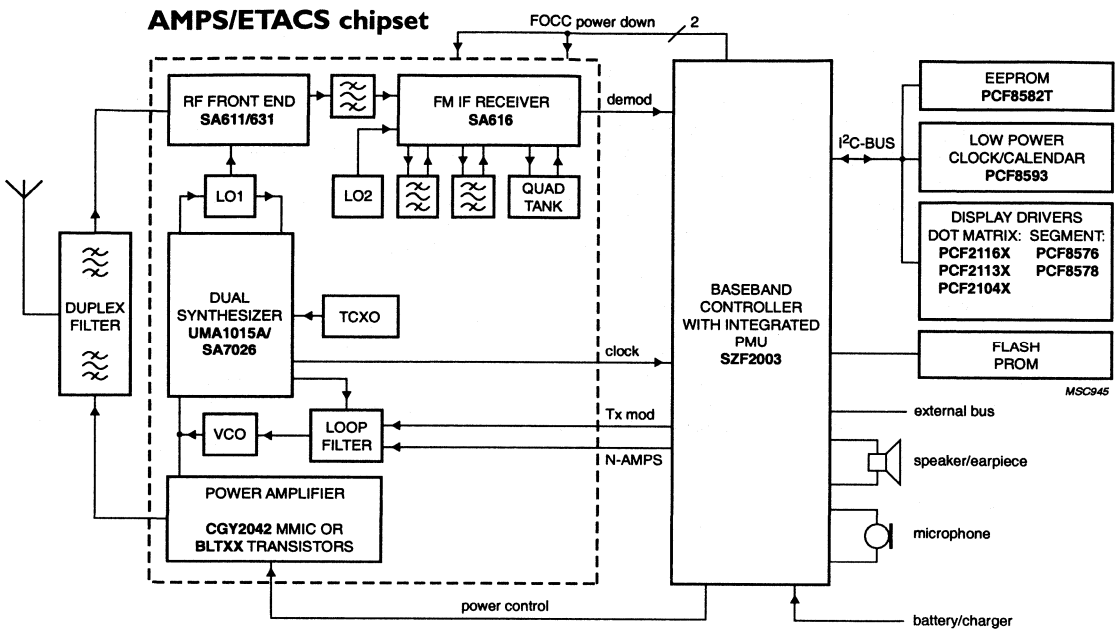
In 1999, the SZF2003 baseband processor will be introduced. This dedicated low-voltage AMPS processor has power management on board and 12 kbytes of low-power RAM data memory, externally expandable to 32 kbytes. The IC is manufactured in advanced 0.35 mm CMOS technology, has a low-power consumption and software selectable modes for power reduction. The SZF2003 includes DTMF detection.

Overview

- The RF Transceiver is composed of three low-voltage, high-performance ICs: the SA611 RF front-end, SA616 FM IF receiver and UMA1015AM dual frequency synthesizer. These ICs typically draw a total of 20 mA or less from a 3 V supply.
- Our BGY series of power modules and BLT series of power and driver transistors provide complete solutions for all power classes of AMPS(E)TACS products.
- The AMPS/(E)TACS baseband solution handles all audio and data processing, control and memory functions.
- Evaluation kits for AMPS (OM4753) and (E)TACS (OM4751), and a demonstration software package (OM4752) are available.

AMPS/(E)TACS ICs

Type	Function
SA611	low-voltage LNA and mixer – 1 GHz
SA616	low-voltage high-performance mixer FM IF system
SA621	low-voltage LNA mixer and VCO
SA910	pre-driver
UMA1015AM	low-power dual frequency synthesizer
CGY2042	power amplifier MMIC
SZF2003	low-voltage baseband processor with PMU and DTMF detection
SZF2002	8-bit low-voltage microcontroller with embedded RAM
UMA1002	low-voltage data processor (DPROC)
TDA7050	audio amplifier


AMPS/ETACS chipset
FOCC power down
2
RF FRONT END
SA611/631
FM IF RECEIVER
SA616
demod
LO1
LO2
QUAD
TANK
DUPLEX
FILTER
DUAL
SYNTHESIZER
UMA1015A/
SA7026
TCXO
clock
VCO
LOOP
FILTER
Tx mod
N-AMPS
POWER AMPLIFIER
CGY2042 MMIC OR
BLTXX TRANSISTORS
power control
BASEBAND
CONTROLLER
WITH INTEGRATED
PMU
SZF2003
I²C-BUS
EEPROM
PCF8582T
LOW POWER
CLOCK/CALENDAR
PCF8593
DISPLAY DRIVERS
DOT MATRIX: SEGMENT:
PCF2116X PCF8576
PCF2113X PCF8578
PCF2104X
FLASH
PROM
MSC945
external bus
speaker/earpiece
microphone
battery/charger

analog cordless

Analog cordless

Philips Semiconductors fully supports the CT0 analog cordless standard with low, mid-range and high-end, highly integrated chipsets.
The low-frequency CT0 analog cordless standard is established in many countries at various frequencies around 50 MHz, including: France (26/41 MHz), Australia (30/39 MHz), The Netherlands and Spain (31/40 MHz), China, S. Korea, Taiwan, USA, Latin America (46/49 MHz), and China (48/74 MHz.).
CT0 chipsets comprise:

- highly integrated transceiver Combo ICs – the UAA2060 and UAA2062
- low voltage TELX baseband processors – P8XCL883/4/6/7
- DSP-based solutions – PCD6002 answering machine and baseband processor
- optimized line interface solutions, depending on the features required.

For other analog standards, we offer a complete range of standard components, including synthesizers, microcontrollers and line-interface ICs.

RF

The UAA2060 and UAA2062 are state-of-art transceiver ICs featuring integration from antenna down to audio. The UAA2060 features a double superhet receiver architecture, on-chip LNA, PLL demodulator, a dual PLL synthesizer, Tx VCO as well as Tx PA. Additionally, microphone and earpiece amplifiers, and a compandor are included. The UAA2060 is programmable via the 3-wire serial bus and is targeted for use in Europe. With all the features of the UAA2060, the UAA2062 is suitable for all countries and adds a clock output to drive a microcontroller.

The high integration level provided in the UAA2060 and UAA2062 eliminates the need for a large number of external components needed with traditional solutions. Moreover, the number of tuning points is significantly reduced because LNA and VCOs can be tuned via the 3-wire serial bus.

Line-interface ICs

We also have a full range of line-interface ICs, from the basic UBA1706 to highly-featured ICs such as the UBA1707 for group listening and the TEA1099 for hands-free operation.

Other recent additions to our range include the TEA1118 and TEA1118A, which are derivatives of our TEA1112/A speech/transmission ICs. These new ICs have transmit inputs which handle signals up to 1 V rms with less than 2%THS, and have low transmit gain (typically 11 dB).
The TEA1118A incorporates DTMF, mute and transmit inputs, and is therefore particularly suitable for CT0. The TEA1099 is unique in the telephony marketplace. It offers auxiliary transmit and receive channels in addition to normal handset, speakerphone and DTMF insertion functions. This makes it ideal for multi-line phones and cordless base-stations (see "Line-interface ICs for cordless phones").

Baseband

Our TELX baseband processors are advanced 80CL51-core microcontrollers with special features for analog cordless applications.
With their many function-specific dedicated blocks, they provide a high level performance with low power consumption, and they also offer software-selectable idle and power-down modes. Capabilities such as a 400 Kbits/s I^2C-bus interface, which allows in-circuit programming, add flexibility for customization with just-in-time production. What's more, they include an on-board DTMF generator, EEPROM, MSK modem, PWM output and software-programmable low-voltage detection (LVD).

Manufactured in a special low-cost EPROM process, TELX processors provide cost-effective user-programmability at a price previously only associated with ROM-masked devices.
The family is available in small-outline 28-pin packages.

TELX microcontrollers (80CL51core-based, optimized for telecom)

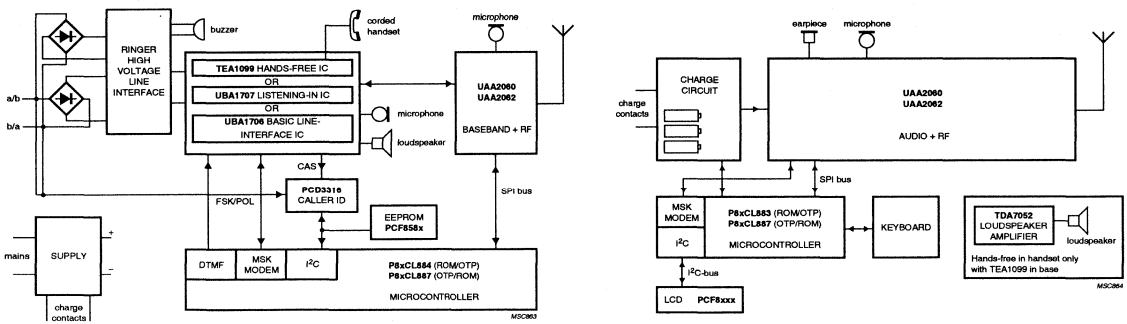
Type	ROM (kB)	RAM (B)	EEPROM (B)	I/O	Operating voltage (V)	Special features	Package	Max. speed (MHz)	Category
P83CL881	63	2048	–	32	2.7–3.6	UART, 400 Kbits/s I²C-bus, low-voltage detection	LQFP44	10[1]	TELX
P87CL881	63 (OTP)	2048	–	32	2.7–3.6	OTP version of P83CL881	LQFP44	10[1]	TELX
P83CL883	8	256	–	18	2.7–3.6	UART, MSK modem, 400 Kbits/s I²C-bus, DTMF, low-voltage det., In-System programming	SO28	3.58[1,2]	TELX
P87CL883	8 (OTP)	256	–	18	2.7–3.6	OTP version of P83CL883	SO28	3.58[1,2]	TELX
P83CL884	8	256	128	18	2.7–3.6	Same as P83CL883 but with additional 256 bytes EEPROM	SO28	3.58[1,2]	TELX
P87CL884	8 (OTP)	256	128	18	2.7–3.6	OTP version of P83CL884	SO28	3.58[1,2]	TELX
P83CL886	16	512	–	18	2.7–3.6	Same as P83CL883, but larger program memory size	SO28	3.58[1,2]	TELX
P87CL886	16 (OTP)	512	–	18	2.7–3.6	OTP version of P83CL886	SO28	3.58[1,2]	TELX
P83CL887	12	512	–	18	2.7–3.6	Same as P83CL883, but larger program memory size	SO28	3.58[1,2]	TELX
P87CL887	12 (OTP)	512	–	18	2.7–3.6	OTP version of P83CL887	SO28	3.58[1,2]	TELX
PCD6002	32 (OTP)	768	–	34	2.7 – 3.6	DTAM chip incl. µC, DSP and MSK modem, DTMF	QFP80	3.58	DTAM
PCD3316	–	–	–	–	2.5 – 3.6	CIDCW receiver	SO16L	3.58M/32k[3]	CID

Notes

[1] TELX core is twice as fast as standard 80C51, i.e. 10 MHz clock corresponds to 20 MHz clock on standard 80C51 with same performance

[2] For DTMF

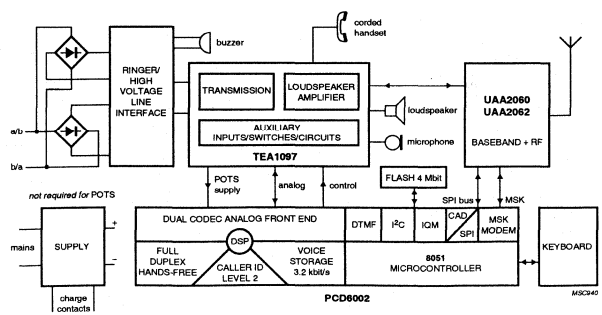
[3] 2 crystals are required: one for RTC, the other to be shared with the microcontroller for DTMF generation.



Mid-range CT0 chipset: base unit (left) and handset (right)

CT0 ICs

Type	Function
UAA206x	transceiver
TELX microcontroller	see table above
PCD3316	see "Caller Identification"
PCD6002	see "DSP-based solutions"
TEA1118A	speech/transmission IC (base unit)
TEA1097/99	featurephone ICs (base unit)
UBA1706/07	programmable speech/transmission ICs (base unit)
TDA7052A/AT	1 W low-voltage audio power amp with DC volume control



High-end CT0 base unit with integrated digital answeringmachine, CID-2 and full-duplex hands-free function.

Chipsets for paging

paging

Advancing in technology and design our pager chipsets are the best option not only for pager manufacturers but also for companies facing the challenges of the wireless telecommunication. We offer chips for all the key functions of numeric and alphanumeric pagers, covering all signal standards. Thanks to their universal design and flexibility they offer also excellent solutions for non-pager applications like car security, remote metering and PDIs.

Powerful POCSAG chipset

The UAA2080/2082 high-performance low-power receivers are primarily intended for VHF and UHF (25-512 MHz) wide-area digital pagers. They employ direct FM non-return-to-zero (NRZ) frequency shift keying (FSK), and are based on the direct conversion principle (zero IF). And operating up to 2400 baud, they are unique in size, power consumption and performance advantages. Key features include high sensitivity and high dynamic range.
The UAA2082 has two additional features: a low battery detect voltage of 1.1 V and an internal oscillator that disconnects when using direct injection from a frequency synthesizer to further reduce current consumption. Together with the PCF5001 or PCD5003A POCSAG decoders, the receivers form a powerful chip set which is unique in size, power consumption and performance advantages. Key features include high sensitivity and high dynamic range. User friendly, PC-based pager development tools (OM4763 and OM4759) make it easy to evaluate, develop and debug pager based on these ICs.

FLEX™ Pager Decoder

The PCD5013 decoder is an innovative IC for next generation high-speed paging protocols. Designed for FLEX™, the IC decodes fast data transmission with reduced paging errors.
Power reduction features allow the design of pagers with a very long battery life.
The PCD5013 interfaces with most off-the-shelf receivers.
The strengths of the device are its extremely low Electro Magnetic Interference susceptibility and the lowest operating current in the industry. A PCD5013 demo system is available. It enables pager designers to debug their software and shorten the system development phase.

The PCA5007 and PCA5010 represent a big innovation push to revolutionize the design of pagers. Together with our UAA3500 4-level FSK pager receiver, the PCA5007 or PCA5010 form an unrivalled chipset for modern pager design. The key strengths of this outstanding chipset are: a perfect receiver-controller combination, highly improved ZIF concept, low component count, extremely low radiation baseband, small size pager sets, signal code flexibility by software, OTP for fast market introduction, longer battery life, and last but not least, a system cost saving of 30-50%.
FLEX™ is a trademark of the Motorola Corporation.

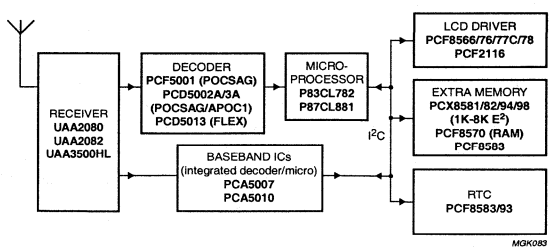
Pager Baseband Processor

The P87CL881 low-voltage baseband processor features 63k program memory and 2k RAM. It interfaces with the PCF5001 and PCD5013 pager decoders to process the decoded pager data. Its comprehensive I/O and built-in 400 Kbits/s I2C-bus enables easy interfacing to a wide range of peripherals such as LCD drivers, EEPROM memory and real-time clock circuits.

PAGING ICs

Type	Function
UAA2080	advanced pager receiver
UAA2082	advanced pager receiver
PCD5003A	advanced POCSAG paging decoder
PCD5002A	APOC1/POCSAG decoder
PCF5001	POCSAG paging decoder
P87CL881	low-voltage microcontroller
PCD5013	FLEX™ decoder
PCA5007	baseband decoder for all pager standards
PCA5010	baseband decoder for all pager standards
UAA3500HL*	pager receiver for all bands (130-930 MHz)

* Compatible with high- (FLEX™, ERMES) and low-speed standards; available mid 1999



Baseband processors

baseband processors

Completing our large portfolio of RF products is an impressive array of baseband processors for the primary digital/analog cellular, digital cordless and paging standards.

Digital cellular

Philips Semiconductors has now started production on a 3rd generation digital cellular chipset suitable for GSM, TDMA and CDMA applications.
The chipset comprises:

- PCF50862 single chip baseband processor
- PCF50731 baseband & audio-interface
- PCF5077 or PCF5078 power amplifier controller
- TDA8003 SIM controller.

Analog cellular

The SZF2003 is a baseband processor with a power-management unit and has embedded data RAM for AMPS handsets.
The SFZ2002 baseband processor is a low-voltage 8-bit microcontroller with embedded memory. Both fit into our second generation audio and data processor chipset, which provides a low-power, cost-effective solution for AMPS and (E)TACS cellular phones.
The SA5752 and SA5753 form the audio processing portion of this set. The UMA1002 provides data transceiving, data processing and SAT functions (including on-chip filtering). In full operation, these three ICs draw typically less then 7 mA from a 3 V supply.

Digital cordless

Philips' evolutionary ABC-Pro chip family combines the ABC family know-how with the tomorrow's cordless requirements.
This single-chip baseband family is GAP and CAP compliant and offers outstanding audio quality. Offering 500 hours standby time and hands-free functionality for the handset (PCD50912), and caller identification in the base unit (PCD50922), these devices greatly enhance products for the residential and small office market. ABC-Pro ICs perform all speech formatting, audio processing and MMI functions. The PCD50937 is designed to address the home and business market of ISDN. The Universal Codec (PCD5096) extends the analog interfaces for small business applications. The ABC-Pro family is fabricated in our low voltage CMOS process.

Analog Cordless

Philips TELX CT0/900 MHz baseband processor family combined with the complementary UAA2060 Combo RF IC provides a minimum component-count solution. Additional features, such as caller-identification can be easily added and controlled via the built-in hardware I^2C-bus. Thanks to the built-in MSK modem, caller-ID information in the base-station can easily be relayed to the handset.

Paging

The PCD5003A is a very low power POCSAG decoder and pager controller.
It supports data rates of 512, 1200 and 2400 bps using a single 78.6 kHz crystal.
An on-chip EEPROM is programmable with a minimum supply of 2.5 V. The PCD5003A draws only 50 mA from a 1.5-6 V supply.
The PCD5002A is a very low power, advanced pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC1 code for extended battery economy. Data rates supported are 512, 200 and 2400 bps using a single 76.8 kHz crystal. An on-chip EEPROM (384 bit) is programmable using a minimum supply voltage of 2.5 V. Key features include an advanced ACCESS synchronization algorithm, 2-bit random and (optional) 4-bit burst error correction, up to 6 user address frames that are independently programmable and, optionally, continuous data decoding upon reception of user programmable sync word.
For FLEX™ we offer the PCD5013 decoder which works at 1600, 3200 and 6400 bps. The IC offers 16 short or 8 long addresses with 16 fixed temporary addresses, any-phase decoding, an RTC time base and "over-the-air" time update support, and is compatible with synthesized receivers.
The PCD5013 belongs to the second generation of FLEX chips with built-in 455 kHz demodulator and roaming capability. The device includes a low battery indication (external detector), extremely low power consumption from a 1.8 - 3.6 V supply and low susceptibility to electromagnetic interference.
It comes in a low-profile LQFP32 package.
The PCA5007 and PCA5010 represent a big innovation push to revolutionize pager design; these unique products are based on the first worldwide implementation of a full static asynchronous 80C51 microcontroller. The outstanding performance of the micro-core means current consumption is 4-6 times lower than comparable 8 bit microcontrollers. Decisive for paging, however, is the complete lack of EMI in the pager frequency band – one factor that immediately and substantially reduces system costs.

Baseband processors

Type	Part type	Application	V_{DD} (V)	I_{DD} (mA)	Package
PCF50862	single-chip baseband	GSM/DCS/PCS	1.5 – 3.3	--	BGA144
PCF50731	baseband & audio interface	GSM/DCS/PCS	1.5 – 3.0	--	LQFP64
P90CL301	16-bit low-voltage microcontroller	digital cellular	2.7 – 3.6	--	LQFP80
PCF5077	power amplifier controller	digital cellular	2.7 – 5.5	--	SSOP16
PCF5078	power amplifier controller	digital cellular	2.4 – 5.5	--	TSSOP8
SFZ2003	baseband processor with PMU	AMPS	2.7 – 3.3	10 typ. 0.7 (down mode)	LQFP128
SZF2002	8-bit low-voltage microcontroller	AMPS	2.7 – 3.3	0.22 mA/MHz active 83 µA/MHz idle	LQFP80
SA5750	audio companding amplifier	AMPS, TACS	5.0	8.4 typ., 1.8 stby	DIP24, SOL28
SA5751	audio filter and control	AMPS, TACS	5.0	2.7 typ., 0.9 stby	DIP24, SOL28
SA5752	audio companding VOX and amplifier	AMPS, TACS	2.7 – 5.5	3.1 typ., 125µA stby	SO20L, SSOP20
SA5753	audio filter and control	AMPS, TACS	3.0 – 5.5	1.7 typ., 600 µA stby	SO20L, SSOP20
PCD509XY	baseband processor, ABC-Pro	DECT, ISDN	1.8 – 3.6	--	LQFP80
PCD5096	universal codec	DECT, ISDN	2.7 – 3.6	--	QFP 44
P8XCL883/4/6/7	TELX microcontroller	CT0/900 MHz	2.7 – 3.6	--	SO28
PCF5001	POCSAG decoder	Paging	1.5 – 6.0	60 µA typ.	SO28L, LQFP32
PCD5002A	APOC1/POCSAG decoder	Paging	1.5 – 6.0	25 µA typ. (OFF) 50 µA typ. (ON)	LQFP32
PCD5003A	advanced POCSAG paging decoder	Paging	1.5 – 6.0	25 µA typ. (OFF) 50 µA typ. (ON)	LQFP32
PCA5007	pager baseband controller for all signal standards	Paging	0.9 – 1.6	50 µA typ. (standby) 200 µA typ. (operating)	LQFP48
PCD5008	FLEX decoder	Paging	1.8 – 3.3	6.8 µA typ.	LQFP32
PCD5013	FLEX decoder with roaming capability	Paging	1.8 – 3.3	6.5 µA typ.	LQFP32
PCA5010	pager baseband controller for all signal standards	Paging	0.9 – 1.6	50 µA typ. (standby) 200 µA typ. (operating)	LQFP48

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

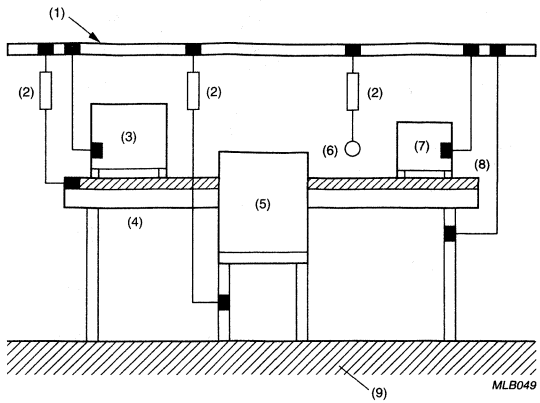
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

(in alphanumeric sequence)

UHF amplifier modules BGY122A; BGY122B

FEATURES

- Single 4.8 V nominal supply voltage
- 1.2 W output power
- Easy control of output power by DC voltage
- Very high efficiency (typ. 55%)
- Silicon bipolar technology
- Standby current less than 100 μA.

APPLICATIONS

- Hand-held transmitting equipment operating in the 824 to 849 MHz and 872 to 905 MHz frequency ranges.

DESCRIPTION

The BGY122A and BGY122B are three-stage UHF amplifier modules in a SOT388B package. Each module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.
The modules produce an output power of 1.2 W into a load of 50 Ω with an RF drive power of 2 mW.

PINNING - SOT388B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

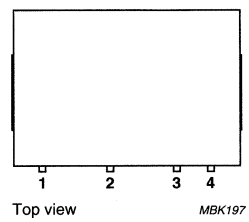


Fig.1 Simplified outline.

QUICK REFERENCE DATA

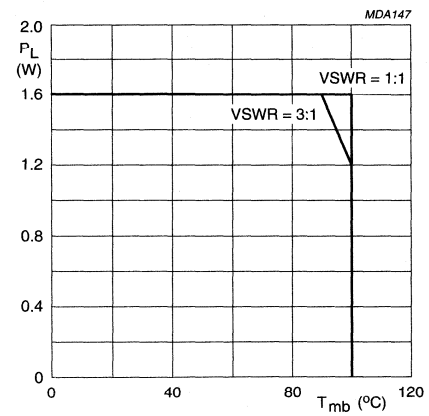
RF performance at T_{mb} = 25 °C.

TYPE	MODE OF OPERATION	f (MHz)	V_S (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
BGY122A	CW	824 to 849	4.8	1.2	≥27.8	typ. 55	50
BGY122B	CW	872 to 905	4.8	1.2	≥27.8	typ. 55	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	$V_C = 0$; $P_D = 0$	–	10	V
V_C	DC control voltage		–	3.5	V
P_D	input drive power		–	5	mW
P_L	load power		–	1.6	W
T_{stg}	storage temperature		−40	+100	°C
T_{mb}	operating mounting base temperature		−30	+100	°C



V_S = 6.5 V.

Fig.2 Load power derating curve.

CHARACTERISTICS

$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $V_C \leq 3$ V; $T_{mb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency					
	BGY122A		824	–	849	MHz
	BGY122B		872	–	905	MHz
I_Q	total quiescent current	$V_C = 0$; $P_D < -60$ dBm	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 1.2$ W	–	–	500	μA
P_L	load power	$V_C = 3$ V	1.2	–	–	W
G_p	power gain	adjust V_C for $P_L = 1.2$ W	27.8	–	–	dB
η	efficiency	adjust V_C for $P_L = 1.2$ W	50	55	–	%
H_2	second harmonic	adjust V_C for $P_L = 1.2$ W	–	–	−36	dBc
H_3	third harmonic	adjust V_C for $P_L = 1.2$ W	–	–	−36	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 1.2$ W	–	–	3 : 1	
	stability	$P_D = 0$ to +6 dBm; $V_S = 4$ to 6.5 V; $V_C = 0$ to 3 V; $P_L \leq 1.2$ W; VSWR ≤ 6 : 1 through all phases	–	–	−60	dBc
	isolation	$V_C = 0$	–	−40	–	dBm
P_n	noise power	adjust V_C for $P_L = 1.2$ W; bandwidth = 30 kHz; $f_n = f_o + 45$ MHz	–	–	−90	dBm
	ruggedness	$V_S = 6.5$ V; adjust V_C for $P_L = 1.4$ W; VSWR ≤ 10 : 1 through all phases	no degradation			

UHF amplifier module BGY205

FEATURES

- 6 V nominal supply voltage
- 3.5 W pulsed output power
- Easy control of output power by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 880 to 915 MHz frequency range.

DESCRIPTION

The BGY205 is a four-stage UHF amplifier module in a SOT321B package. The module consists of four NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT321B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

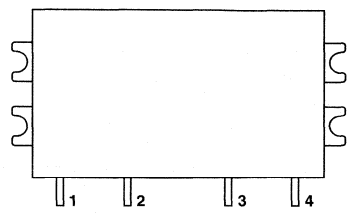


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
Pulsed; δ = 1 : 8	880 to 915	6	≤4	3.5	≥32.5	≥40	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	DC supply voltage	–	8.5	V
V_C	DC control voltage	–	4.5	V
P_D	input drive power	–	7	mW
P_L	load power	–	4	W
T_{stg}	storage temperature	−40	+100	°C
T_{mb}	operating mounting base temperature	−30	+100	°C

CHARACTERISTICS

$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $V_C \leq 4$ V; f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.5$ V	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 3.5$ W	–	–	500	μA
P_L	load power	$V_C = 4$ V	3.5	–	–	W
G_p	power gain	adjust V_C for $P_L = 3.5$ W	32.5	–	–	dB
η	efficiency	adjust V_C for $P_L = 3.5$ W	40	45	–	%
H_2	second harmonic	adjust V_C for $P_L = 3.5$ W	–	–	−40	dBc
H_3	third harmonic	adjust V_C for $P_L = 3.5$ W	–	–	−40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 3.5$ W	–	–	2 : 1	
	stability	$P_D = 0$ to 6 dBm; $V_S = 5$ to 8.5 V; $V_C = 0$ to 4 V; $P_L \leq 3.5$ W; VSWR ≤ 6 : 1 through all phases	–	–	−60	dBc
	isolation	$V_C = 0.5$ V	–	–	−36	dBm
	control bandwidth	R1 = 0; C1 = 0; see Fig.16	1	–	–	MHz
	AM-AM conversion	P_D with 3% AM; f = 100 kHz; $P_L = 3.5$ mW to 3.5 W	–	–	12	%
P_n	noise power	$P_L = 3.5$ W; bandwidth = 30 kHz; 20 MHz above transmitter band	–	–	−85	dBm
	ruggedness	$V_S = 8.5$ V; adjust V_C for $P_L = 3.5$ W; VSWR ≤ 10 : 1 through all phases	no degradation			

UHF amplifier module BGY206

FEATURES

- 4.8 V nominal supply voltage
- 3 W output power
- Easy control of output power by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 880 to 915 MHz frequency range.

DESCRIPTION

The BGY206 is a three-stage UHF amplifier module in a SOT388B package. The module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT388B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

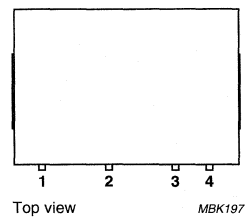


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
Pulsed; δ = 1 : 8	880 to 915	4.8	≤3.5	3	≥30	typ. 45	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	$V_C < 0.5$ V	–	10	V
V_C	DC control voltage		–	4	V
P_D	input drive power		–	13	mW
P_L	load power		–	3.5	W
T_{stg}	storage temperature		–40	+100	°C
T_{mb}	operating mounting base temperature		–30	+100	°C

CHARACTERISTICS

$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ mW; $V_S = 4.8$ V; $V_C \leq 3.5$ V; f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.5$ V	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 3$ W	–	–	500	μA
P_L	load power	$V_C = 3.5$ V	3	–	–	W
		$V_C = 3.5$ V; $V_S = 4.3$ V; $T_{mb} = 85$ °C	2	–	–	W
G_p	power gain	adjust V_C for $P_L = 3$ W	30	–	–	dB
η	efficiency	adjust V_C for $P_L = 3$ W	40	45	–	%
H_2	second harmonic	adjust V_C for $P_L = 3$ W	–	–	–40	dBc
H_3	third harmonic	adjust V_C for $P_L = 3$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 3$ W	–	–	2.5 : 1	
	stability	$P_D = 1.5$ to 6 mW; $V_S = 4$ to 6.5 V; $V_C = 0$ to 3.5 V; $P_L \leq 3$ W; VSWR ≤ 6 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C = 0.5$ V	–	–	–36	dBm
	control bandwidth		1	–	–	MHz
P_n	noise power	$P_L = 3$ W; bandwidth = 30 kHz; 20 MHz above transmission band	–	–	–85	dBm
	ruggedness	$V_S = 6.5$ V; adjust V_C for $P_L = 3$ W; VSWR ≤ 10 : 1 through all phases	no degradation			

UHF amplifier module BGY240S

FEATURES

- 3.5 V nominal supply voltage
- 3 W output power
- Easy output power control by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 890 to 915 MHz frequency range.

DESCRIPTION

The BGY240S is a three-stage UHF amplifier module in a SOT388C package. The module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT388C

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

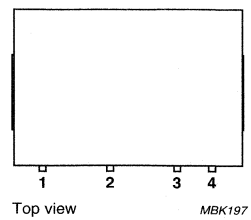


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S, Z_L (Ω)
Pulsed; δ = 1 : 8	890 to 915	3.5	≤2.2	≥3 typ. 3.5	≥35	typ. 47	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	V_C < 0.2 V; no RF	–	7	V
		V_C ≥ 0.2 V	–	5	V
V_C	DC control voltage		–	3	V
P_D	input drive power		–	5	mW
P_L	load power		–	3.8	W
T_{stg}	storage temperature		−40	+100	°C
T_{mb}	operating mounting base temperature		−30	+100	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

CHARACTERISTICS

$Z_S = Z_L = 50\ \Omega$; $P_D = 1$ mW; $V_S = 3.5$ V; $V_C \leq 2.2$ V; f = 890 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.2$ V	–	–	10	μA
I_{CM}	peak control current	adjust V_C for $P_L = 2.5$ W	–	–	3	mA
P_L	load power	$V_C = 2.2$ V	3	3.5	–	W
G_p	power gain	adjust V_C for $P_L = 2.5$ W	35	–	–	dB
η	efficiency	adjust V_C for $P_L = 2.5$ W	–	44	–	%
H_2	second harmonic	adjust V_C for $P_L = 2.5$ W	–	–	–35	dBc
H_3	third harmonic	adjust V_C for $P_L = 2.5$ W	–	–	–33	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 2.5$ W	–	1.8 : 1	3 : 1	
	stability	$V_S = 3$ to 5 V; $P_D = -2$ to +5 dBm; $V_C = 0$ to 2.2 V; $P_L \leq 3$ W; VSWR ≤ 12 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C = 0.2$ V	–	–45	–36	dBm
P_n	noise power	$P_L = 2.5$ W; bandwidth = 30 kHz; 10 MHz above transmission band	–	–82	–80	dBm
	AM/PM conversion	$P_D = -2$ to +5 dBm; $P_L = 6$ to 34 dBm	–	–	3	deg/dB
	AM/AM conversion	P_D with 3% AM; f = 100 kHz; $P_L = 6$ to 34 dBm	–	–	12	%
t_r	carrier rise time	$P_L = 6$ to 34 dBm; time to settle within –0.5 dB of final P_L	–	1.5	2	μs
t_f	carrier fall time	$P_L = 6$ to 34 dBm; time to settle within –0.5 dB of final P_L	–	1.5	2	μs
	ruggedness	$V_S = 5$ V; adjust V_C for $P_L = 3$ W; VSWR ≤ 12 : 1 through all phases	no degradation			

Dual N-channel enhancement mode MOS transistor BSH301

FEATURES

- 40 mΩ on-state resistance at 2.5 V gate drive
- R_{DSon} rating down to 1.8 V
- ESD gate protection.

APPLICATIONS

- Li-Ion safety switch
- Power management.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic TSSOP8 package.

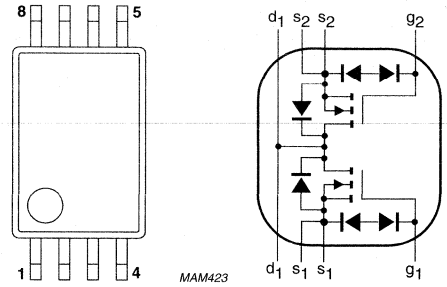


Fig.1 Simplified outline (SOT530) and symbol.

PINNING SOT530 (TSSOP8)

PIN	SYMBOL	DESCRIPTION
1	d1	drain 1
2	s1	source 1
3	s1	source 1
4	g1	gate 1
5	g2	gate 2
6	s2	source 2
7	s2	source 2
8	d1	drain 1

CAUTION
The device is supplied in an antistatic package. The gate inputs must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_S = 80 °C; note 1	–	5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 3.5 A	–	0.04	Ω
P_{tot}	total power dissipation	T_S = 80 °C	–	1.75	W

Note

1. T_S is the temperature at the soldering of the drain lead.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	20	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_S = 80 °C; note 1	–	5	A
I_{DM}	peak drain current	note 2	–	20	A
P_{tot}	total power dissipation	T_S = 80 °C; note 3	–	1.75	W
		T_{amb} = 25 °C; note 4	–	1.85	W
		T_{amb} = 25 °C; note 5	–	0.95	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_S = 80 °C	–	1.75	A
I_{SM}	peak pulsed source current	note 2	–	7	A

Notes

1. T_S is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 °C/W.
5. Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 °C/W.

GSM 4 W power amplifier CGY2013G

FEATURES

- Power Amplifier (PA) overall efficiency 52%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Low output noise floor of PA < −130 dBm/Hz in GSM RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCF5077
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2013G is a GSM class 4 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply.

The PA requires only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.6	–	V
I_{DD}	positive peak supply current	–	2.4	–	A
$P_{o(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

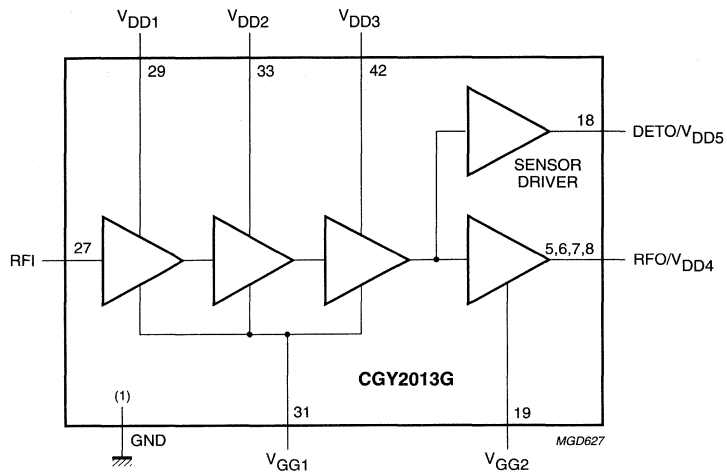
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2013G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 4, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 4	ground
RFO/V_{DD4}	5 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

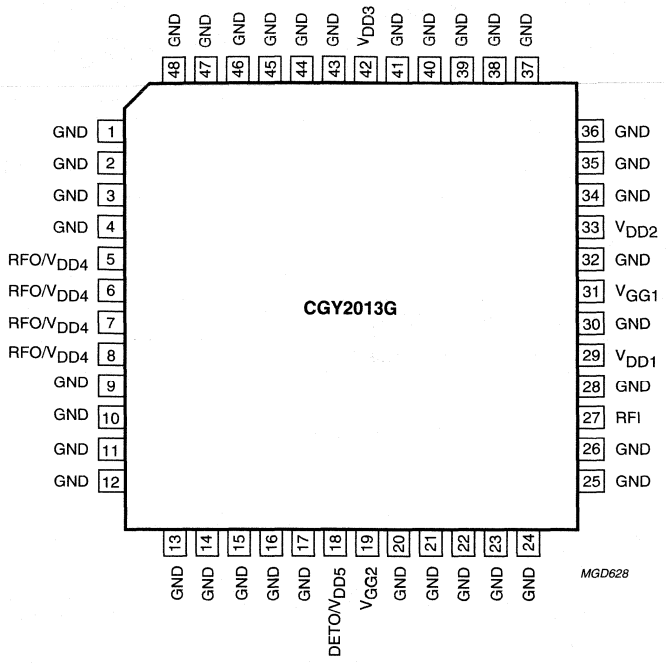


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2013G is designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *"ETS 300 577 specification"*, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

The device is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	−10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	25	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 3.6 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	3.6	5.5	V
I_{DD}	positive peak supply current		–	2.4	3.0	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	−1.8	–	V
V_{GG2}	negative supply voltage	note 1	–	−1.8	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

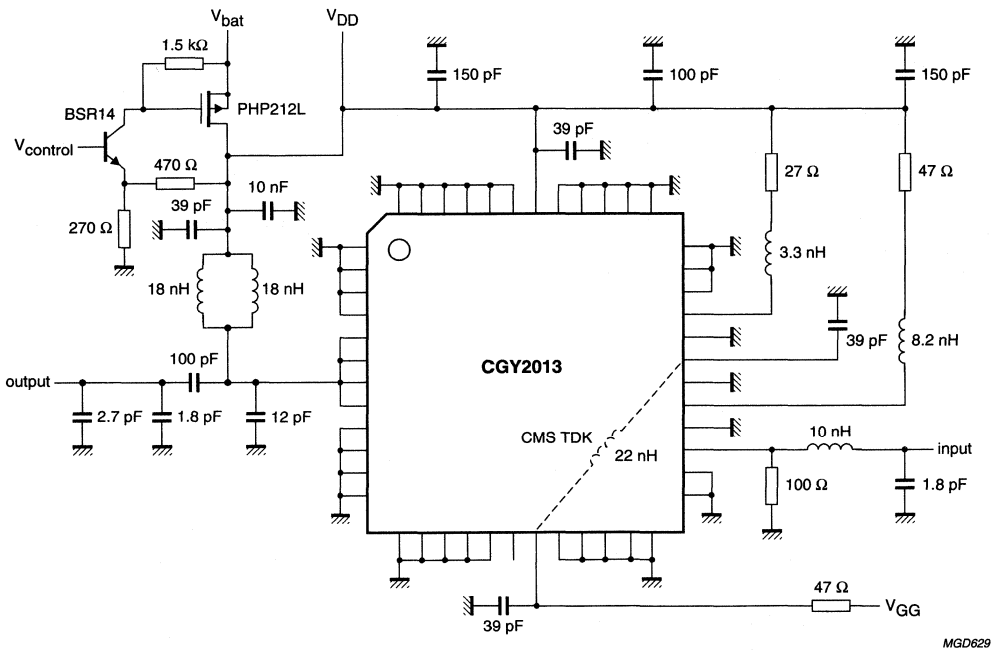
V_{DD} = 3.6 V; T_{amb} = 25 °C; V_{GG1} = V_{GG2} = −1.8 V; measured on Philips demoboard.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		−2	–	+2	dBm
f_{RF}	RF frequency range		880	–	915	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 3.6 V	33.5	35.5	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 3 V	32	–	–	dBm
η	efficiency	V_{DD} = 3.6 V	42	52	–	%
$P_{o(min)}$	minimum output power	V_{DD} < 0.1 V	–	−20	−15	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 to 935 MHz at $P_{o(max)}$	–	–	−117	dBm/Hz
		f_{RF} = 935 to 960 MHz at $P_{o(max)}$	–	–	−125	dBm/Hz
H2	2nd harmonic level		–	–	−35	dBc
H3	3rd harmonic level		–	–	−35	dBc
Stab	stability	note 1	–	–	−70	dBc

Note

1. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION



All SMD size components are 0603.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).

DCS/PCS 2 W power amplifier CGY2021G

FEATURES

- Power Amplifier (PA) overall efficiency 50% (DCS)
- 34 dB gain
- 0 dBm input power
- Gain control range >50 dB
- Integrated power sensor driver
- Low output noise floor of PA <–121 dBm/Hz in DCS/PCS RX band
- Wide operating temperature range –20 to +85 °C
- LQFP 48-pin package
- Compatible with power ramping controller PCA5077 and GaAs PA power modulator UBA1710.

APPLICATIONS

- Hand-held transceivers for DCS/PCS applications (DCS: 1710 to 1785 MHz and PCS: 1850 to 1910 MHz)
- 1800 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2021G is a DCS/PCS class 1 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 4.8 V battery supply.

The chip also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a simple low-pass filter to comply with the DCS/PCS transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.5	–	V
I_{DD}	positive peak supply current	–	1.4	–	A
$P_{o(max)}$	maximum output power	–	34	–	dBm
T_{amb}	operating ambient temperature	–20	–	+85	°C

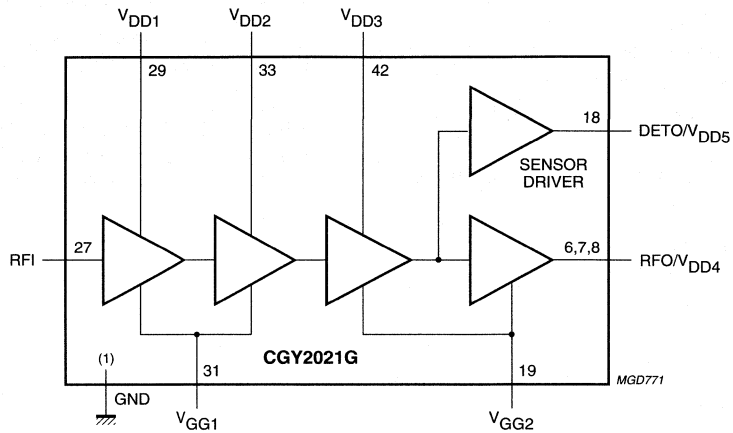
Note

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2021G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	PA output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	third and fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	PA input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first and second stage negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

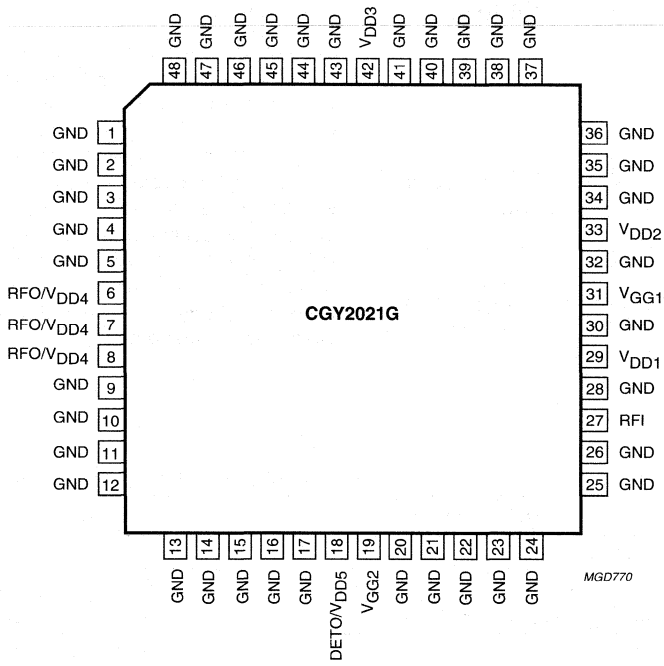


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2021G is designed to meet the European Telecommunications Standards Institute (ETSI) DCS documents, the ETS 300 577 specification, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

This amplifier is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The Power Amplifier (PA) consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress of the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers an output signal at the DETO pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage. An impedance mismatch at the PA output therefore does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently, the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.3	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	45	K/W

Note

1. This thermal resistance is a typical value and is measured under DCS/PCS pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; peak current values during burst; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		–	4.5	–	V
I_{DD}	positive peak supply current		–	1.4	–	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	−1.6	–	V
V_{GG2}	negative supply voltage	note 1	–	−1.6	–	V
I_{GG1} + I_{GG2}	negative peak supply current		–	–	2	mA

Note

1. The negative bias V_{GG} must be applied 10 µs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

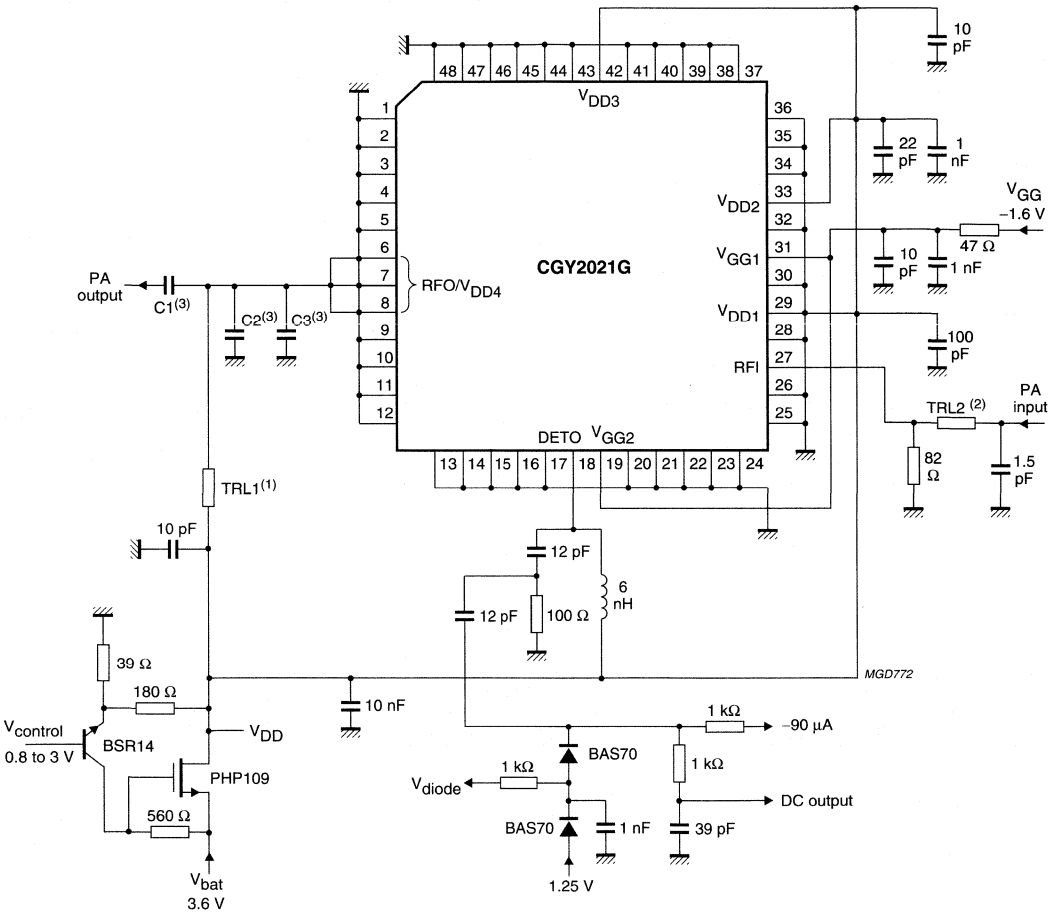
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.
Measured and guaranteed on CGY2021G evaluation board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		–2	–	+2	dBm
S_{11}	input return loss	50 Ω source; note 1	–	–	–10	dB
f_{RF}	RF frequency range	DCS	1710	–	1785	MHz
		PCS	1850	–	1910	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	33	34	–	dBm
		T_{amb} = –20 to +85 °C; V_{DD} = 4.2 V	31	–	–	dBm
η	efficiency	DCS; at $P_{o(max)}$	40	50	–	%
		PCS; at $P_{o(max)}$	–	47	–	%
R_S	optimum series load resistance		–	6	–	Ω
C_S	optimum series load capacitance		–	11	–	pF
$P_{o(off)}$	isolation	PA OFF; P_i = 0 dBm	–	–50	–	dBm
N_{RX}	output noise in RX band		–	–	–121	dBm/Hz
H2	2nd harmonic level		–	–40	–	dBc
H3	3rd harmonic level		–	–35	–	dBc
Stab	stability	note 2	–	–	–50	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	–25	–	dBc

Notes

1. Including the 82 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

APPLICATION INFORMATION



All capacitors are type: SMD0603.
Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.
(1) TRL1: width = 0.3 mm; length = 16 mm.
(2) TRL2: width = 0.5 mm; length = 10 mm.
(3) the component values are:

SYSTEM	C1 (pF)	C2 (pF)	C3 (pF)
DCS	2.2	1.8	2.2
PCS	1.5	1.8	1.2

Fig.3 Evaluation board schematic.

DECT 500 mW power amplifier CGY2030M

FEATURES

- Power Amplifier (PA) overall efficiency 40%
- 27 dB gain
- 0 dBm input power
- Operation possible without negative supply
- Wide operating temperature range –30 to +85 °C
- SSOP16 package.

GENERAL DESCRIPTION

The CGY2030M is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. When power control is not required, it can be operated without negative supply voltage.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS).

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	positive peak supply current	–	400	–	mA
P_o	output power	–	27	–	dBm
T_{amb}	operating ambient temperature	–30	–	+85	°C

Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2030M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

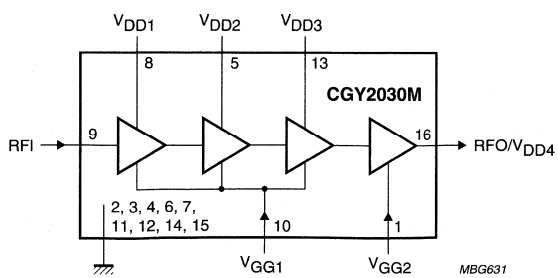


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{GG2}	1	fourth stage negative gate supply voltage
GND	2 to 4	ground
V_{DD2}	5	second stage supply voltage
GND	6 and 7	ground
V_{DD1}	8	first stage supply voltage
RFI	9	PA input
V_{GG1}	10	first second and third stages negative gate supply voltage
GND	11 and 12	ground
V_{DD3}	13	third stage supply voltage
GND	14 and 15	ground
RFO/V_{DD4}	16	PA output and fourth stage supply voltage

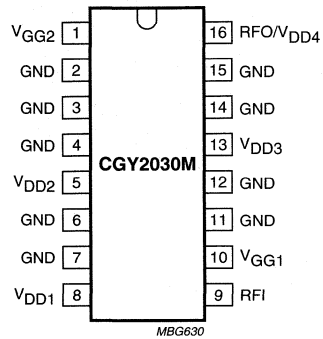


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2030M is a 4-stage GaAs MESFET power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of an external PNP series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a maximum duty factor of 25%.

Biasing

Two modes of operation are possible:

- Mode 1
- Mode 2.

MODE 1

In the first mode, the pins V_{GG1} and V_{GG2} are simply connected together to the ground via resistors (10 kΩ in the evaluation board; see Fig.4). The amplifier biases itself internally to a negative voltage by action of the incoming RF signal. In this mode, power control cannot be achieved by varying the amplifier supply voltage; therefore it is suitable only for applications where power control is not required such as DECT.

MODE 2

If a negative bias is available, a second mode of operation is possible, in which the amplifier is biased by providing adequate negative voltages at pins V_{GG1} and V_{GG2}. In this mode, the amplifier internal bias does not depend on the incoming RF level, nor on the drain voltage, so that power control is possible by variation of the supply voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		–	–	5.2	V
$V_{DD} - V_{GG}$	voltage difference between supply voltage and gate bias voltage	no input signal	–	–	8	V
$T_{j(max)}$	maximum operating junction temperature		–	–	150	°C
P_{tot}	total power dissipation		–	–	400	mW
T_{stg}	IC storage temperature		–55	–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	145	K/W

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

DC CHARACTERISTICS

V_{DD} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2} and V_{DD1}						
V_{DD}	positive supply voltage		2.6	3.2	4.2	V
I_{DD}	positive peak supply current		–	400	500	mA
Pins V_{GG1} and V_{GG2}; in mode 2						
V_{GG1}	bias voltage for input stages	note 1	–	–1.2	–	V
V_{GG2}	bias voltage for output stage	note 1	–	–2.0	–	V
$I_{GG(tot)}$	total gate peak current	note 2	–1	–	+1	mA

Notes

1. Negative voltages V_{GG1} and V_{GG2} must be applied before supply voltage V_{DD}.
2. Due to non linear effects at high power levels, the gate current can be either negative or positive.

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 25%; 50 Ω impedance system; measured and guaranteed on CGY2030M evaluation board (see Fig.4).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power	note 1	−3	–	+5	dBm
δ	duty factor		–	–	25	%
f_{RF}	operating frequency		–	1900	–	MHz
Measured in mode 1; without negative biasing; V_{GG1} and V_{GG2} connected to ground						
P_o	output power		26	27	28.5	dBm
η	efficiency		–	40	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	−40	–	dBm
H2, H3	second and third harmonics level		–	−35	–	dBc
Stab	stability (spurious levels)	note 2	–	−60	–	dBc
Measured in mode 2; with negative biasing at pins V_{GG1} and V_{GG2}						
P_o	output power		25.5	26.5	28	dBm
η	efficiency		–	35	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	−50	–	dBm

Notes

1. Self biasing guaranteed in mode 1 at minimum input power (−3 dBm) and minimum supply voltage V_{DD} (2.6 V).
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

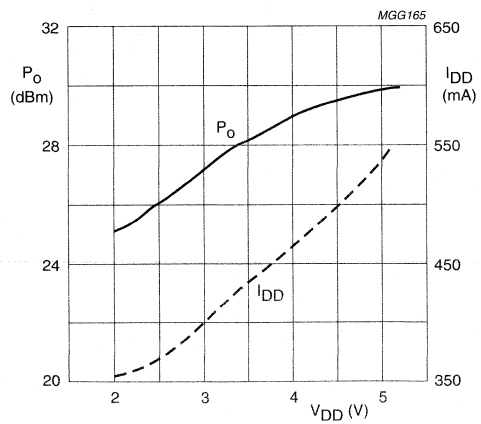
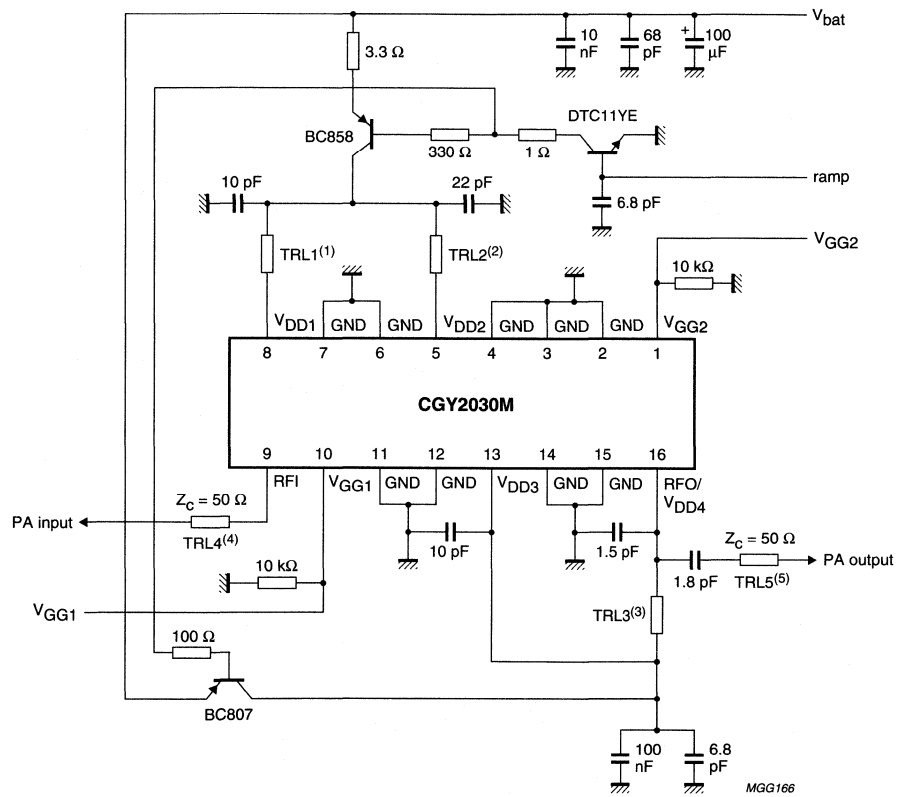


Fig.3 Typical power and current characteristics in mode 1.

APPLICATION INFORMATION

The CGY2030M is operated and tested in accordance with the circuit diagram shown in Fig.4. Supply voltage switching is achieved by two bipolar PNP transistors. One transistor switches the first and second stages and the other switches the third and fourth stages.

By switching on the last amplifier stages with some delay compared to the first stages, it is possible to get the last stages already self-biased before their supply voltage has reached its steady state value. This enables smooth power up-ramping without any power overshoot. A simpler drain switching circuit can be used if the amplifier is operated with negative biasing of the pins V_{GG1} and V_{GG2}.



Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.

(1) TRL1: width = 500 µm; length = 11200 µm.
(2) TRL2: width = 500 µm; length = 7770 µm.
(3) TRL3: width = 300 µm; length = 15450 µm.
(4) TRL4: width = 1600 µm; length = 12000 µm.
(5) TRL5: width = 1600 µm; length = 11000 µm.

Fig.4 Evaluation board schematic.

DECT 500 mW power amplifier CGY2032TS

FEATURES

- Power Amplifier (PA) overall efficiency 50%
- 28 dBm saturated output power at 3.2 V
- 0 dBm input power
- 40 dB linear gain
- Operation without negative supply
- Wide operating temperature range −30 to +85 °C
- SSOP16 package.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS and PCS).

GENERAL DESCRIPTION

The CGY2032TS is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate from 3.6 V battery supply. No negative supply voltage is required for operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	positive peak supply current	–	350	–	mA
P_o	output power	–	28	–	dBm
T_{amb}	operating ambient temperature	−30	–	+85	°C

Note

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2032TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

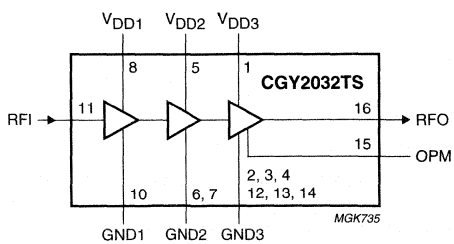


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD3}	1	third stage supply voltage
GND3	2 to 4 and 12 to 14	third stage ground
V_{DD2}	5	second stage supply voltage
GND2	6 and 7	second stage ground
V_{DD1}	8	first stage supply voltage
n.c.	9	not connected
GND1	10	first stage ground
RFI	11	PA input
OPM	15	output pre-matching
RFO	16	PA output

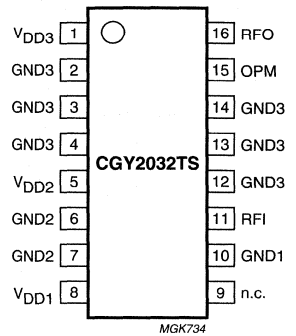


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2032TS is a 3-stage GaAs power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of a single external PNP or PMOS series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a duty factor of 50% and can work up to 100% with good thermal performance PCBs.

Biasing

Internal biasing is provided inside the amplifier for class AB operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	operating supply voltage	note 1	–	5.2	V
$T_{j(max)}$	maximum operating junction temperature		–	150	°C
P_{tot}	total power dissipation	note 2	–	450	mW
P_i	input power		–	15	dBm
T_{stg}	storage temperature		−55	+125	°C

Notes

1. On Philips evaluation board.
2. On Philips evaluation board, P_{tot} maximum value is 800 mW.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	145	K/W

Note

1. On Philips evaluation board, $R_{th(j-a)}$ value is typically 80 K/W.

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

DC CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{DD1}, V_{DD2} and V_{DD3}						
V_{DD}	positive supply voltage		1.8	3.2	4.2	V
I_{DD}	positive peak supply current	V_{DD} = 3.2 V	–	–	800	mA

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 50%; 50 Ω impedance system; measured and guaranteed on CGY2032TS evaluation board (see Fig.5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power		–5	0	+5	dBm
δ	duty factor		–	50	100	%
P_o	output power	V_{DD} = 3.2 V	26.5	28	29	dBm
I_{DD}	total drain current	V_{DD} = 3.2 V	–	–	500	mA
η	efficiency		–	55	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–40	–35	dBm
H2	second harmonic level		–	–	–30	dBc
H3	third harmonic level		–	–	–35	dBc
Stab	stability (spurious levels)	note 1	–	–60	–	dBc

Note

1. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

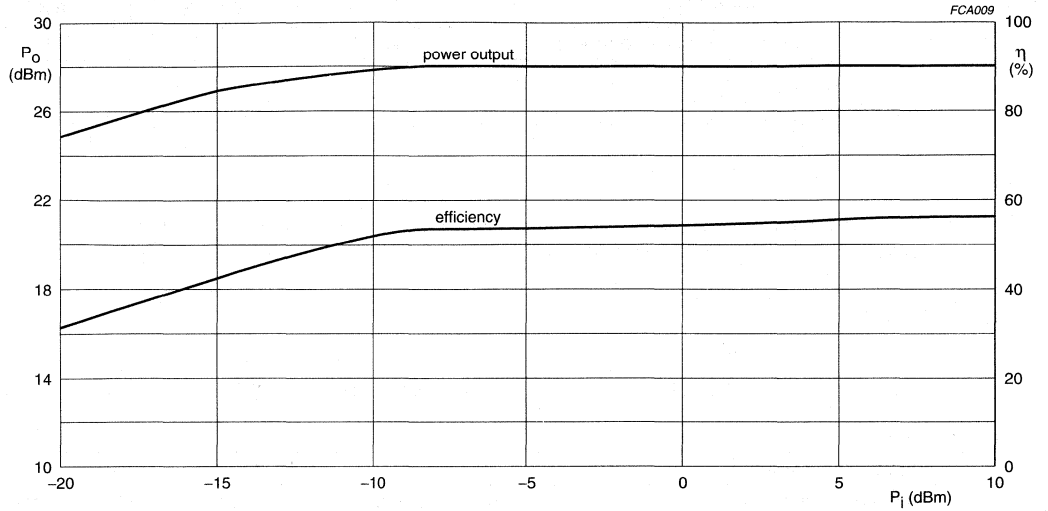


Fig.3 Typical output power and efficiency versus input power - V_{DD} = 3.2 V.

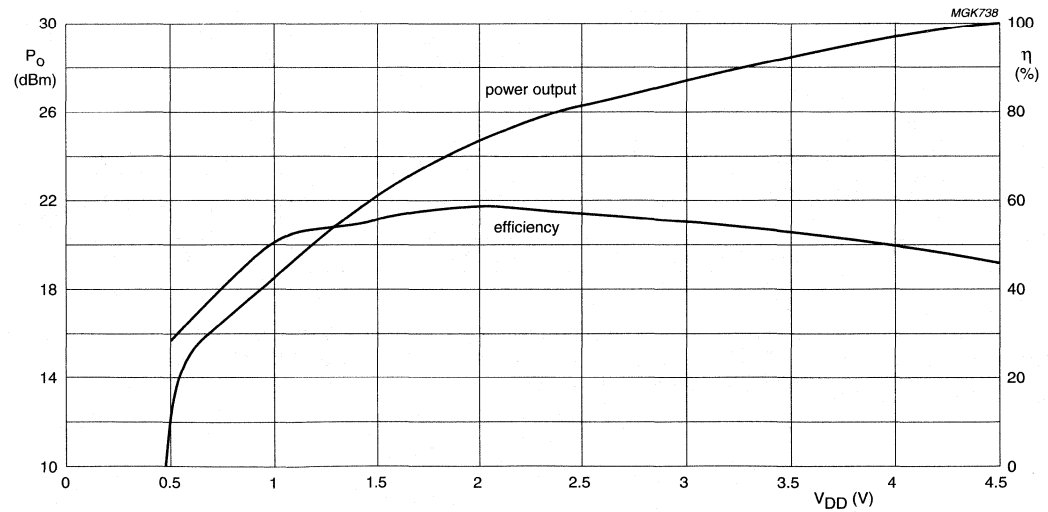
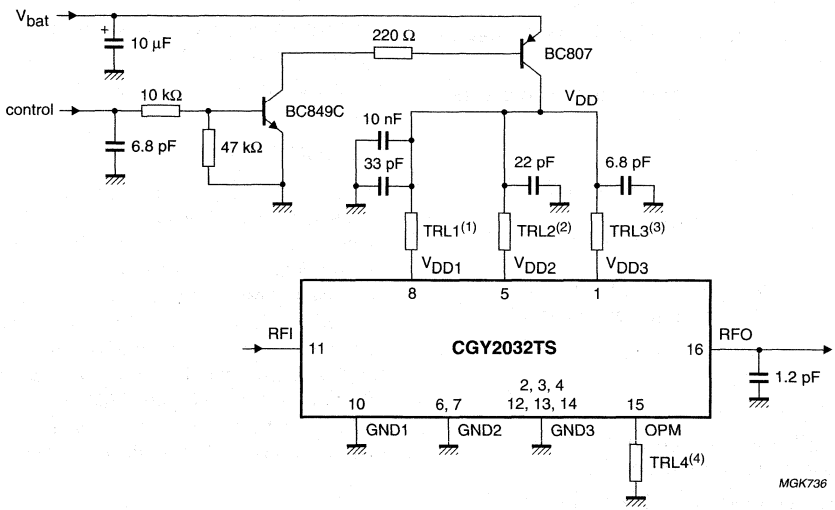


Fig.4 Typical output power and efficiency versus supply voltage - pin = 0 dB.

APPLICATION INFORMATION

The CGY2032TS is operated and tested in accordance with the circuit diagram shown in Fig.5. Supply voltage switching is achieved by a single bipolar PNP transistor.



Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.

(1) TRL1: width = 500 µm; length = 10 mm.

(2) TRL2: width = 500 µm; length = 3000 µm.

(3) TRL3: width = 500 µm; length = 7 mm.

(4) TRL4: adjusted for optimum matching; width = 500 µm; length = 1 to 3 mm.

Fig.5 Evaluation board circuit diagram.

Universal LCD driver for low multiplex rates

OM4085

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.0 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple OM4085 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The OM4085 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The OM4085 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4085T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

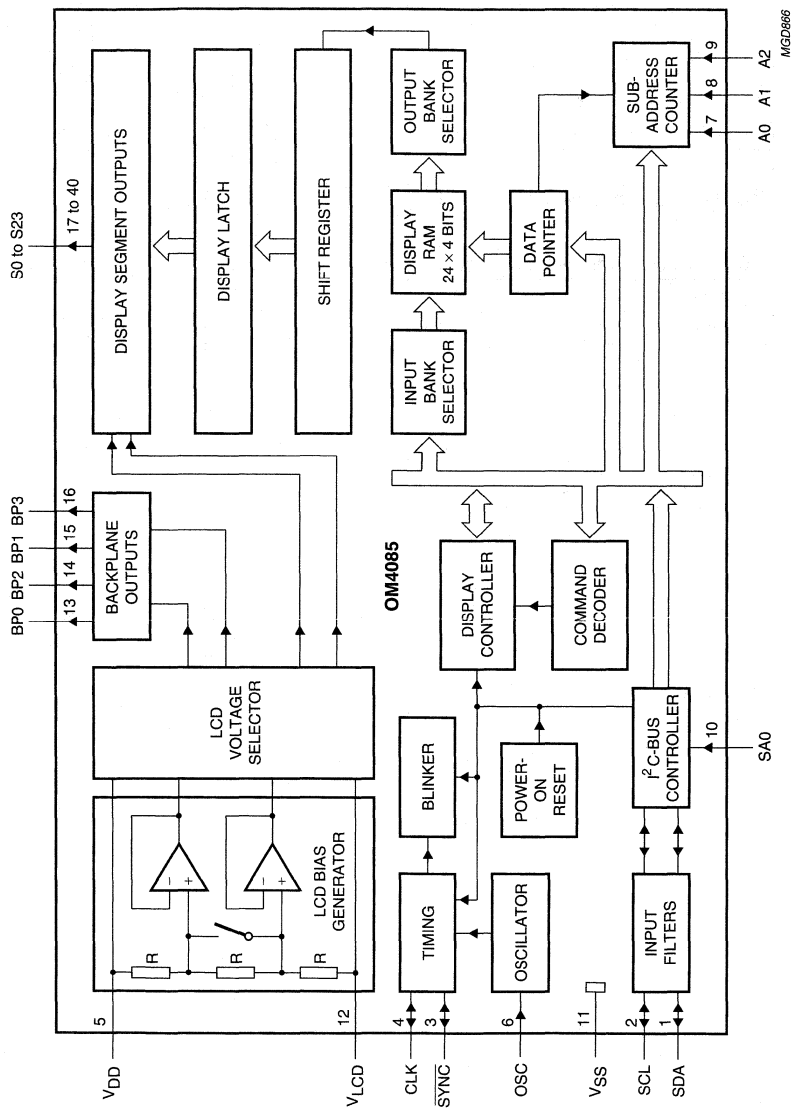


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

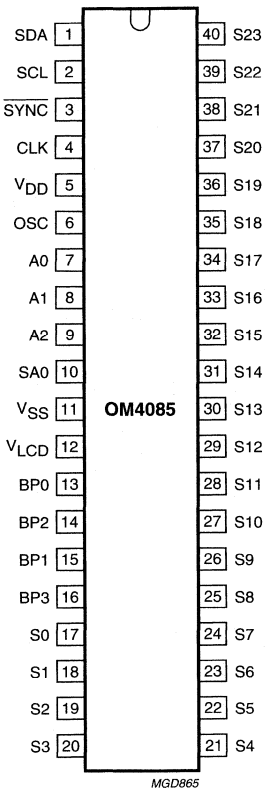
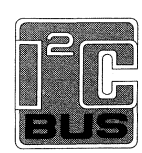


Fig.2 Pin configuration.

CONTENTS



1 FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 56-lead VSO or 64-lead QFP package
- 256 bytes on-chip RAM Data Memory
- 6 kbytes on-chip ROM Program Memory for P83CL580
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- Five 8-bit ports; 40 I/O lines
- Three 16-bit Timers/Event counters
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector, nested interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Analog-to-digital converter (ADC) with Power-down mode; 4 input channels and 8-bit ADC
- Pulse Width Modulated (PWM) output (8-bit resolution)
- Watchdog Timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: 0 to 12 MHz. For ADC operation minimum 250 kHz at 2.7 V
- Supply voltage: 2.5 to 6.0 V
- Very low current consumption: typically 4.5 mA at 2.5 V and 8 MHz
- Operating ambient temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

The P80CL580; P83CL580 (hereafter generally referred to as P8xCL580) is manufactured in an advanced CMOS technology. The P8xCL580 has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device operates over a wide range of supply voltages and has low power consumption; there are two software selectable modes for power reduction: Idle and Power-down. For emulation purposes, the P85CL580 (piggy-back version) with 256 bytes of RAM is recommended.

This data sheet details the specific properties of the P80CL580; P83CL580. For details of the 80C51 core and the I²C-bus see *"Data Handbook IC20"*.

2.1 ROMless version: P80CL580

The P80CL580 is the ROMless version of the P83CL580. The mask options on the P80CL580 are fixed as follows:

- All ports have option '1S' (standard port, HIGH after reset), except ports P1.6 and P1.7 which have option '2S' (open-drain, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: off.

3 APPLICATIONS

The P8xCL580 is an 8-bit general purpose microcontroller especially suited for cordless telephone and mobile communication applications. The P8xCL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

4 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
P8xCL580HFT	VSO56	plastic very small outline package; 56 leads	SOT190-1
P8xCL580HFH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT319-2

Note

1. 'x' = 0 or 3. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

5 BLOCK DIAGRAM

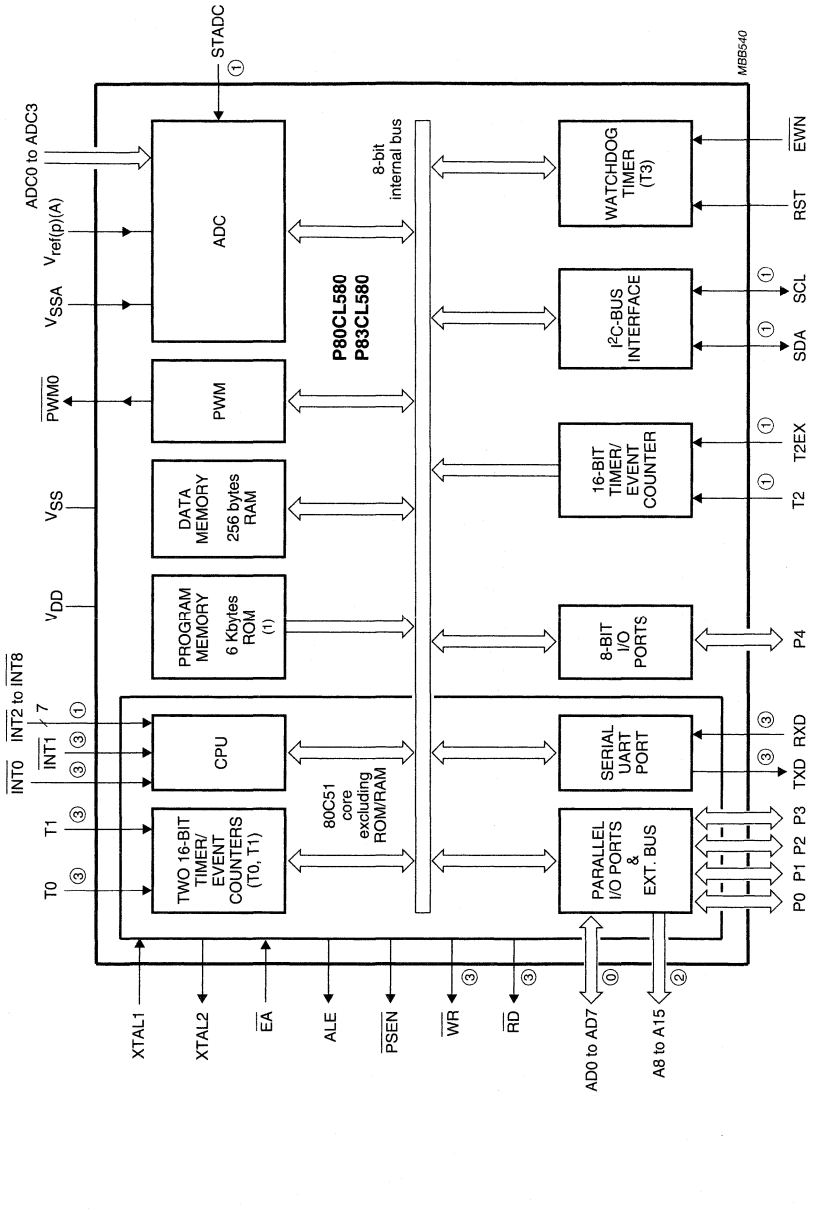


Fig.1 Block diagram.

(1) Not available in the **P80CL580**.

6 FUNCTIONAL DIAGRAM

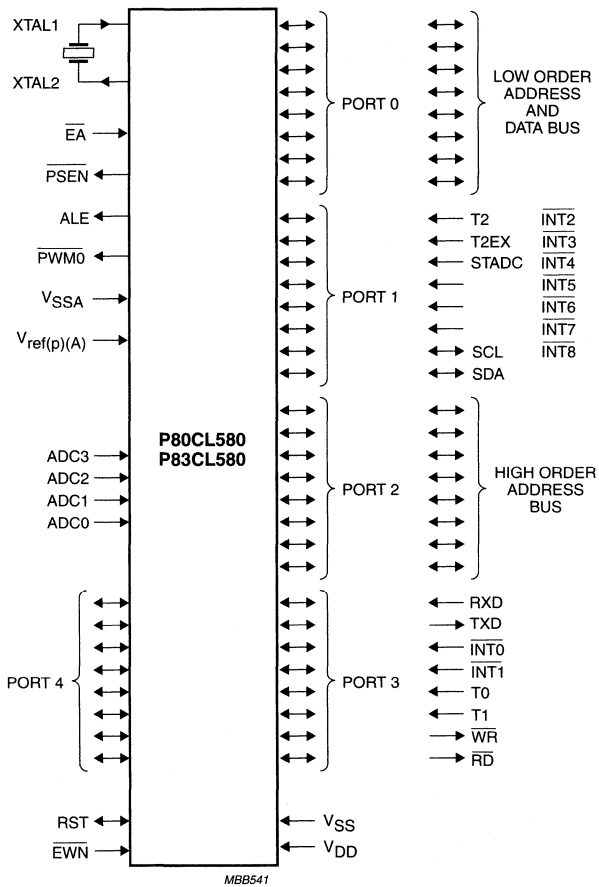


Fig.2 Functional diagram.

7 PINNING INFORMATION

7.1 Pinning

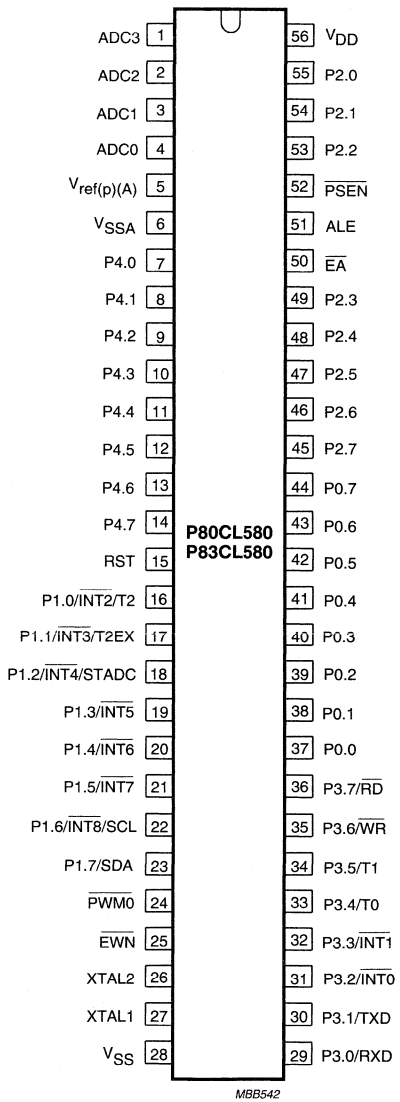


Fig.3 Pin configuration for VSO56 package.

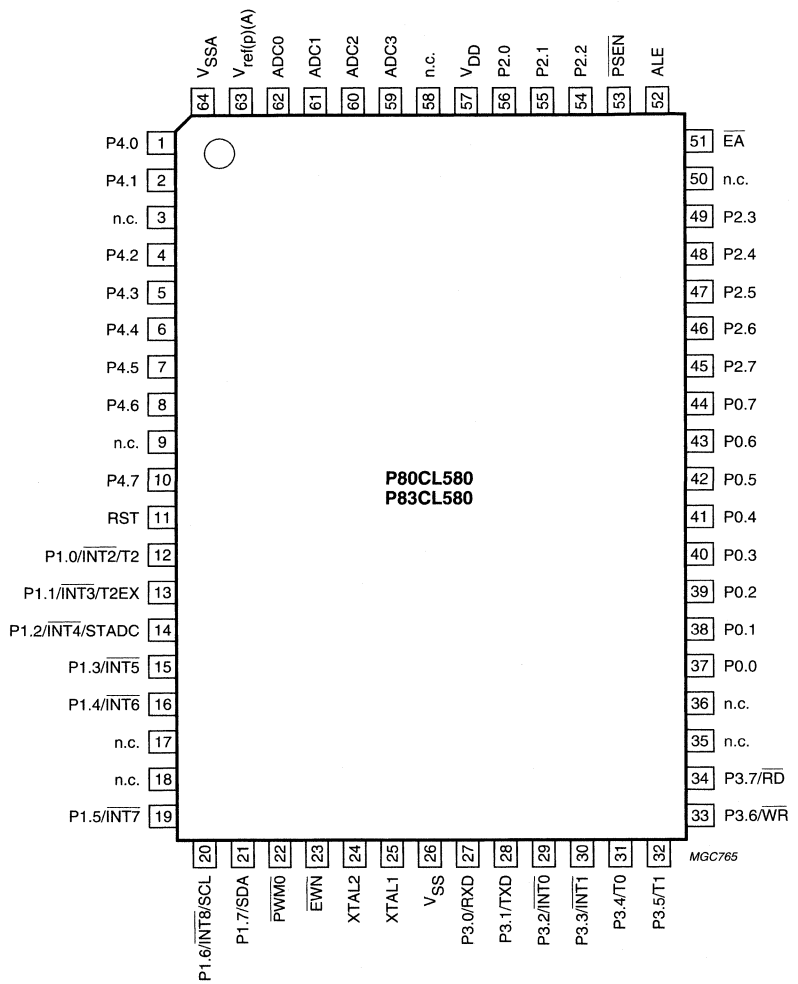


Fig.4 Pin configuration for QFP64 package.

7.2 Pin description

Table 1 Pin description for VSO56 (SOT190-1) and QFP64 (SOT319-2)
For more extensive description of the port pins see Chapter 10 "I/O facilities".

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
ADC3 to ADC0	1 to 4	59 to 62	4 input channels to the ADC.
$V_{ref(p)(A)}$	5	63	Positive potential of analog-to-digital conversion reference resistor.
V_{SSA}	6	64	Analog part ground.
P4.0 to P4.7	7 to 14	1, 2, 4 to 8, 10	**Port 4**: 8-bit bidirectional I/O port. (P4.0 to P4.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 4 pins that are externally pulled LOW will source current (I_{IL}, see Chapter 23) due to the internal pull-ups. Port 4 output buffers can sink/source 4 LS TTL loads.
RST	15	11	**Reset**: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P1.0/$\overline{INT2}$/T2	16	12	• **Port 1:** 8-bit bidirectional I/O port (P1.0 to P1.7). Same characteristics as Port 4, but note that P1.6 and P1.7 are open-drain only. • **Alternative functions:** – INT2 to INT8 are external interrupt inputs – STADC is the external trigger of the analog-to-digital converter – T2 and T2EX are the Timer/event counter 2 inputs – SCL and SDA are the I²C-bus clock and data lines.
P1.1/$\overline{INT3}$/T2EX	17	13	
P1.2/$\overline{INT4}$/STADC	18	14	
P1.3/$\overline{INT5}$	19	15	
P1.4/$\overline{INT6}$	20	16	
P1.5/$\overline{INT7}$	21	19	
P1.6/$\overline{INT8}$/SCL	22	20	
P1.7/SDA	23	21	
$\overline{PWM0}$	24	22	**Pulse Width Modulation output 0**.
$\overline{EWN}$	25	23	**Enable Watchdog Timer**: enable for Watchdog Timer and enable Power-down mode.
XTAL2	26	24	**Crystal oscillator output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	27	25	**Crystal oscillator input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V_{SS}	28	26	Ground: circuit ground potential.
P3.0/RXD	29	27	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 4 • **Alternative functions:** – RXD is the UART serial data input (asynchronous) or data input/output (synchronous) – TXD is the UART serial data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ and $\overline{INT1}$ are external interrupts 0 and 1 – T0 and T1 are external inputs for timers 0 and 1.
P3.1/TXD	30	28	
P3.2/$\overline{INT0}$	31	29	
P3.3/$\overline{INT1}$	32	30	
P3.4/T0	33	31	
P3.5/T1	34	32	
P3.6/$\overline{WR}$	35	33	
P3.7/$\overline{RD}$	36	34	

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
P0.0 to P0.7	37 to 44	37 to 44	• **Port 0**: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. • **Low-order addressing**: Port 0 is also the multiplexed low-order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
P2.0 to P2.7	55 to 53, 49 to 45	56 to 54, 49 to 45	• **Port 2**: 8-bit bidirectional I/O port with internal pull-ups. Same characteristics as Port 4. • **High-order addressing**: Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
$\overline{EA}$	50	51	**External Access**. When $\overline{EA}$ is held HIGH the CPU executes out of internal Program Memory (unless the program counter exceeds 17FFH). Holding $\overline{EA}$ LOW forces the CPU to execute out of external memory regardless of the value of the Program Counter.
ALE	51	52	**Address Latch Enable**. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $1/6 \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
$\overline{PSEN}$	52	53	**Program Store Enable**. Output read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{PSEN}$ activations are skipped.
V_{DD}	56	57	Power supply.
n.c.	–	3, 9, 17, 18, 35, 36, 50 and 58	Not connected.

8 FUNCTIONAL DESCRIPTION OVERVIEW

This chapter gives a brief overview of the device. The detailed functional description is in the following chapters:

Chapter 9 "Memory organization"

Chapter 10 "I/O facilities"

Chapter 11 "Timers/event counters"

Chapter 12 "Pulse Width Modulated output"

Chapter 13 "Analog-to-digital converter (ADC)"

Chapter 14 "Reduced power modes"

Chapter 15 "I²C-bus serial I/O"

Chapter 16 "Standard serial interface SIO0: UART"

Chapter 17 "Interrupt system"

Chapter 18 "Oscillator circuitry"

Chapter 19 "Reset".

8.1 General

The P8xCL580 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as cordless telephone and mobile communications, instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of Data Memory.

The P8xCL580 contains a 6 kbytes Program Memory (ROM; P83CL580); a static 256 bytes Data Memory (RAM); 40 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit, 4-channel 8-bit A/D converter, Watchdog Timer and Pulse Width Modulation output.

The device has two software-selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the derivative functions (timers, serial I/O, ADC, PWM) and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, two serial interfaces are provided on-chip:

- A standard UART serial interface, and
- A standard I²C-bus serial interface. The I²C-bus serial interface has byte-oriented master and slave functions allowing communication with the whole family of I²C-bus compatible devices.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P8xCL580 has 6 kbytes of Program Memory (ROM; P83CL580 only) plus 256 bytes of Data Memory (RAM) on board.The device has separate address spaces for Program and Data Memory (see Fig.6). Using Port latches P0 and P2, the P8xCL580 can address up to 128 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

9.1 Program Memory

The P83CL580 contains 6 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 6 kbytes of Program Memory can be implemented in either on-chip ROM or external Program Memory.

If the $\overline{EA}$ pin is tied to V_{DD}, then Program Memory fetches from addresses 0000H to 17FFH are directed to the internal ROM. Fetches from addresses 1800H to FFFFH are directed to external ROM. Program Counter values greater than 17FFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

9.2 Data Memory

The P8xCL580 contains 256 bytes of internal RAM and 40 Special Function Registers (SFRs). Figure 6 shows the internal Data Memory space divided into the lower 128 bytes, the upper 128 bytes, and the SFRs space. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

9.3 Special Function Registers (SFRs)

The upper 128 bytes are the address locations of the SFRs. Figures 7 and 8 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 directly addressable locations in the SFR address space. Bit addressable SFRs are those that end in 000B.

9.4 Addressing

The P8xCL580 has five methods for addressing source operands:

- Register
- Direct
- Register-indirect
- Immediate
- Base-register plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

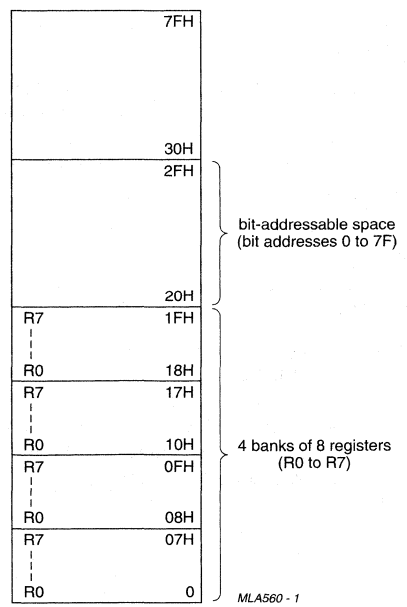


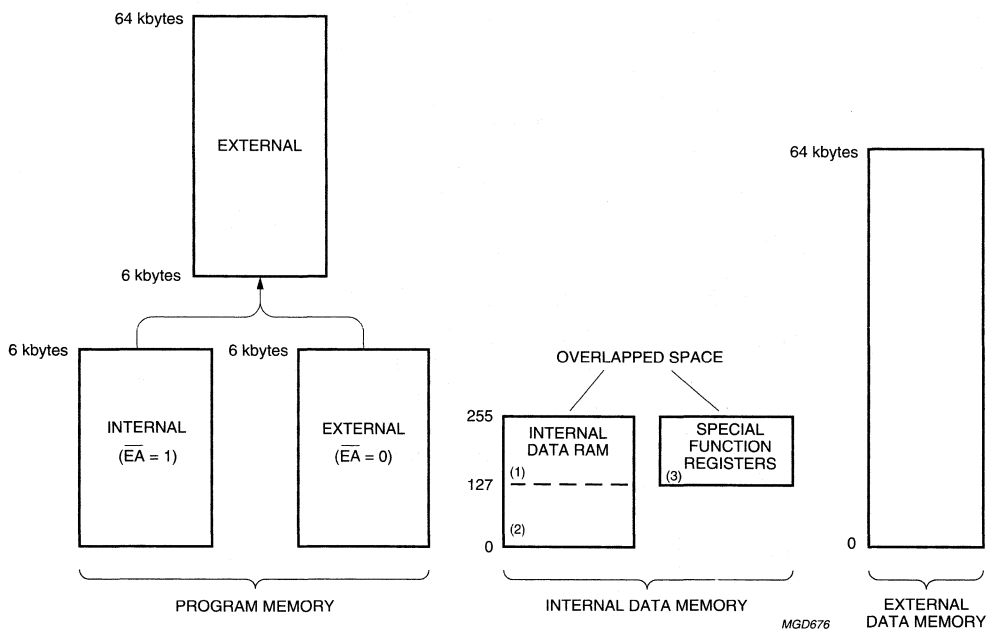
Fig.5 The lower 128 bytes of internal RAM.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or register-indirect
- Lower 128 bytes of internal RAM through direct or register-indirect; upper 128 bytes of internal RAM through direct
- Special Function Registers through direct
- External Data Memory through register-indirect
- Program Memory look-up tables through base-register plus index-register-indirect.

The P8xCL580 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.



(1) Accessible via indirect addressing only.
(2) Accessible via direct and indirect addressing.
(3) Accessible via direct addressing.

Fig.6 Memory map.

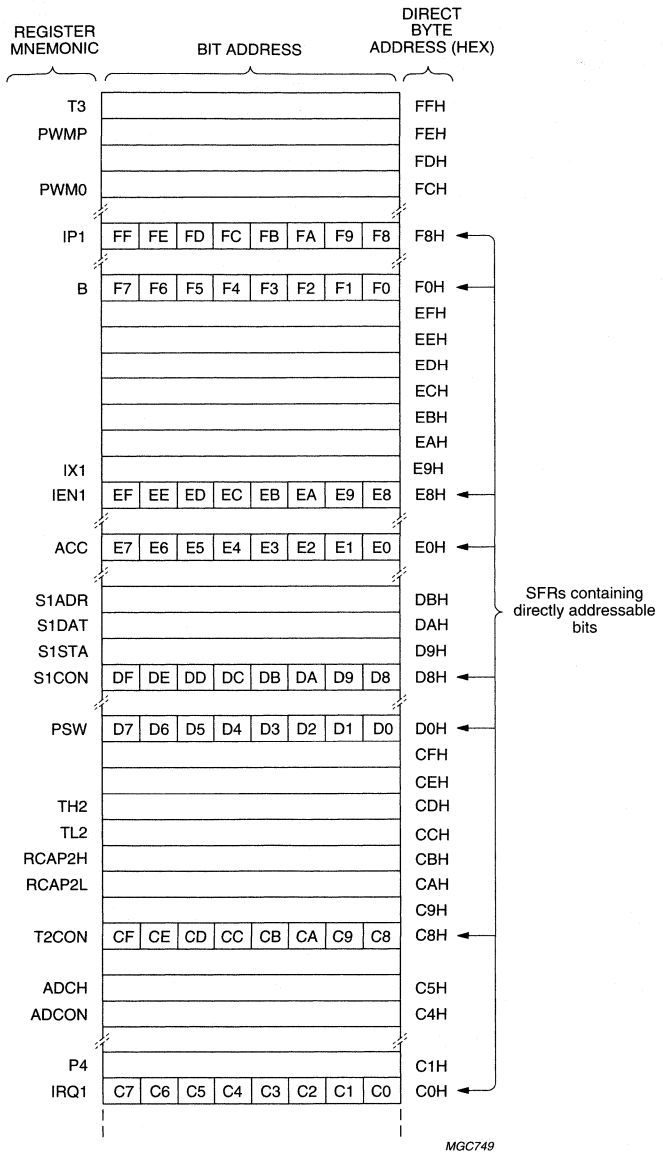


Fig.7 Special Function Register memory map (continued in Fig.8).

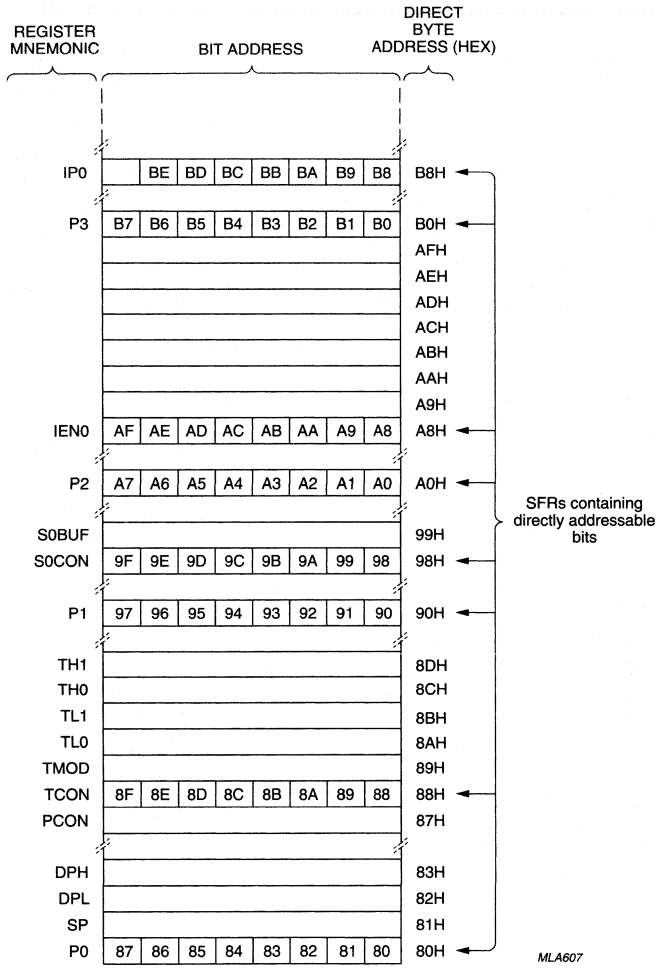


Fig.8 Special Function Register memory map (continued from Fig.7).

10 I/O FACILITIES

10.1 Ports

The P8xCL580 has 40 I/O lines treated as one 8-bit port plus 32 individually addressable bits or as five parallel 8-bit addressable ports.

Port 4 has no alternative functions. To enable a port pin alternative function for Ports 0, 1, 2 and 3, the port bit latch in its SFR must contain a logic 1. The alternative functions are detailed below:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts: $\overline{INT2}$ to $\overline{INT8}$.
- External activation of Timer 2: T2.
- External trigger of the ADC: STADC.
- The I²C-bus interface: SCL and SDA.

Port 2 Provides the high-order address when expanding the device with external Program or Data Memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{INT1}$ and $\overline{INT0}$.
- Counter input: T1 and T0.
- Control signals to read and write to external memories: $\overline{RD}$ and $\overline{WR}$.
- UART input and output: RXD and TXD.

Each port consists of a latch (SFRs P0 to P4), an output driver and input buffer. Ports 1, 2, 3 and 4 have internal pull-ups (except P1.6 and P1.7). Figure 9(a) shows that the strong transistor 'p1' is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter. This inverter and 'p3' form a latch which holds the logic 1. In Port 0 the pull-up 'p1' is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 0 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

10.2 Port options

38 of the 40 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.9.

Option 1 **Standard Port**; quasi-bidirectional I/O with pull-up. The strong booster pull-up 'p1' is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.9(a).

Option 2 **Open-drain**; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; see Fig.9(b).

Option 3 **Push-pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs; see Fig.9(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 External memory accesses

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up 'p1' will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.9(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.9(c).

10.4 SET/RESET options

Individual mask selection of the post-reset state is available with any of the above pins. The selection is made by appending 'S' or 'R' to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

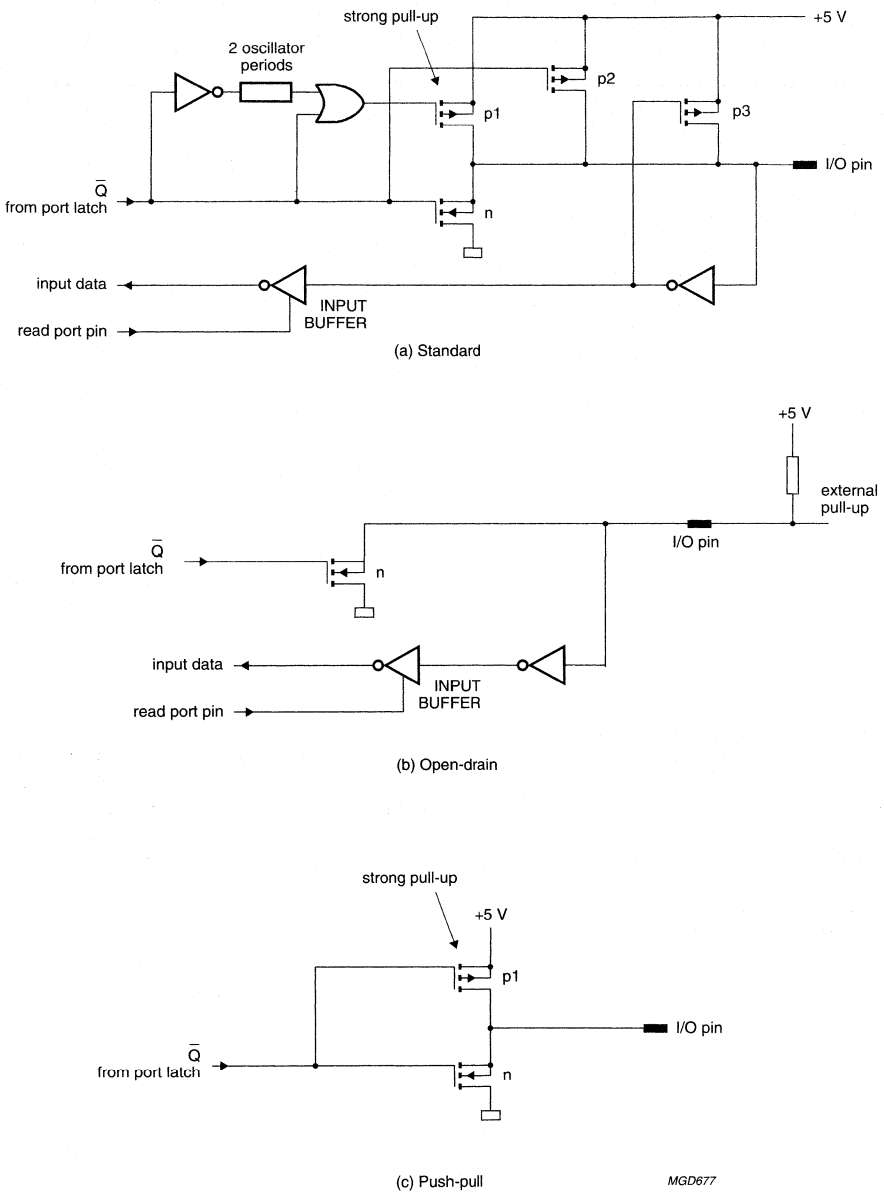


Fig.9 Port configuration options.

11 TIMERS/EVENT COUNTERS

The P8xCL580 contains three 16-bit timer/event counter registers; Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12 \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/24 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

11.2 Timer T2

Timer T2 is a 16-bit timer/counter that can operate (like Timer 0 and 1) either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register; see Tables 2 and 3.

Three operating modes are available Capture, Auto-reload and Baud Rate Generator, which also are selected via the T2CON register; see Table 4.

11.2.1 CAPTURE MODE

Figure 10 shows the Capture mode. Two options in this mode, may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

11.2.2 AUTO-RELOAD MODE

Figure 11 shows the Auto-reload mode. Also two options in this mode are selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

11.2.3 BAUD RATE GENERATOR MODE

The Baud Rate Generator mode is selected when RTCLK = 1. It will be described in conjunction with the serial port (UART); see Section 16.3.2.

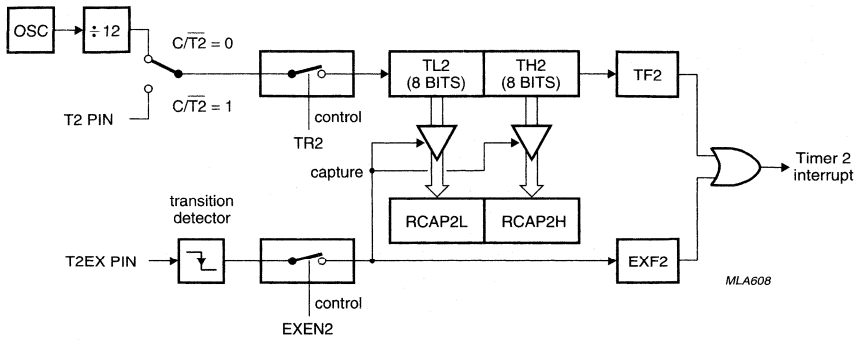


Fig.10 Timer 2 in Capture mode.

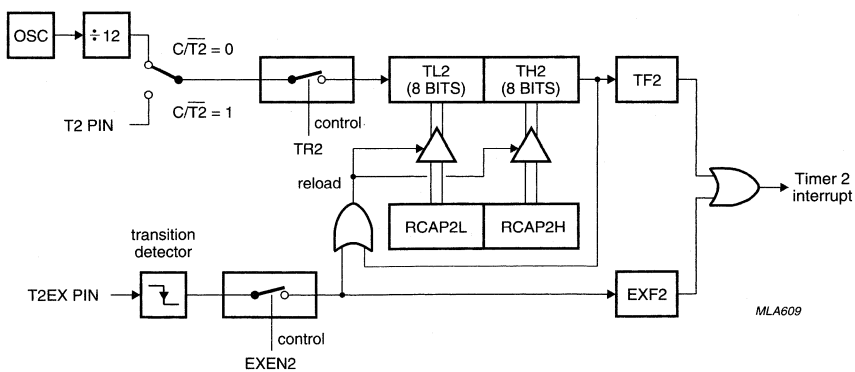


Fig.11 Timer 2 in Auto-Reload mode.

11.3 Timer/Counter 2 Control Register (T2CON)

Table 2 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 3 Description of T2CON bits.

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag**. Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
6	EXF2	**Timer 2 external flag.** Set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	GF2	**General purpose flag** bit.
4	RTCLK	**Receive/transmit clock flag**. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
3	EXEN2	**Timer 2 external enable flag**. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0, causes Timer 2 to ignore events at T2EX.
2	TR2	**Start/stop control for Timer 2**. TR2 = 1 starts the timer.
1	C/$\overline{T2}$	**Timer or counter select for Timer 2**. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $^1/_{12} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge triggered.
0	CP/$\overline{RL2}$	**Capture/Reload flag**. When set, captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 4 Timer 2 operating modes; X = don't care.

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	Off

11.4 Watchdog Timer

In addition to Timer T2 and the standard timers, a Watchdog Timer (consisting of an 11-bit prescaler and an 8-bit timer) is also incorporated.

The Watchdog Timer is controlled by the Watchdog Enable pin ($\overline{EWN}$). When $\overline{EWN}$ = 0, the timer is enabled and the Power-down mode is disabled. When $\overline{EWN}$ = 1, the timer is disabled and the Power-down mode is enabled. In the Idle mode the Watchdog Timer and reset circuitry remain active.

The Watchdog Timer is shown in Fig. 12.

The timer frequency is derived from the oscillator frequency using the following formula:

$$f_{timer} = \frac{f_{osc}}{(12 \times 2048)}$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at the RST pin. To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The Watchdog Timer can only be reloaded if the condition flag WLE (PCON.4) has been previously set by software. At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer reloading and the occurrence of a reset is dependent upon the reloaded value. For example, this time period may range from 2 ms to 500 ms when using an oscillator frequency f_{osc} = 12 MHz.

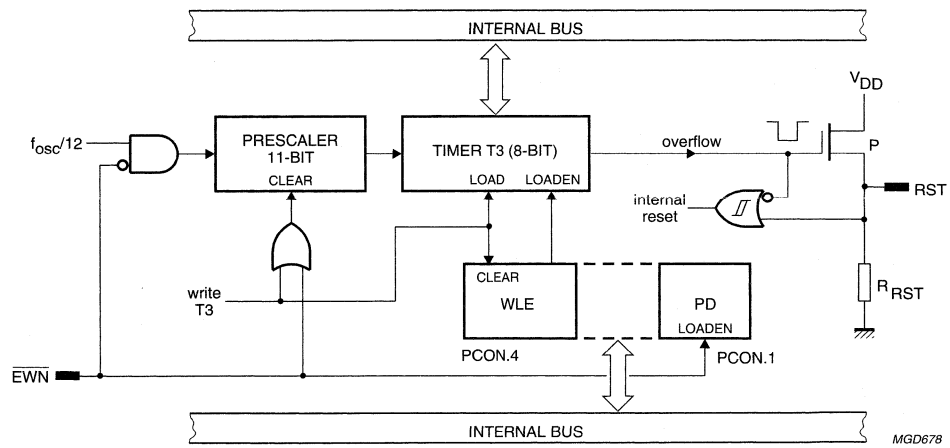


Fig.12 Functional diagram of the T3 Watchdog Timer.

12 PULSE WIDTH MODULATED OUTPUT

One Pulse Width Modulated output channel ($\overline{PWM0}$) is provided which outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler (PWMP) that generates the clock for the counter. The 8-bit counter counts modulo 255, i.e. from 0 to 254 inclusive. The value held in the 8-bit counter is compared to the contents of the register PWM0.

Provided the contents of this register are greater than the counter value, the $\overline{PWM0}$ output is set LOW. If the contents of register $\overline{PWM0}$ are equal to, or less than the counter value, the $\overline{PWM0}$ output is set HIGH.
The pulse-width-ratio is therefore defined by the contents of register PWM0. The pulse-width-ratio will be in the range 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency (f_{PWM}) at the $\overline{PWM0}$ output is given by:

$$f_{PWM} = \frac{f_{osc}}{\{2 \times (1 + PWMP) \times 255\}}$$

For f_{osc} = 12 MHz the above formula gives a repetition frequency range of 92 Hz to 23.5 kHz.

By loading the PWM0 register with either 00H or FFH, the $\overline{PWM0}$ output can be retained at a constant HIGH or LOW level respectively. When loading FFH into the PWM0 register, the 8-bit counter will never actually reach this value.

The $\overline{PWM0}$ output pin is driven by push-pull drivers and is not shared with any other function.

12.1 Prescaler Frequency Control Register (PWMP)

Table 5 Prescaler Frequency Control Register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 6 Description of PWMP bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWMP.7 to PWMP.0	Prescaler division factor = (PWMP) + 1.

12.2 Pulse Width Register (PWM0)

Table 7 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 8 Description of PWM0 bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWM0.7 to PWM0.0	LOW/HIGH ratio of $\overline{PWM0}$ signal = $\frac{(PWM0)}{\{255 - (PWM0)\}}$

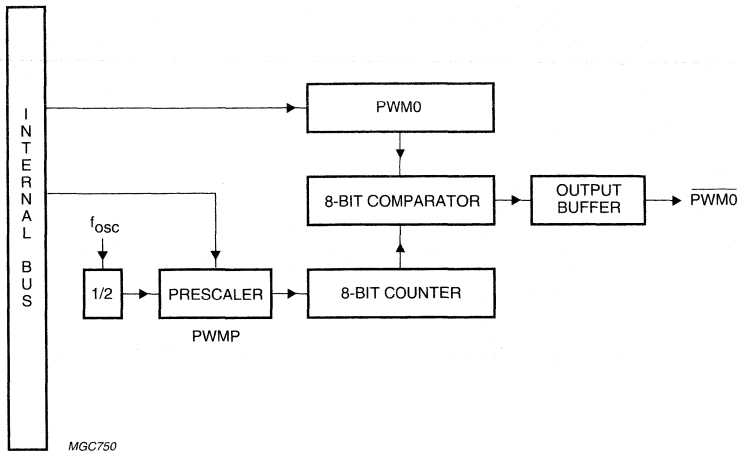


Fig.13 Functional diagram of Pulse Width Modulated output ($\overline{PWM0}$).

13 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consists of a 4-bit analog multiplexer and an ADC with 8-bit resolution. The analog reference voltage ($V_{ref(p)(A)}$) and analog ground (V_{SSA}) are connected via separate input pins. The conversion is selectable from 24 machine cycles (24 µs at f_{osc} = 12 MHz) to 48 machine cycles. The functional diagram of the ADC is shown in Fig. 14.

The ADC is controlled using the ADC Control Register (ADCON). Input channels are selected by the analog multiplexer via the ADCON register bits AADR0 and AADR1. The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in the Special Function Register ADCH (address C5H).

An ADC conversion in progress is unaffected by an external software ADC start.

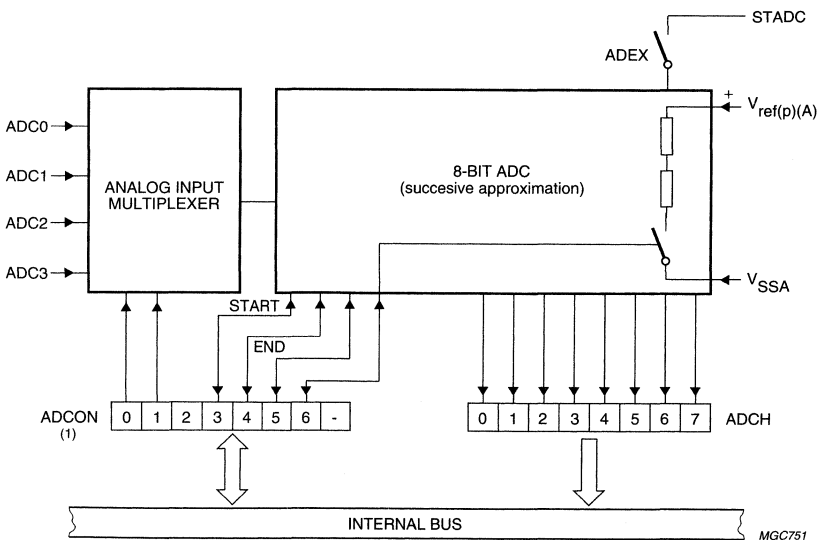
The result of a completed conversion remains unaffected provided ADCI = 1. While ADCS = 1 or ADCI = 1, a new ADC start will be blocked and consequently lost.

An ADC conversion already in progress is aborted when the Power-down mode is entered. The result of a completed conversion (ADCI = 1) remains unaffected when entering the Idle or Power-down mode.

The analog-to-digital conversion can be started in 3 ways:

- Start in operating mode, continue in operating mode
- Start in operating mode, by setting the ADCS bit, then go to Idle mode
- Set the ADEX bit, go to the Idle mode and start conversion externally via the STADC pin.

For the three cases mentioned above the internal flag ADCI is set upon completion of the conversion.



(1) For the descriptions of ADCON bits see Table 10.

Fig.14 Functional diagram of analog input.

13.1 ADC Control Register (ADCON)

Table 9 ADC Control Register (address C4H)

7	6	5	4	3	2	1	0
–	ADPD	ADEX	ADCI	ADCS	CKDIV	AADR1	AADR0

Table 10 Description of ADCON bits

BIT	SYMBOL	DESCRIPTION
7	–	Reserved.
6	ADPD	**Power-down.** This bit switches off the resistor reference to save power even when the CPU is operating.
5	ADEX	**Enable external start of conversion**. This bit determines whether a conversion can be started using the external pin STADC. When ADEX = 0, a conversion cannot be started externally using STADC. When ADEX = 1, a conversion can be started externally using STADC.
4	ADCI	**ADC interrupt flag**. This flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if this is enabled. This flag must be cleared by software (it cannot be set by software); see Table 11.
3	ADCS	**ADC start and status flag**. When this bit is set an ADC conversion is started. ADCS may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion ADCS is reset and after that the interrupt flag ADCI is set. ADCS cannot be reset by software; see Table 11.
2	CKDIV	This bit selects the conversion time, in terms of instruction cycles. This allows the CPU to be run at the maximum frequency (12 MHz) yet keeping the ADC timing at low frequency. When CKDIV = 0, the conversion time is equivalent to 24 instruction cycles. When CKDIV = 1, the conversion time is equivalent to 48 instruction cycles. The conversion time includes a sampling time of 6 cycles.
1	AADR1	**Analog input select**. These bits are used to select one of the four analog inputs; see Table 12. They only can be changed when ADCI and ADCS are both LOW.
0	AADR0	

Table 11 Analog-to-digital operation

ADCI	ADCS	OPERATION
0	0	ADC not busy; a conversion can be started.
0	1	ADC busy; start of a new conversion is blocked.
1	0	Conversion completed; start of a new conversion is blocked.
1	1	Intermediate status for a maximum of one machine cycle before conversion is completed (ADCI = 1, ADCS = 0).

Table 12 Selection of analog input channel

AADR1	AADR0	SELECTED CHANNEL
0	0	AD0
0	1	AD1
1	0	AD2
1	1	AD3

14 REDUCED POWER MODES

There are two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

14.1 Idle mode

Idle mode operation permits the interrupt, serial ports, timer blocks, PWM and ADC to continue to function while the clock to the CPU is halted.

Idle mode is entered by setting the IDL bit in the Power Control Register (PCON.0, see Table 14). The instruction that sets IDL is the last instruction executed in the normal operating mode before the Idle mode is activated

Once in Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 13.

The following functions remain active during the Idle mode:

- Timer 0, Timer 1, Timer 2 and Timer 3
- UART, I²C-bus interface
- External interrupt
- $\overline{\text{PWM0}}$ (reset; output = HIGH)
- ADC.

These functions may generate an interrupt or reset; thus ending the Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause IDL (PCON.0) to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 (PCON.2) and GF1 (PCON.3) may be used to determine whether the interrupt was received during normal execution or during the Idle mode.
   For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

14.2 Power-down mode

Operation in Power-down mode freezes the oscillator. The internal connections which link both Idle and Power-down signals to the clock generation circuit are shown in Fig.15.

Power-down mode is entered by setting the PD bit in the Power Control Register (PCON.1, see Table 14).
The instruction that sets PD is the last executed prior to going into the Power-down mode.

Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{\text{PSEN}}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

14.3 Wake-up from Power-down mode

When in Power-down mode the controller can be woken-up with either the external interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$, or a reset operation. The wake-up operation has two basic approaches as explained in Section 14.3.1; 14.3.2 and illustrated in Fig.16.

14.3.1 WAKE-UP USING $\overline{\text{INT2}}$ TO $\overline{\text{INT8}}$

If any of the interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$ are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

14.3.2 WAKE-UP USING RST

To wake-up the P8xCL580, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

14.4 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 13. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor 'p1'; see Fig.9(a).

Table 13 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	$\overline{\text{PWM0}}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	active	port data	port data	port data	port data	port data
	external	1	1	active	floating	port data	address	port data	port data
Power-down	internal	0	0	HIGH	port data	port data	port data	port data	port data
	external	0	0	HIGH	floating	port data	port data	port data	port data

14.5 Power Control Register (PCON)

Idle and Power-down modes are activated by software using this SFR. PCON is not bit addressable, the reset value of PCON is 0XX00000B.

Table 14 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	WLE	GF1	GF0	PD	IDL

Table 15 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate bit**. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
6 and 5	–	Reserved.
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading the Watchdog Timer (T3). It is cleared when T3 is loaded.
3 and 2	GF1 and GF0	**General purpose flag bits**.
1	PD	**Power-down bit**. Setting this bit activates the Power-down mode. This bit can only be set if input $\overline{\text{EWN}}$ is HIGH. If a logic 1 is written to both PD and IDL at the same time, PD takes precedence.
0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode.

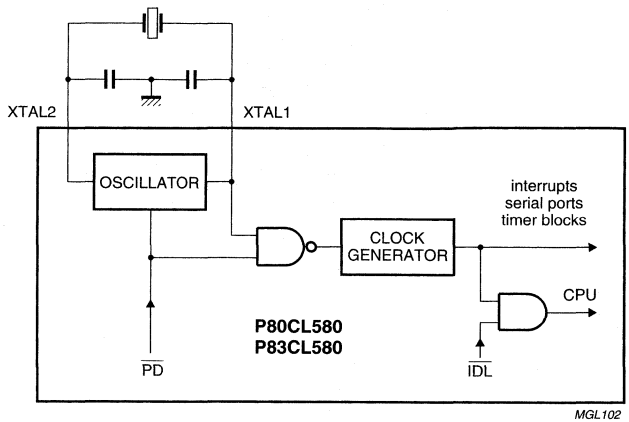


Fig.15 Internal clock control in Idle and Power-down modes.

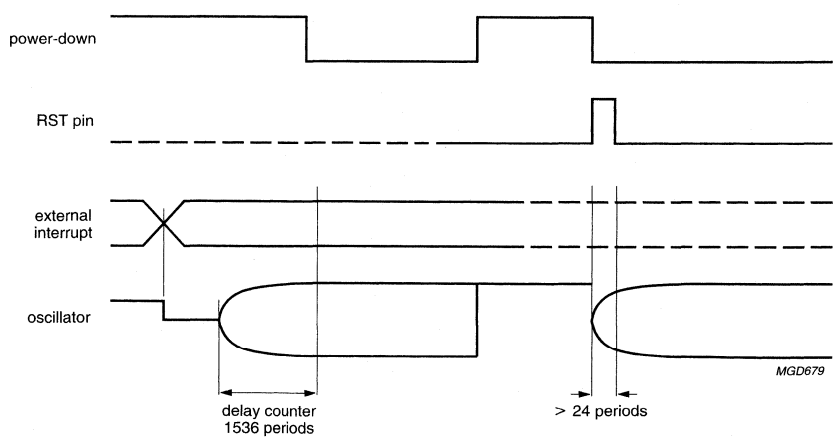


Fig.16 Wake-up operation.

15 I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus, which consists of a serial data line (SDA) and a serial clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the Serial Control Register S1CON. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR is the Slave Address Register. Slave address recognition is performed by on-chip hardware.

Figure 17 is the block diagram of the I²C-bus serial I/O.

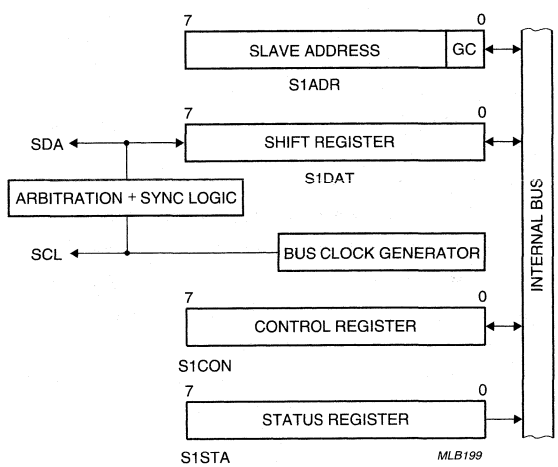


Fig.17 Block diagram of I²C-bus serial I/O.

15.1 Serial Control Register (S1CON)

Table 16 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 17 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
7	CR2	This bit along with bits CR1 (S1CON.1) and CR0 (S1CON.0) determines the serial clock frequency when SIO is in the Master mode. See Table 18.
6	ENS1	**ENABLE serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
5	STA	**START flag**. When this bit is set in Slave mode, the SIO hardware checks the status of the I²C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
4	STO	**STOP flag**. With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I²C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I²C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while GC (S1ADR.0) = 1 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A Stop or Start condition is received as selected slave receiver or transmitter.
2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received; GC (S1ADR.0) = 1 • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
1	CR1	These two bits along with the CR2 (S1CON.7) bit determine the serial clock frequency when SIO is in the Master mode. See Table 18.
0	CR0	

Table 18 Selection of the serial clock frequency SCL in a Master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE(kHz) AT f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100.0
1	1	0	60	59.7	100.0	–
1	1	1	not allowed	–	–	–

15.2 Serial Status Register (S1STA)

S1STA is a read-only register.The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given in Tables 21 to 25.

Table 19 Serial Status Register (address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 20 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
3 to 7	SC4 to SC0	5-bit status code.
0 to 2	–	These three bits are always zero.

Table 21 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 22 MST/REC mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
38H	Arbitration lost while returning $\overline{ACK}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{ACK}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{ACK}$ returned.

Table 23 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{ACK}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 24 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{ACK}$ received.
C8H	Last DATA byte has been transmitted (AA = 0), ACK received.

Table 25 Miscellaneous.

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.
F8H	No relevant state information available, SI = 0.

Table 26 Symbols used in Tables 21 to 25

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit is logic 0)
$\overline{ACK}$	No acknowledgement (acknowledge bit is logic 1)
DATA	8-bit data byte to or from I²C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

15.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. The MSB (bit 7) is transmitted or received first; i.e. data shifted from right to left.

Table 27 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

15.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 28 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 29 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	Own slave address.
0	GC	This bit is used to determine whether the general call address is recognized. When GC = 0, the general call address is not recognized; when GC = 1, the general call address is recognized.

16 STANDARD SERIAL INTERFACE SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted/received (LSB first). The baud rate is fixed at $1/12 \times f_{osc}$. See Figs 19 and 20.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable. See Figs 21 and 22.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of a logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64 \times f_{osc}$. See Figs 23 and 24.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable. See Figs 25 and 26.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

16.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

16.2 Serial Port Control and Status Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 30 Serial Port Control Register (address 98H)

7	6	5	4	3	2	1	0
SMO	SM1	SM2	REN	TB8	RB8	TI	RI

Table 31 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
7	SM0	These bits are used to select the serial port mode; see Table 32.
6	SM1	
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be a logic 0.
4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (except see SM2). Must be cleared by software.

Table 32 Selection of the serial port modes

SMO	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	Mode 0	Shift register	$1/12 \times f_{osc}$
0	1	Mode 1	8-bit UART	variable
1	0	Mode 2	9-bit UART	$1/32$ or $1/64 \times f_{osc}$
1	1	Mode 3	9-bit UART	variable

16.3 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as:

$$\text{Baud Rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON and may be calculated as:

$$\text{Baud Rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

- If SMOD = 0 (value on reset), the baud rate is $1/64 \times f_{osc}$
- If SMOD = 1, the baud rate is $1/32 \times f_{osc}$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

16.3.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the Baud Rate Generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow Rate.}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either 'timer' or 'counter' operation in any of its 3 running modes. In most typical applications, it is configured for 'timer' operation, in the Auto-reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{\{12 \times (256 - TH1)\}}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 33 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 33 Commonly used baud rates generated by Timer 1

BAUD RATE(kb/s)	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
1000.0[1]	12.000	X[2]	X	X	X
375.0[3]	12.000	1	X	X	X
62.5[4]	12.000	1	0	Mode 2	FFH
19.2	11.059	1	0	Mode 2	FDH
9.6	11.059	0	0	Mode 2	FDH
4.8	11.059	0	0	Mode 2	FAH
2.4	11.059	0	0	Mode 2	F4H
1.2	11.059	0	0	Mode 2	E8H
137.5	11.986	0	0	Mode 2	1DH
110.0	6.000	0	0	Mode 2	72H
110.0	12.000	0	0	Mode 1	FEEBH

Notes

1. Maximum in Mode 0.
2. X = don't care.
3. Maximum in Mode 2.
4. Maximum in Modes 1 and 3.

16.3.2 Using Timer 2 to generate baud rates

Timer 2 is selected as a Baud Rate Generator by setting the RTCLK bit in T2CON. The Baud Rate Generator mode is similar to the Auto-reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer 2 can be configured for either 'timer' or 'counter' operation. In the most typical applications, it is configured for 'timer' operation ($C/\overline{T2} = 0$). 'Timer' operation is slightly different for Timer 2 when it is being used as a Baud Rate Generator. Normally, as a timer it would increment every machine cycle at a frequency of $^1/_{12} \times f_{osc}$. However, as a Baud Rate Generator it increments every state time at a frequency of $^1/_2 \times f_{osc}$. In this case the baud rate in Modes 1 and 3 is determined as:

$$\text{Baud Rate} = \frac{f_{osc}}{32 \times \{65536 - (\text{RCAP2H; RCAP2L})\}}$$

Where (RCAP2H; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Baud Rate Generator mode for Timer 2 is shown in Fig.18. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the Baud Rate Generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2, TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the Baud Rate Generator mode, registers TH2 and TL2 should not be accessed (read or write). Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The registers RCAP2H and RCAP2L however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 or RCAP2H/RCAP2L should first be turned off by clearing the TR2 bit.

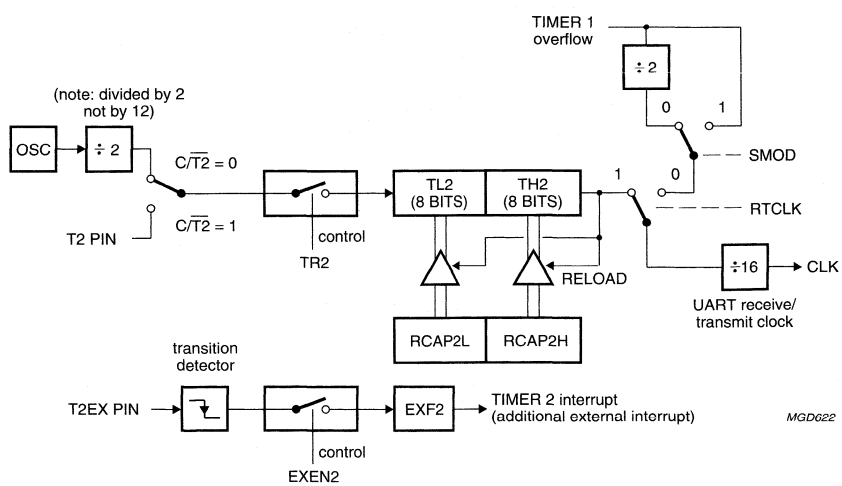


Fig.18 Timer 2 in Baud Rate Generator mode.

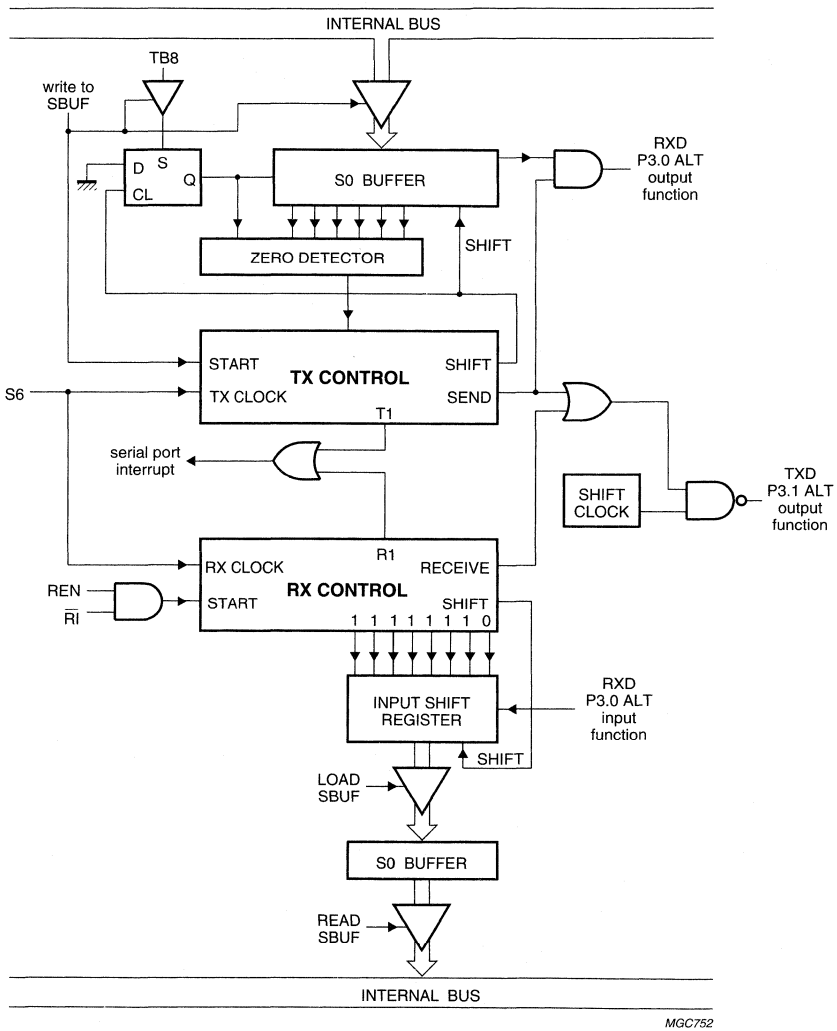


Fig.19 Serial port Mode 0.

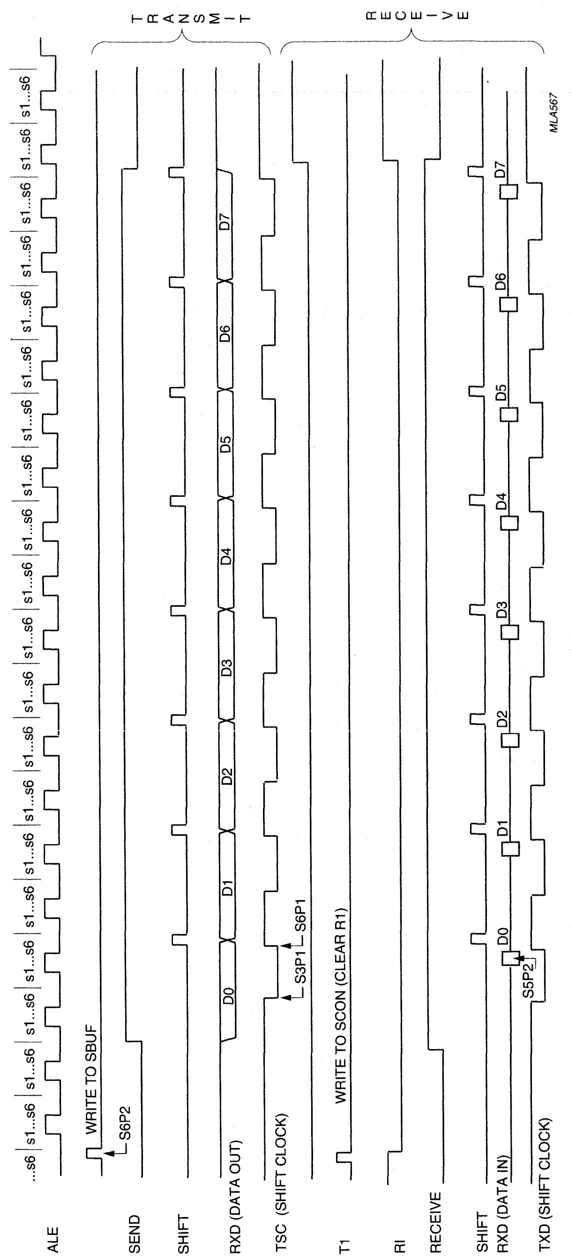


Fig.20 Serial port Mode 0 timing.

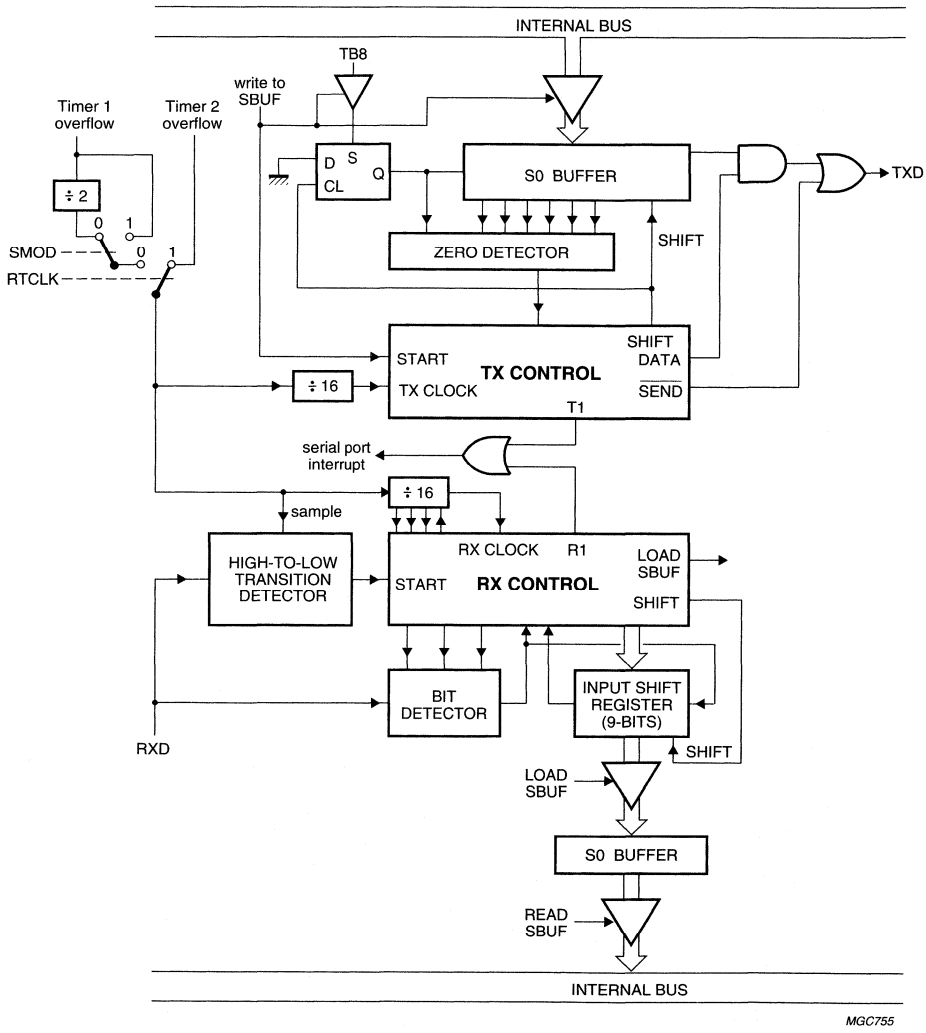


Fig.21 Serial port Mode 1.

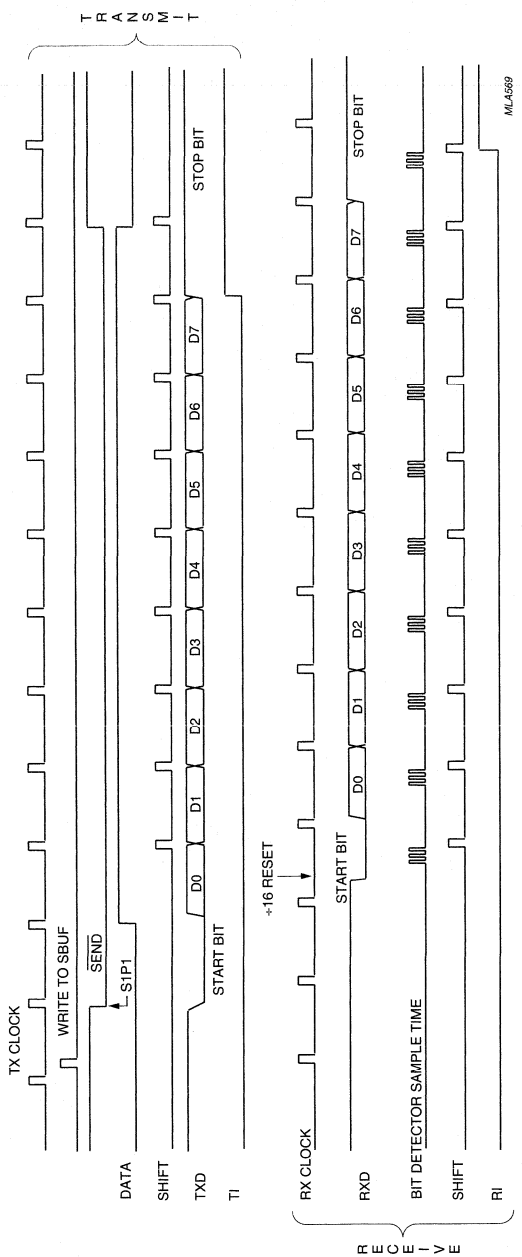


Fig.22 Serial port Mode 1 timing.

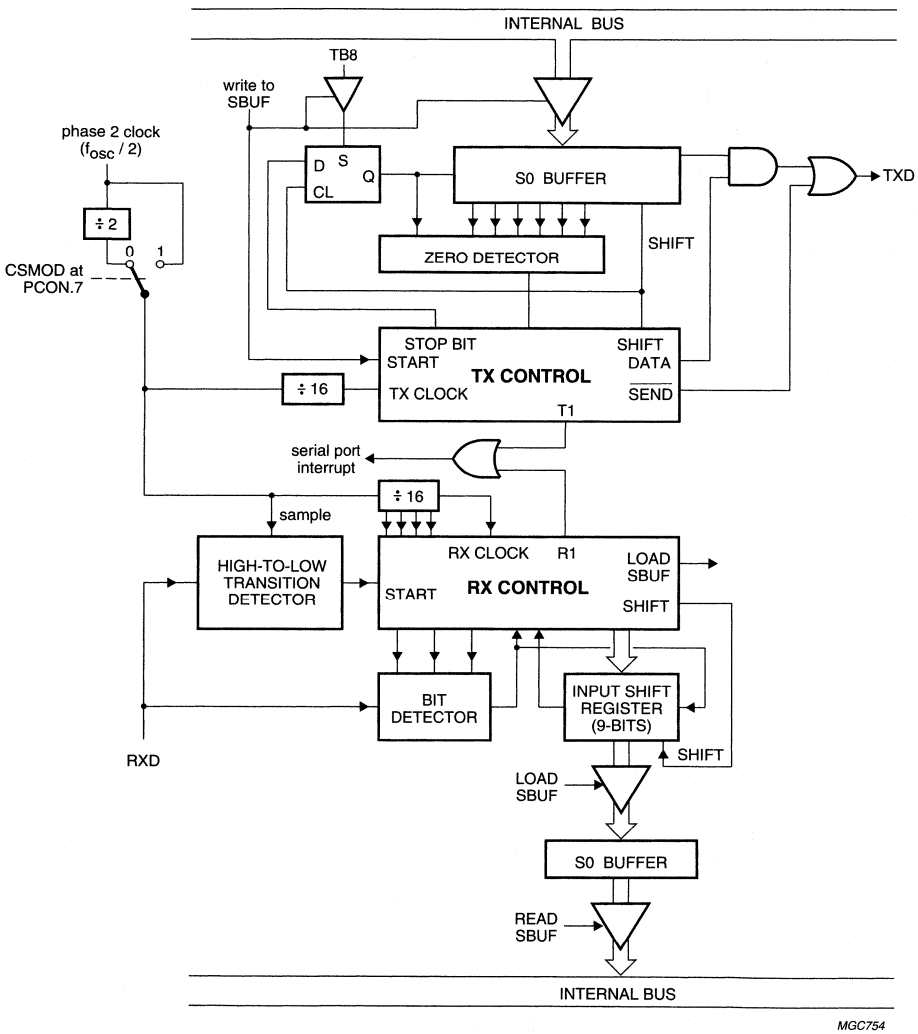


Fig.23 Serial port Mode 2.

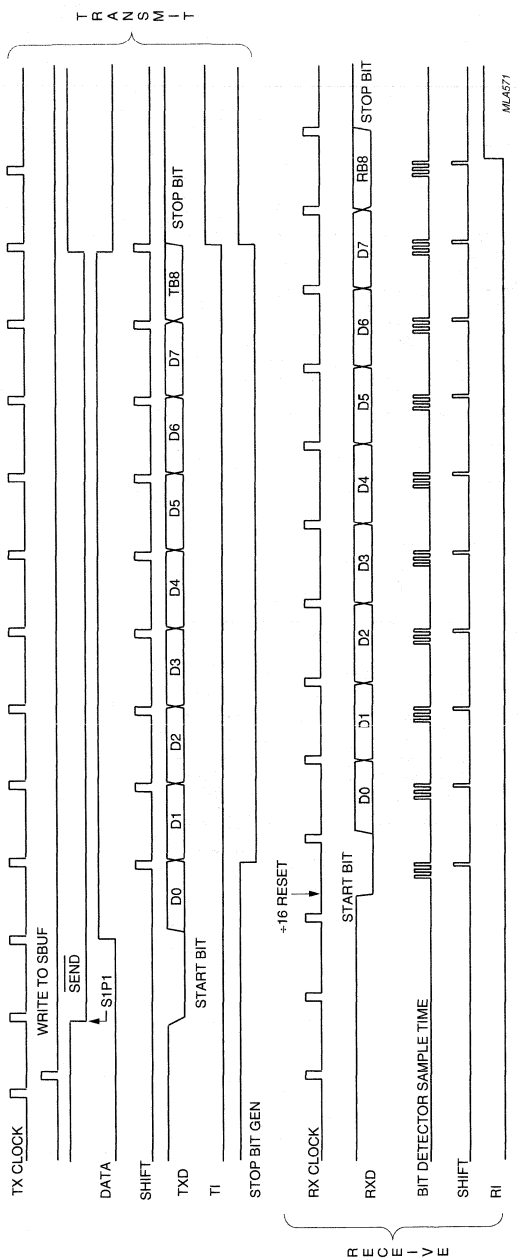


Fig.24 Serial port Mode 2 timing.

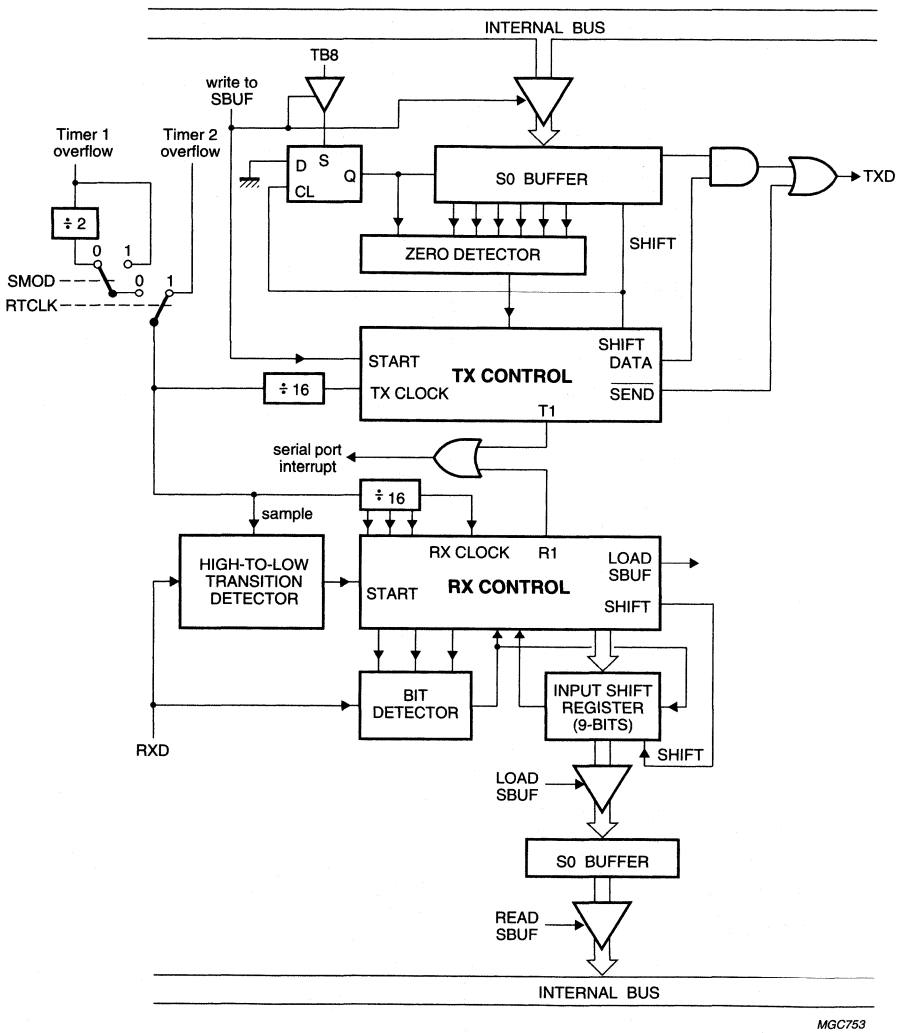


Fig.25 Serial port Mode 3.

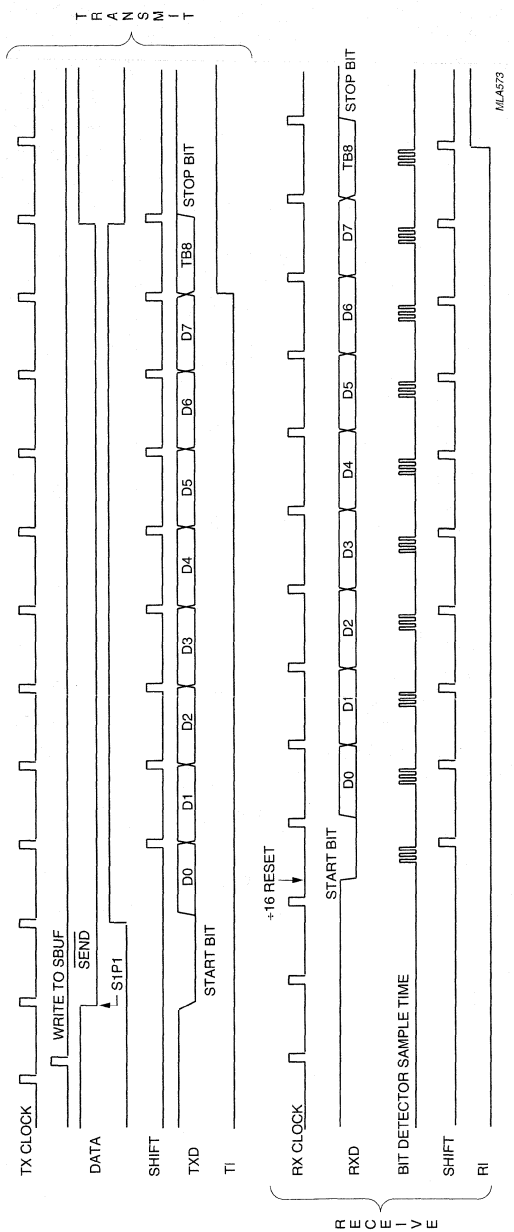


Fig.26 Serial port Mode 3 timing.

17 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU at unpredictable times. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The system is shown in Fig.27. The P8xCL580 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{INT0}$ to $\overline{INT8}$
- Timer 0, Timer 1 and Timer 2
- I²C-bus serial I/O
- UART
- ADC.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. Figure 27 shows the interrupt system.

17.1 External interrupts $\overline{INT2}$ to $\overline{INT8}$

Port 1 lines serve an alternative purpose as seven additional interrupts $\overline{INT2}$ to $\overline{INT8}$. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 28 shows the external interrupt system.

17.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If a low priority interrupt is received simultaneously with a high priority interrupt, the high priority interrupt will be dealt with first.

If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to the sequence shown in Table 34 and in Fig.27. The 'vector address' is the ROM location where the appropriate interrupt service routine starts.

Table 34 Interrupt vector polling sequence

SYMBOL	VECTOR ADDRESS (HEX)	SOURCE
X0 (first)	0003	External 0
S1	002B	I²C port
X5	0053	External 5
T0	000B	Timer 0
T2	0033	Timer 2
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
SO	0023	UART
X4	004B	External 4
ADC (last)	0073	ADC

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

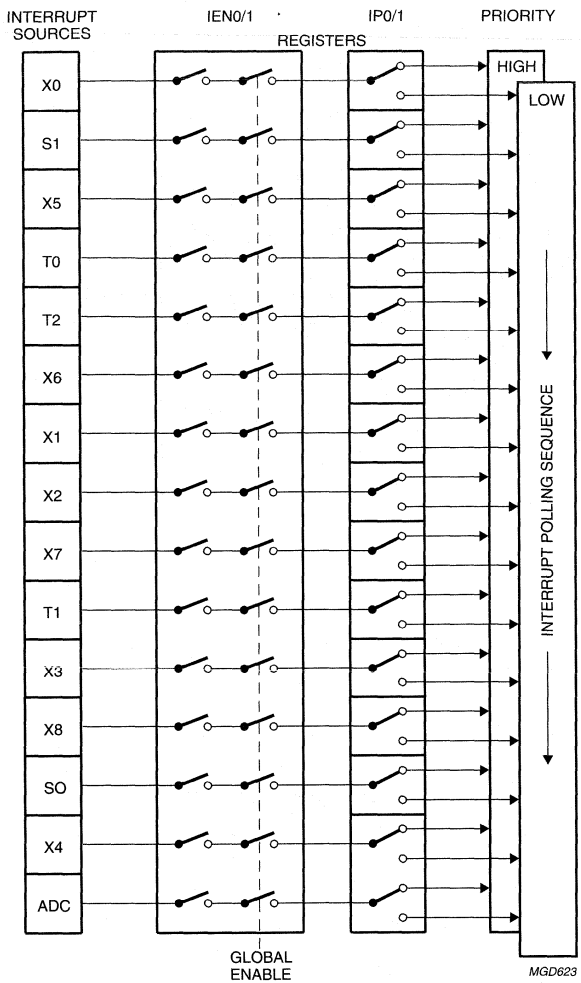


Fig.27 Interrupt system.

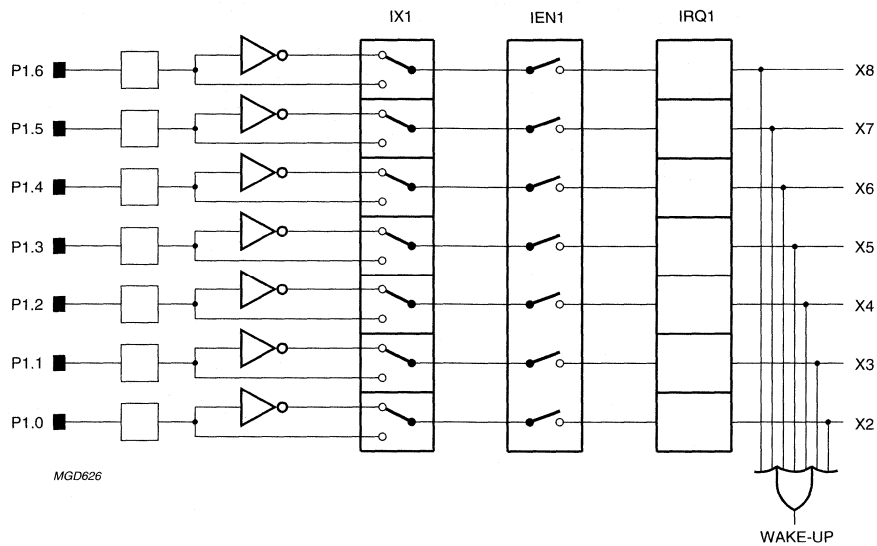


Fig.28 External interrupt configuration.

17.3 Interrupt registers

The registers used in the interrupt system are listed in Table 35. Tables 36 to 47 describe the contents of these registers.

Table 35 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register ($\overline{INT2}$ to $\overline{INT8}$)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

17.3.1 Interrupt Enable Register (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 36 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 37 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
6	ET2	enable T2 interrupt
5	ES1	enable I²C interrupt
4	ES0	enable UART SIO interrupt
3	ET1	enable Timer 1 interrupt (T1)
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt (T0)
0	EX0	enable external interrupt 0

17.3.2 Interrupt Enable Register (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 38 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EAD	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 39 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EAD	Enable ADC interrupt.
6	EX8	enable external interrupt 8
5	EX7	enable external interrupt 7
4	EX7	enable external interrupt 6
3	EX5	enable external interrupt 5
2	EX4	enable external interrupt 4
1	EX3	enable external interrupt 3
0	EX2	enable external interrupt 2

17.3.3 Interrupt Priority Register (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 40 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 41 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	PT2	Timer 2 interrupt priority level
5	PS1	I²C interrupt priority level
4	PS0	UART SIO interrupt priority level
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

17.3.4 Interrupt Priority Register (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 42 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PADC	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 43 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PADC	ADC interrupt priority level
6	PX8	external interrupt 8 priority level
5	PX7	external interrupt 7 priority level
4	PX6	external interrupt 6 priority level
3	PX5	external interrupt 5 priority level
2	PX4	external interrupt 4 priority level
1	PX3	external interrupt 3 priority level
0	PX2	external interrupt 2 priority level

17.3.5 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 44 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
–	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 45 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

17.3.6 Interrupt Request Flag Register (IRQ1)

Table 46 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
–	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 47 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

18 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCL580 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.30. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 48 and Fig.29).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator invertor is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.29.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.29(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 48 and shown in Fig.29. The required option should be stated when ordering.

Table 48 Oscillator options

OPTION	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.29(c).
Oscillator 2	Low-power, low-frequency operations using LC components; see Fig.29(e).
Oscillator 3	Medium frequency range applications.
Oscillator 4	High frequency range applications.
RC oscillator	RC oscillator configuration; see Figs 29(g) and 31.

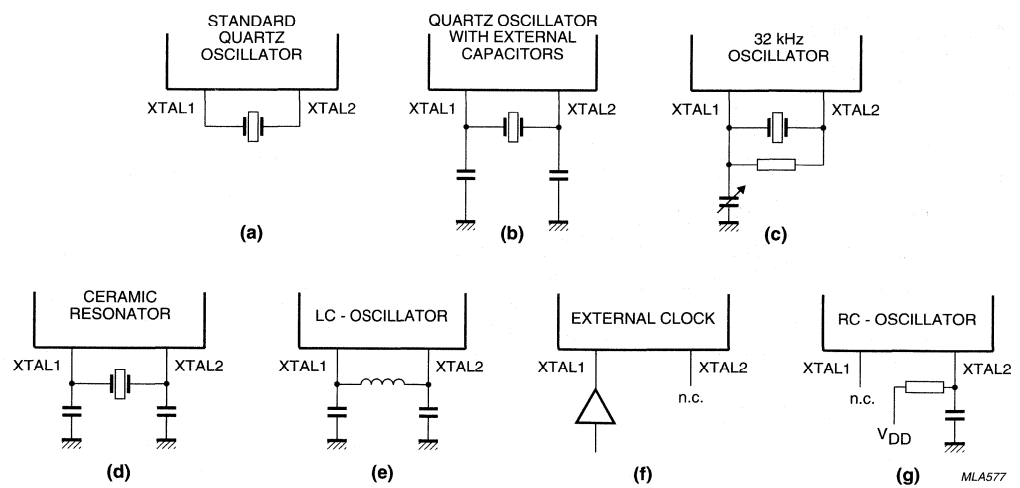


Fig.29 Oscillator configurations.

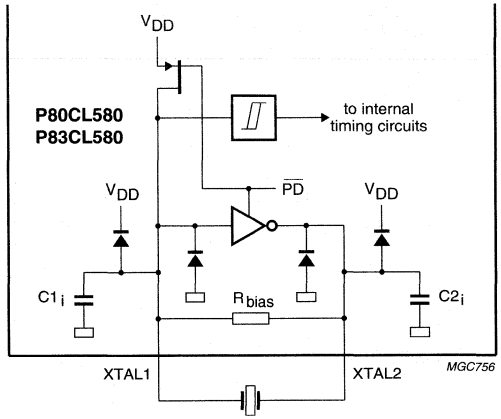
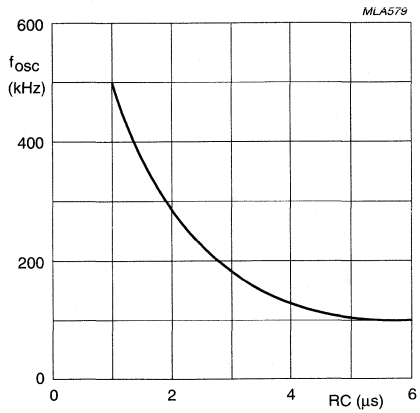


Fig.30 Standard oscillator.



RC oscillator frequency is externally adjustable; 100 kHz ≤ f_{osc} ≤ 500 kHz.

Fig.31 RC oscillator; frequency as a function of RC.

Table 49 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 48)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ; note 1
	1.0	Oscillator 2	0	30	0	30	600 Ω
	3.58		0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0	Oscillator 4	0	15	0	15	60 Ω
	12.0		0	10	0	10	40Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455	Oscillator 2	40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58		0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC		Oscillator 2	20	90	20	90	10 µH = 1 Ω 100 µH = 5 Ω 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

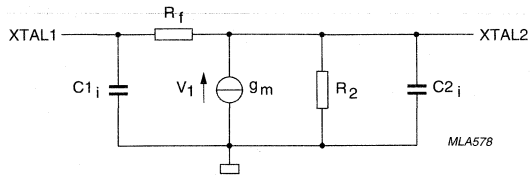


Fig.32 Oscillator equivalent circuit diagram.

Table 50 Oscillator equivalent circuit parameters

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Oscillator 1; 32 kHz	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
		Oscillator 2		200	600	1000	µS
		Oscillator 3		400	1 500	4000	µS
		Oscillator 4		1000	4000	10000	µS
$C1_i$	input capacitance	Oscillator 1; 32 kHz		–	3.0	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
$C2_i$	output capacitance	Oscillator 1; 32 kHz		–	23	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
R2	output resistance	Oscillator 1; 32 kHz		–	3800	–	kΩ
		Oscillator 2		–	65	–	kΩ
		Oscillator 3		–	18	–	kΩ
		Oscillator 4		–	5.0	–	kΩ

19 RESET

To initialize the P8xCL580 a reset is performed by either of three methods:

- Applying an external signal to the RST pin
- Via Power-on-reset circuitry
- Watchdog Timer.

A reset leaves the internal registers as shown in Chapter 20. The reset state of the port pins is mask-programmable and can be defined by the user.

19.1 External reset using the RST pin

The reset input for the P8xCL580 is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The reset circuitry is also affected by the Watchdog timer; see Section 11.4. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

19.2 Power-on-reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation (see Fig.35).

The on-chip Power-on reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on-reset circuitry is shown in Fig.34.

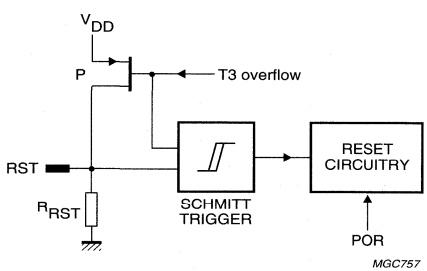


Fig.33 Reset configuration.

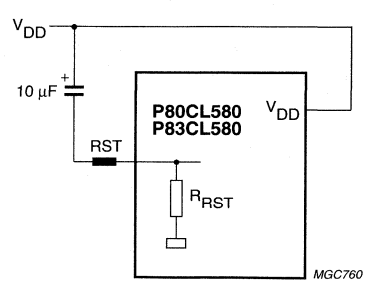


Fig.34 Recommended Power-on-reset circuitry.

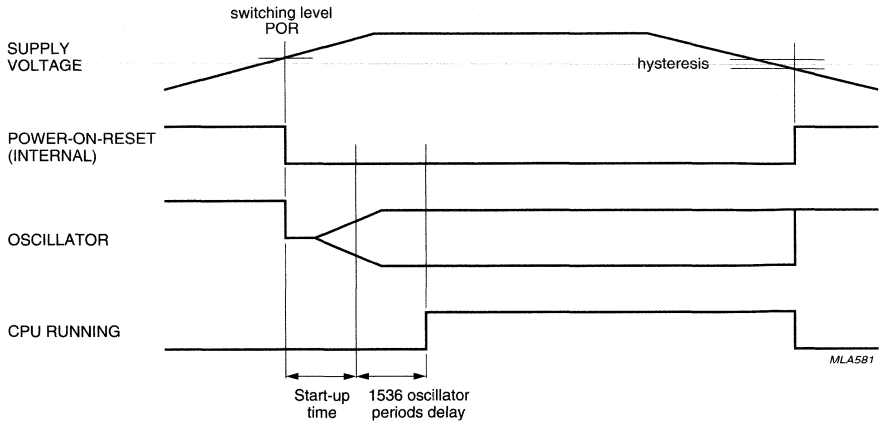


Fig.35 Power-on-reset switching level.

20 SPECIAL FUNCTION REGISTERS_OVERVIEW

The P8xCL580 has 40 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
FF	T3	00000000	Watchdog Timer
FE	PWMP	00000000	Prescaler Frequency Control Register
FC	PWM0	00000000	Pulse Width Register 0
F8	IP1	00000000	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
F0	B(1)	00000000	B Register
E9	IX1	00000000	Interrupt Polarity Register
E8	IEN1(1)	00000000	Interrupt Enable Register 1
E0	ACC(1)	00000000	Accumulator
DB	S1ADR	00000000	I²C-bus Slave Address Register
DA	S1DAT	00000000	I²C-bus Data Shift Register
D9	S1STA	11111000	I²C-bus Serial Status Register
D8	S1CON(1)	00000000	I²C-bus Serial Control Register
D0	PSW(1)	00000000	Program Status Word
CD	TH2	00000000	Timer 2 High byte
CC	TL2	00000000	Timer 2 Low byte
CB	RCAP2H	00000000	Timer 2 Reload/Capture Register High byte
CA	RCAP2L	00000000	Timer 2 Reload/Capture Register Low byte
C8	T2CON(1)	00000000	Timer/Counter 2 Control Register
C5	ADCH	11111111	ADC Result Register
C4	ADCON	X0000000	ADC Control Register
C1	P4	XXXXXXXX(2)	Digital I/O Port Register 4
C0	IRQ1(1)	00000000	Interrupt Request Flag Register

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
B8	IP0[1]	X0000000	Interrupt Priority Register 0
B0	P3[1]	XXXXXXXX[2]	Digital I/O Port Register 3
A8	IEN0[1]	00000000	Interrupt Enable Register
A0	P2[1]	XXXXXXXX[2]	Digital I/O Port Register 2
99	S0BUF	XXXXXXXX	Serial Data Buffer Register 0
98	S0CON[1]	00000000	Serial Port Control Register 0
90	P1[1]	XXXXXXXX[2]	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON[1]	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	0XX00000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0[1]	XXXXXXXX[2]	Digital I/O Port Register 0

Notes

1. Bit addressable register.
2. Port reset state determined by the customer.

21 INSTRUCTION SET

The P8xCL580 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 55.

Table 51 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 52 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 53 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 54 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 55 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	111-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 56 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	1	MOV direct,Rr 0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	1	SUB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	1	MOV Rr,direct 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	1	CJNE Rr,#data,rel 0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	1	DJNZ Rr,rel 0	1	2	3	4	5	6	7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV A,direct [1]	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV direct,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

Note

1. MOV A, ACC is not a valid instruction.

22 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
I_I	DC current on any input	−5.0	+5.0	mA
I_O	DC current on any output	−5.0	+5.0	mA
P_{tot}	total power dissipation	−	300	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
T_j	operating junction temperature	−	+125	°C

23 DC CHARACTERISTICS

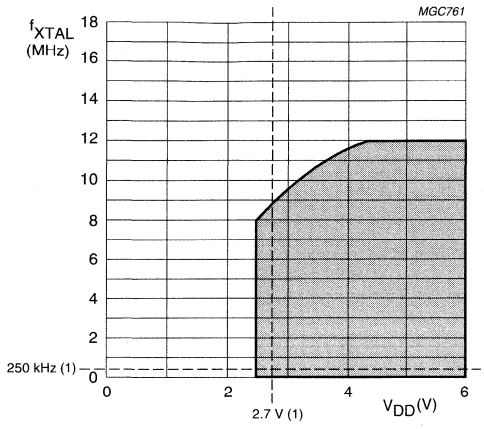
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +55 °C; see notes 1 and 2; all voltages with respect to V_{SS} unless specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.5	−	6.0	V
	RAM retention voltage in Power-down mode		1.0	−	6.0	V
I_{DD}	supply current operating	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 3	−	−	27.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 3	−	−	5.0	mA
$I_{DD(idle)}$	supply current Idle mode	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 4	−	−	10.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	−	−	3.0	mA
$I_{DD(pd)}$	Power-down current	V_{DD} = 1.8 V; T_{amb} = 25°C; note 5	−	−	10	µA
Inputs (note 6)						
V_{IL}	LOW level input voltage		V_{SS}	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	V
I_{LI}	input leakage current (Port 0; $\overline{EA}$)	$V_{SS} < V_I < V_{DD}$	−	−	±10	µA
Outputs						
I_{OL}	LOW level output current (except SDA; SCL)	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	−	−	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	−	−	mA
	LOW level output current SDA; SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	−	−	mA
	LOW level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OL} = 0.4 V	3.2	−	−	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	1.6	−	−	mA
I_{OH}	HIGH level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OH} = V_{DD} − 0.4 V	−3.2	−	−	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} − 0.4 V	−1.6	−	−	mA
I_{OH}	HIGH level output current (push-pull options only)	V_{DD} = 5 V; V_{OH} = V_{DD} − 0.4 V	−1.6	−	−	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} − 0.4 V	−0.7	−	−	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	input current logic 0	V_{DD} = 5 V; V_{IN} = 0.4 V	–	–	–100	µA
		V_{DD} = 2.5 V; V_{IN} = 0.4 V	–	–	–50	µA
I_{ITL}	input current logic 0; HIGH-to-LOW transition	V_{DD} = 5 V; V_{IN} = 0.5V_{DD}	–	–	–1.0	mA
		V_{DD} = 2.5 V; V_{IN} = 0.5V_{DD}	–	–	–500	µA
R_{RST}	RST pull-down resistor		10	–	200	kΩ
Analog inputs (note 7)						
$V_{IN(A)}$	analog input voltage		V_{SSA}	–	V_{DD}	mA
$V_{ref(p)(A)}$	reference voltage		2.7	–	V_{DD}	mA
R_{ref}	resistance between $V_{ref(p)(A)}$ and V_{SSA}		25	–	100	kΩ
C_{AIN}	analog on-chip input capacitance		–	3	–	pF
A_e	absolute error (note 8)		–	–	±1	LSB
OS_e	zero-offset error (note 9)		–	–	±1	LSB
DL_e	differential non-linearity (note 10)		–	–	±1	LSB
M_{ctc}	channel-to-channel matching (note 11)		–	–	±½	LSB

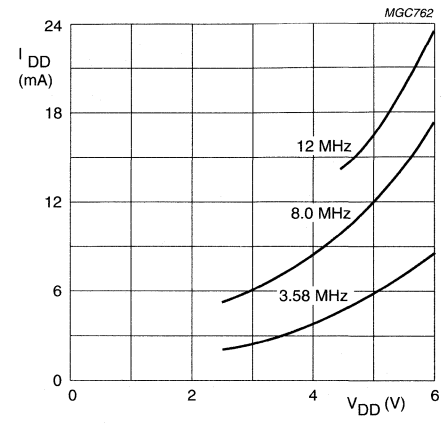
Notes to the DC characteristics

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these make a HIGH-to-LOW transition during bus operations. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse conditions (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
2. Capacitive loading on Ports 0 and 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9V_{DD} specification when the address bits are stabilizing.
3. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
4. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
5. The power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I²C-bus specification. Therefore, an input voltage below 0.3V_{DD} will be recognized as a logic 0 and an input voltage above 0.7V_{DD} will be recognized as a logic 1.
7. V_{DD} = 2.7 to 6 V; V_{SS} = 0 V; V_{SSA} = 0 V; $V_{ref(p)(A)} = V_{DD}$; T_{amb} = –40 to +85 °C, unless otherwise specified. $f_{xtal(min)}$ = 250 kHz.
8. Absolute error: the maximum difference between actual and ideal code transitions. Absolute error accounts for all deviations of an actual converter from an ideal converter.
9. Zero-offset error: the difference between the actual and ideal input voltage corresponding to the first actual code transition.
10. Differential non-linearity: the difference between the actual and ideal code widths.
11. Channel-to-channel matching: the difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions. Not tested, but verified on sampling basis.



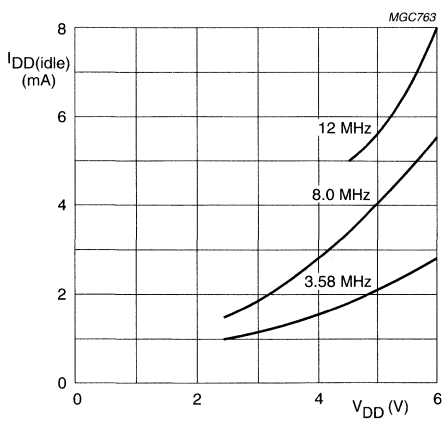
(1) The area above the dotted lines give the ADC operating area.

Fig.36 Frequency operating range.



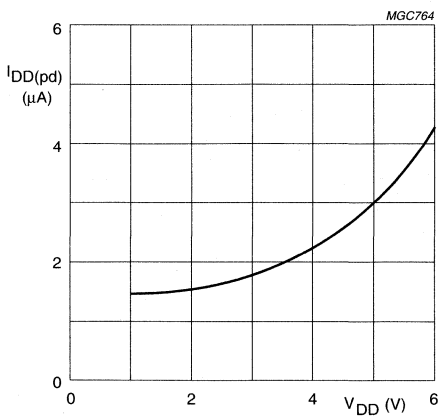
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.37 Typical operating current as a function of frequency and V_{DD}.



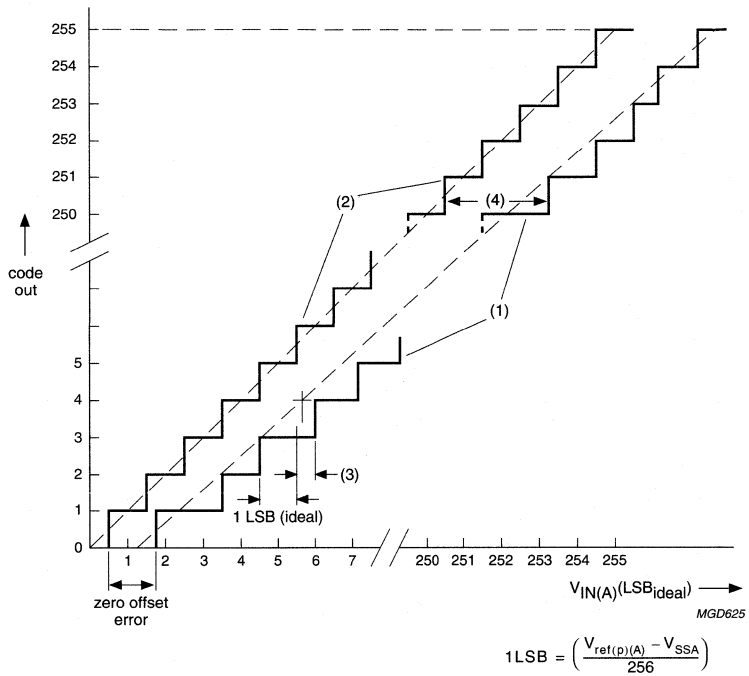
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.38 Typical Idle current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.

Fig.39 Typical Power-down current as a function of V_{DD}.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Absolute error.

Fig.40 Analog-to-digital conversion characteristics.

24 AC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified; $t_{CLK} = 1/f_{CLK}$.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Program Memory (Fig.41)						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	58	–	$t_{CLK} - 25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLK} - 35$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	125	–	$3t_{CLK} - 125$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLK} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid	75	–	$t_{CLK} - 8$	–	ns
t_{AVIV}	address to valid instruction in	–	302	–	$5t_{CLK} - 115$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	12	–	0	–	ns
External Data Memory (Figs 42 and 43)						
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	150	–	$5t_{CLK} - 165$	ns
t_{RHDZ}	data float after $\overline{RD}$	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	517		$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	203	–	4	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	12	–	12	ns

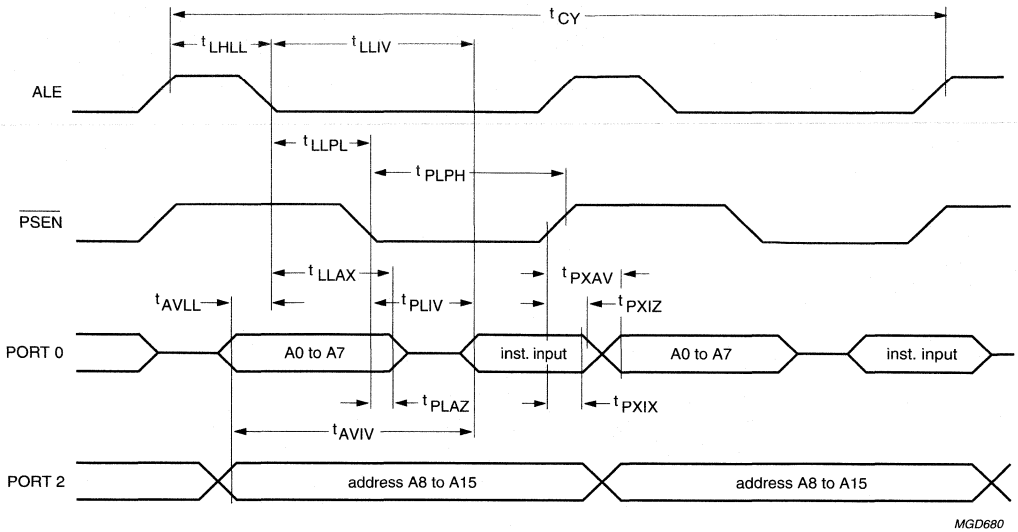


Fig.41 Read from Program Memory.

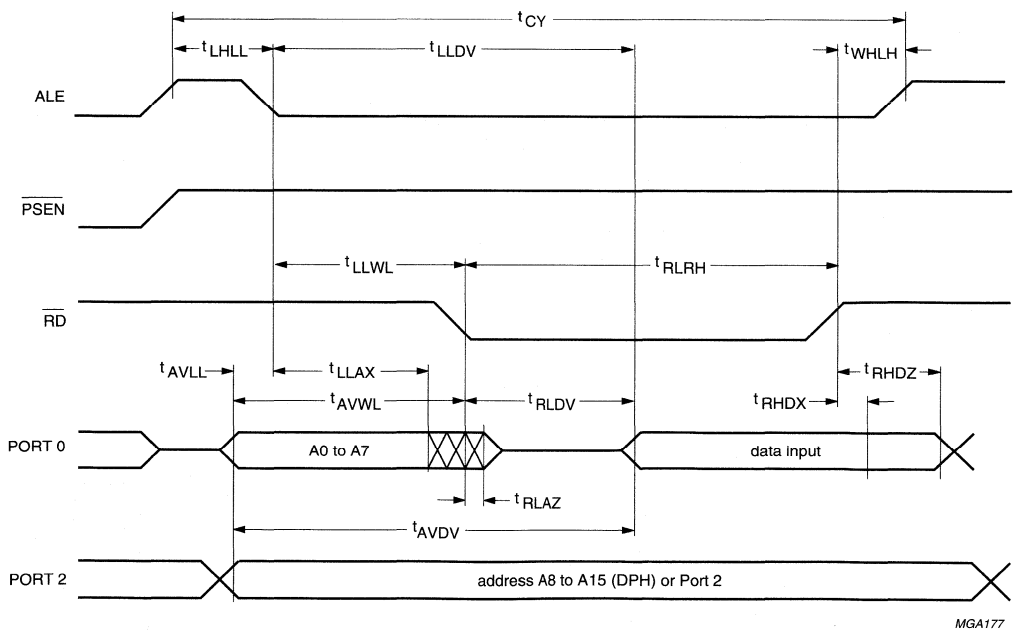


Fig.42 Read from Data Memory.

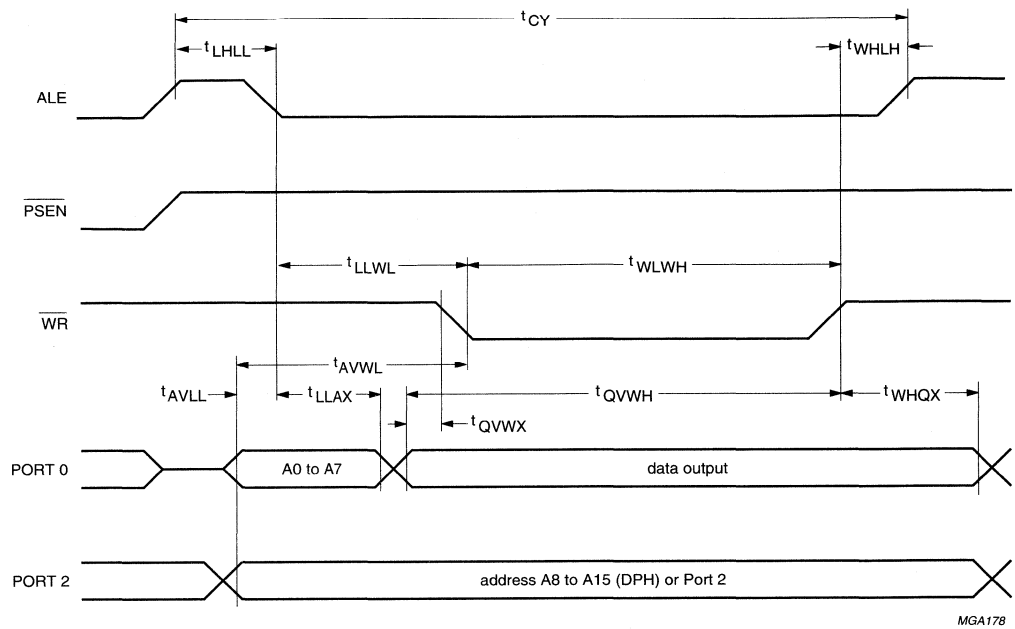


Fig.43 Write to Data Memory.

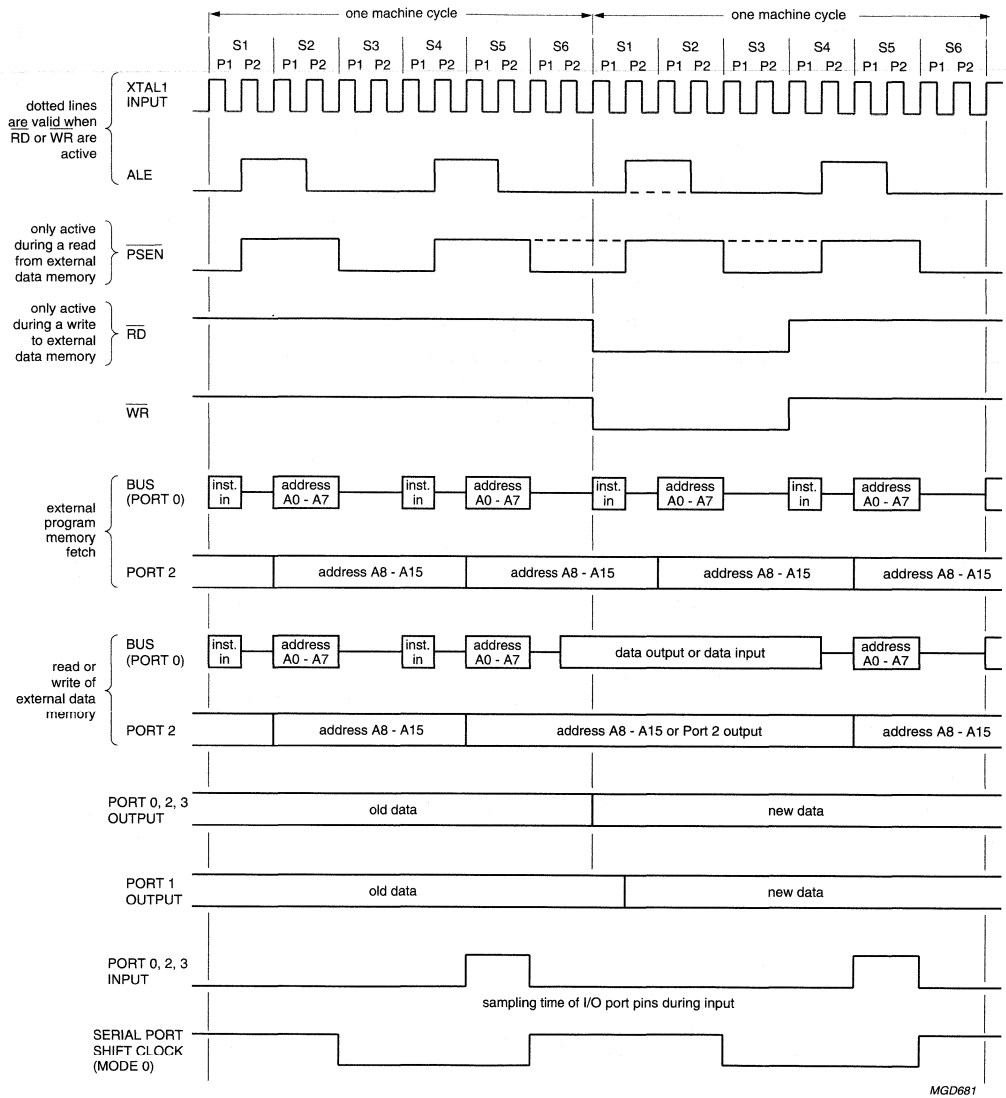


Fig.44 Instruction cycle timing.

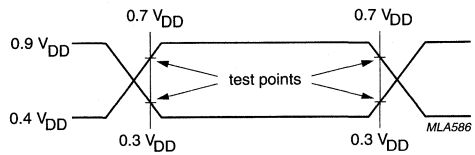


Fig.45 AC testing input waveform.

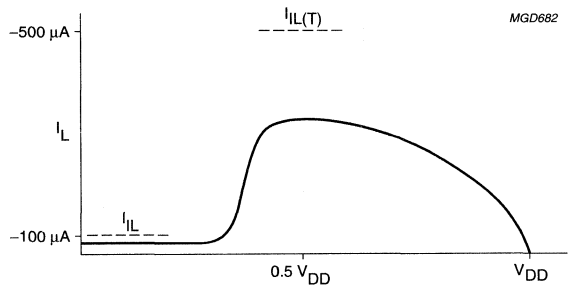


Fig.46 Input current.

Low voltage 8-bit microcontrollers with UART and I²C-bus

P83CL781; P83CL782

CONTENTS

Low voltage 8-bit microcontrollers with UART and I²C-bus

P83CL781; P83CL782

1 FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a 40-lead DIP or 44-lead QFP package
- 16 kbytes ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8 to 6.0 V
- Operating ambient temperature:
  - 83CL781: –40 to +85 °C
  - 83CL782: –25 to +55 °C.
- Frequency range of DC to 12 MHz
- Very low current consumption.

2 GENERAL DESCRIPTION

The term P83CL78x is used throughout this data sheet to refer to both the P83CL781 and P83CL782; differences between the devices are highlighted in the text.

The P83CL78x is manufactured in an advanced CMOS technology. The P83CL78x has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device has low power consumption and a wide range of supply voltage; there are two software-selectable modes of reduced activity for further power reduction: Idle and Power-down. For emulation purposes, the P85CL781 (piggy-back version) with 256 bytes of RAM is recommended.

The P83CL782 is a faster version of the P83CL781 and operates at a maximum frequency of 12 MHz at $V_{DD} \geq 3.1$ V.

This data sheet details the specific properties of the P83CL78x. For details of the 80C51 core and the I²C-bus see *"Data Handbook IC20"*.

3 APPLICATIONS

The P83CL78x is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The P83CL78x also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

4 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL781HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P83CL782HDP			
P83CL781HFH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
P83CL782HDH			
P83CL781HFH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
P83CL781HDH			

Note

1. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

5 BLOCK DIAGRAM

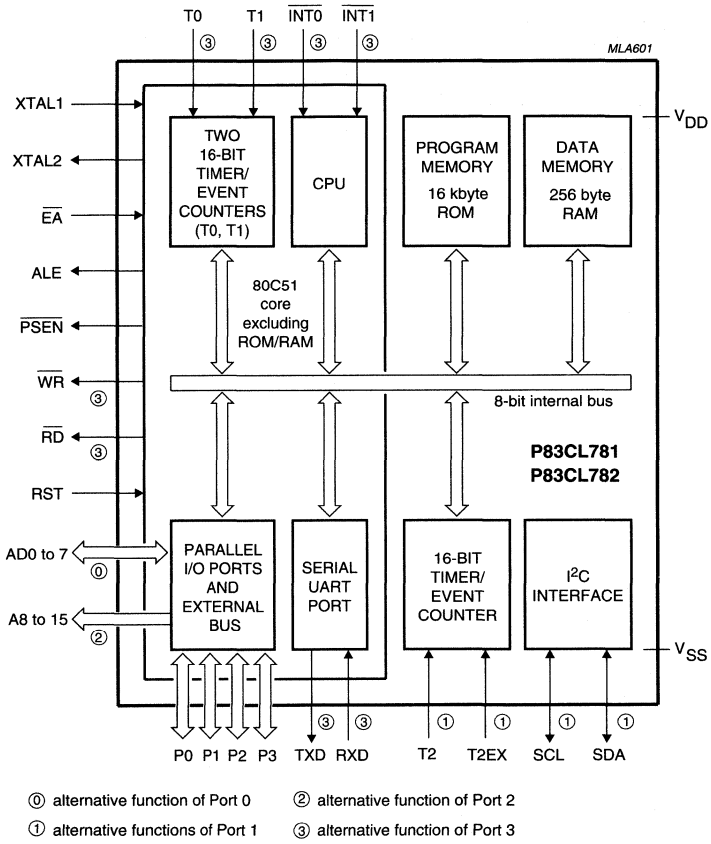


Fig.1 Block diagram.

6 FUNCTIONAL DIAGRAM

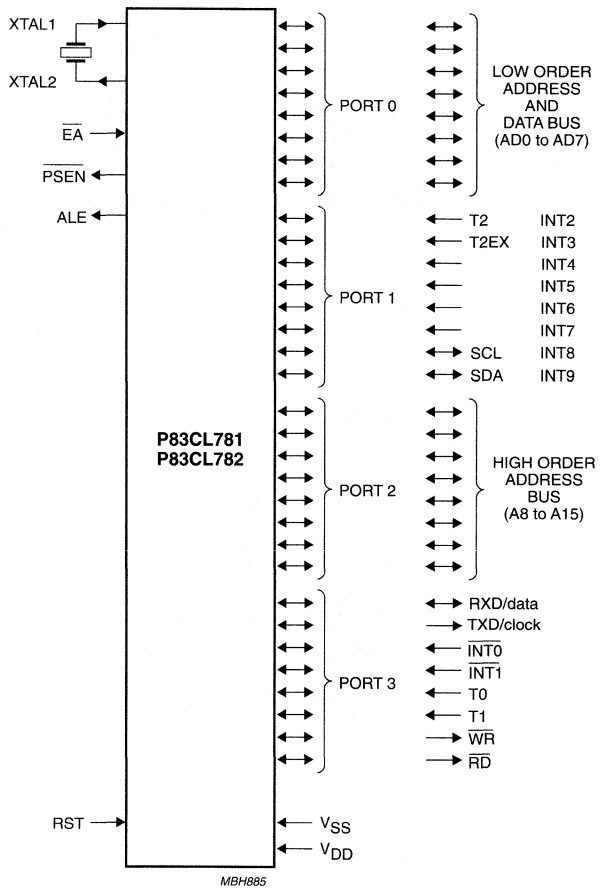


Fig.2 Functional diagram.

7 PINNING INFORMATION

7.1 Pinning

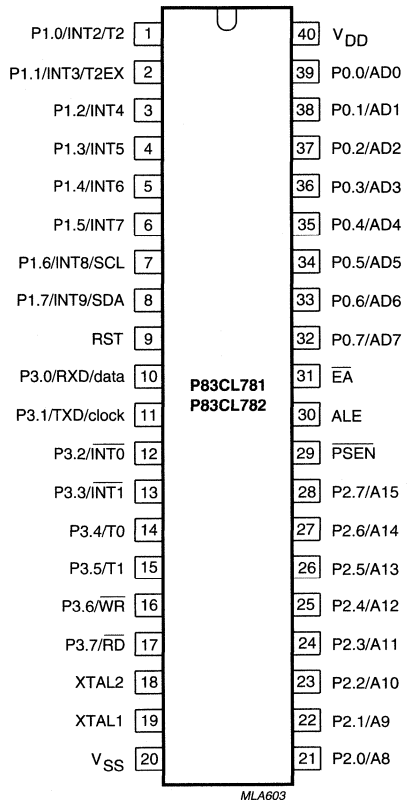


Fig.3 Pin configuration for DIP40 package.

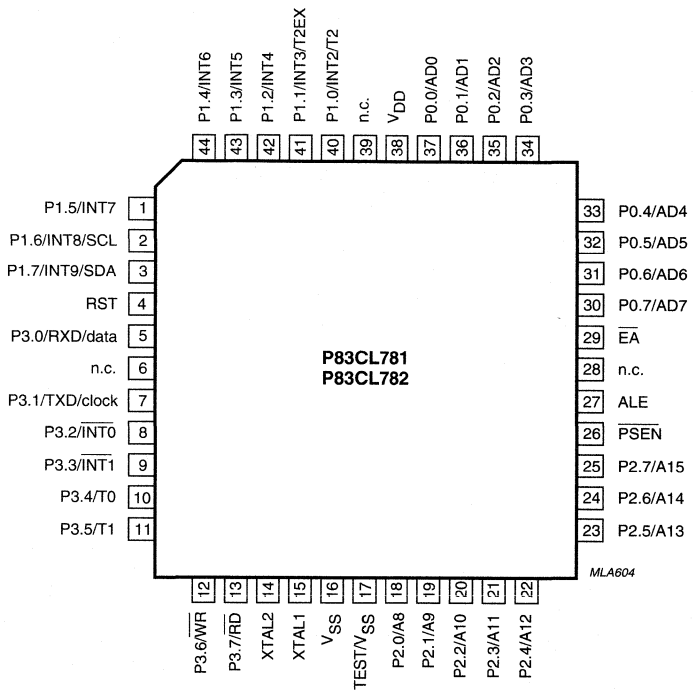


Fig.4 Pin configuration for QFP44 packages.

7.2 Pin description

SYMBOL	PIN		DESCRIPTION
	DIP40	QFP44	
P1.0/INT2/T2 P1.1/INT3/T2EX P1.2/INT4 P1.3/INT5 P1.4/INT6 P1.5/INT7 P1.6/INT8/SCL P1.7/INT9/SDA	1 2 3 4 5 6 7 8	40 41 42 43 44 1 2 3	• **Port 1:** 8-bit bidirectional I/O port (P1.0 to P1.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs (note that P1.6 and P1.7 are open-drain only). As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. • **Alternative functions:** – INT2 to INT9 are external interrupt inputs – T2 and T2EX are the Timer/event counter 2 inputs – SCL and SDA are the I²C-bus clock and data lines.
RST	9	4	**Reset:** A HIGH level on this pin for two machine cycles while the oscillator is running, resets the device.
n.c.	–	6	Not connected.
P3.0/RXD/data P3.1/TXD/clock P3.2/$\overline{\text{INT0}}$ P3.3/$\overline{\text{INT1}}$ P3.4/T0 P3.5/T1 P3.6/$\overline{\text{WR}}$ P3.7/$\overline{\text{RD}}$	10 11 12 13 14 15 16 17	5 7 8 9 10 11 12 13	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 1. • **Alternative functions:** – RXD/data is the UART serial data input (asynchronous) or data I/O (synchronous) – TXD/clock is the UART serial data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are external interrupt lines – T0 and T1 are external inputs for Timer 0 and Timer 1 respectively – $\overline{\text{WR}}$ is the external memory write strobe and $\overline{\text{RD}}$ is the external memory read strobe.
XTAL2	18	14	**Crystal Output:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
XTAL1	19	15	**Crystal Input:** Input to the inverting amplifier that forms the oscillator, also the input for an externally generated clock source.
V_{SS}	20	16	**Ground:** Circuit ground potential.
TEST/V_{SS}	–	17	**Test Input:** Must be connected to V_{SS} or left open.
P2.0/A8 P2.1/A9 P2.2/A10 P2.3/A11 P2.4/A12 P2.5/A13 P2.6/A14 P2.7/A15	21 22 23 24 25 26 27 28	18 19 20 21 22 23 24 25	• **Port 2:** 8-bit bidirectional I/O port (P2.0 to P2.7). Same characteristics as Port 1. • **High-order addressing:** A8 to A15 make up the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX@DPTR). In this application the pins use the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX@Ri), the pins emit the contents of the P2 Special Function Register.

SYMBOL	PIN		DESCRIPTION
	DIP40	QFP44	
$\overline{PSEN}$	29	26	**Program Store Enable:** Read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{PSEN}$ activations are skipped.
ALE	30	27	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes.
n.c.	–	28	Not connected.
$\overline{EA}$	31	29	**External Access:** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal Program Memory (unless the Program Counter exceeds 3FFFH). When $\overline{EA}$ is held LOW, the CPU executes out of external Program Memory regardless of the value of the program counter.
P0.7/AD7	32	30	• **Port 0:** 8-bit open-drain bidirectional I/O port (P0.7 to P0.0). As an open-drain output port it can sink/source 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in this state will function as high-impedance inputs. • **Low-order addressing:** AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory. In this application the pins use the strong internal pull-ups when emitting logic 1s.
P0.6/AD6	33	31	
P0.5/AD5	34	32	
P0.4/AD4	35	33	
P0.3/AD3	36	34	
P0.2/AD2	37	35	
P0.1/AD1	38	36	
P0.0/AD0	39	37	
V_{DD}	40	38	**Power supply.**
n.c.	–	39	Not connected.

8 FUNCTIONAL DESCRIPTION OVERVIEW

This chapter gives a brief overview of the device. The detailed functional description is in the following chapters:

Chapter 9 "Memory organization"

Chapter 10 "I/O facilities"

Chapter 11 "Timer/event counters"

Chapter 12 "Reduced power modes"

Chapter 13 "I²C-bus serial I/O"

Chapter 14 "Standard serial interface SIO0: UART"

Chapter 15 "Interrupt system"

Chapter 16 "Oscillator circuitry"

Chapter 17 "Reset".

8.1 General

The P83CL78x is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products. The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of data storage.

The P83CL78x contains a non-volatile 16 kbyte read-only Program Memory; a static 256 byte read/write Data Memory; 32 I/O lines; three 16-bit timer/event counters; a fifteen-source, two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software-selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the timers, serial I/O and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, two serial interfaces are provided on-chip:

- a standard UART serial interface, and
- a standard I²C-bus serial interface. The I²C-bus serial interface has byte-oriented master and slave functions allowing communication with the whole family of I²C-bus compatible devices.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P83CL78x has a 16 kbyte Program Memory (ROM) plus 256 bytes of Data Memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory (see Fig.6). Using Ports P0 and P2, the P83CL78x can address up to 128 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

9.1 Program memory

The P83CL78x contains 16 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 16 kbytes of Program Memory can be implemented in either on-chip ROM or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then Program Memory fetches from addresses 0000H through to 3FFFH are directed to the internal ROM. Fetches from addresses 4000H through to FFFFH are directed to external ROM. Program Counter values greater than 3FFFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

9.2 Data memory

The P83CL78x contains 256 bytes of internal RAM and 34 Special Function Registers (SFRs). The memory map (Fig.6) shows the internal Data Memory space divided into the lower 128 bytes, the upper 128 bytes and the SFR space. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

9.3 Special Function Registers

The upper 128 bytes are the address locations of the Special Function Registers. Figures 7 and 8 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, and so on. These registers can only be accessed by direct addressing. There are 128 addressable locations in the SFR address space (SFRs with addresses divisible by eight).

9.4 Addressing

The P83CL78x has five methods for addressing source operands:

- Register
- Direct
- Register-indirect
- Immediate
- Base-register plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

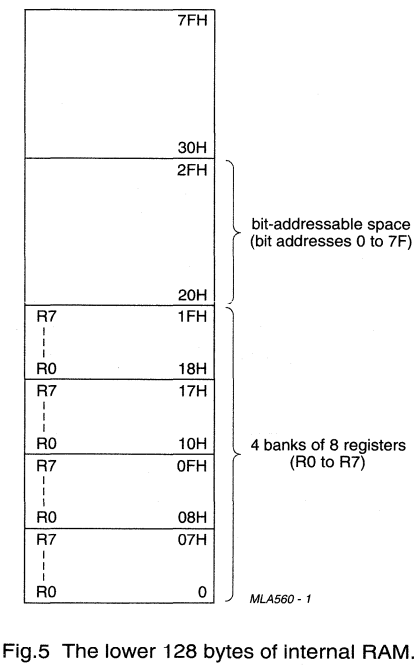


Fig.5 The lower 128 bytes of internal RAM.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or register-indirect
- 256 bytes of internal data RAM through direct or register-indirect
- Special Function Registers through direct
- External Data Memory through register-indirect
- Program Memory look-up tables through base-register plus index-register-indirect.

The P83CL78x is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

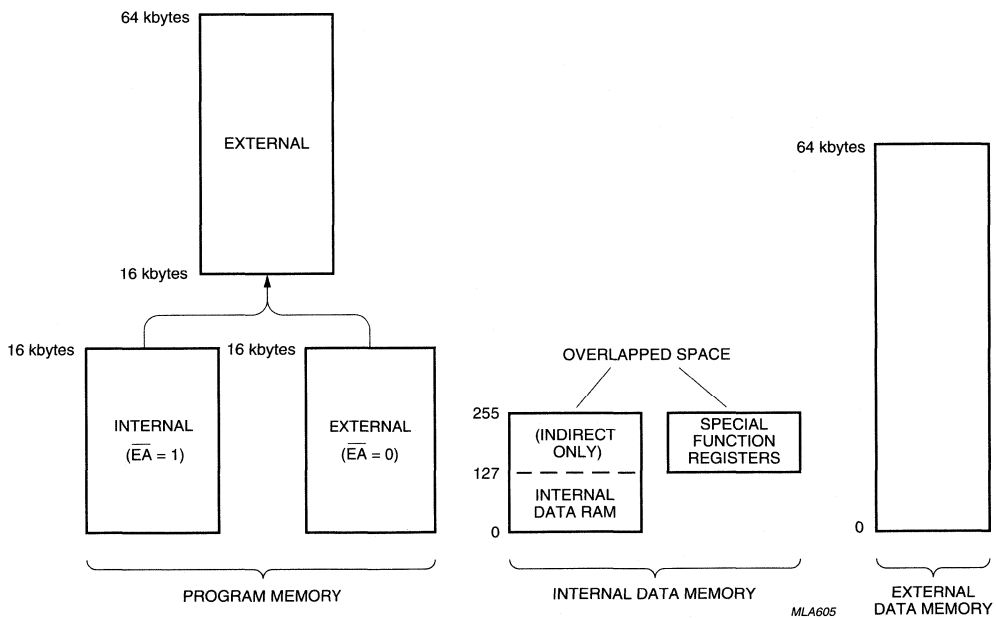


Fig.6 Memory map.

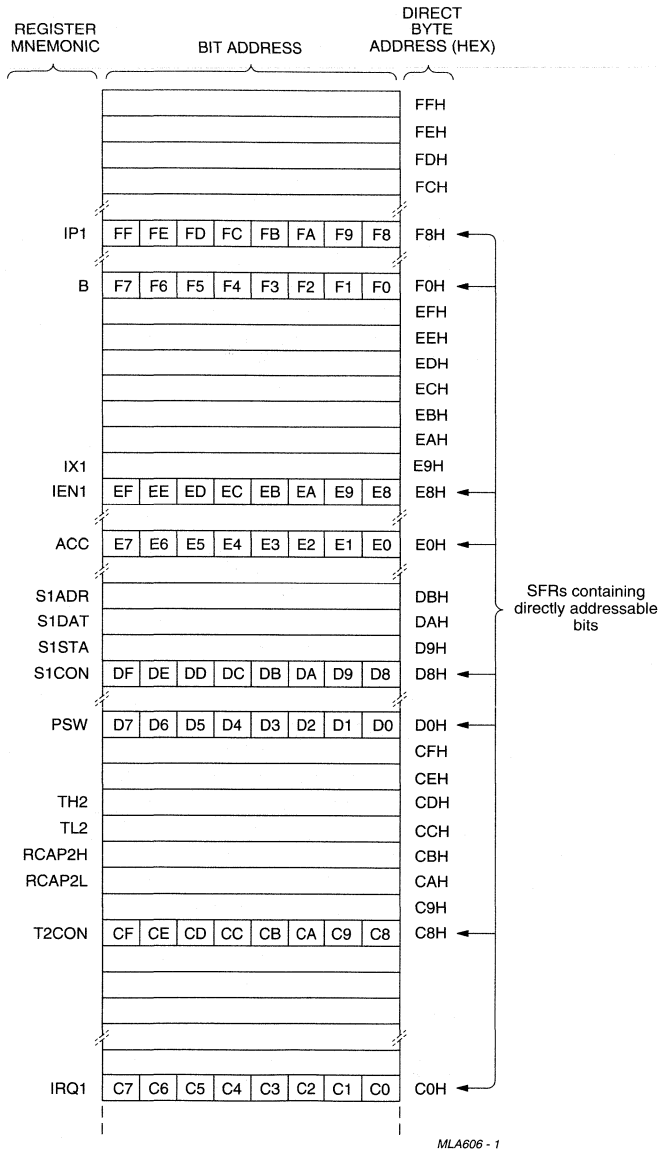


Fig.7 Special Function Register memory map (continued in Fig.8).

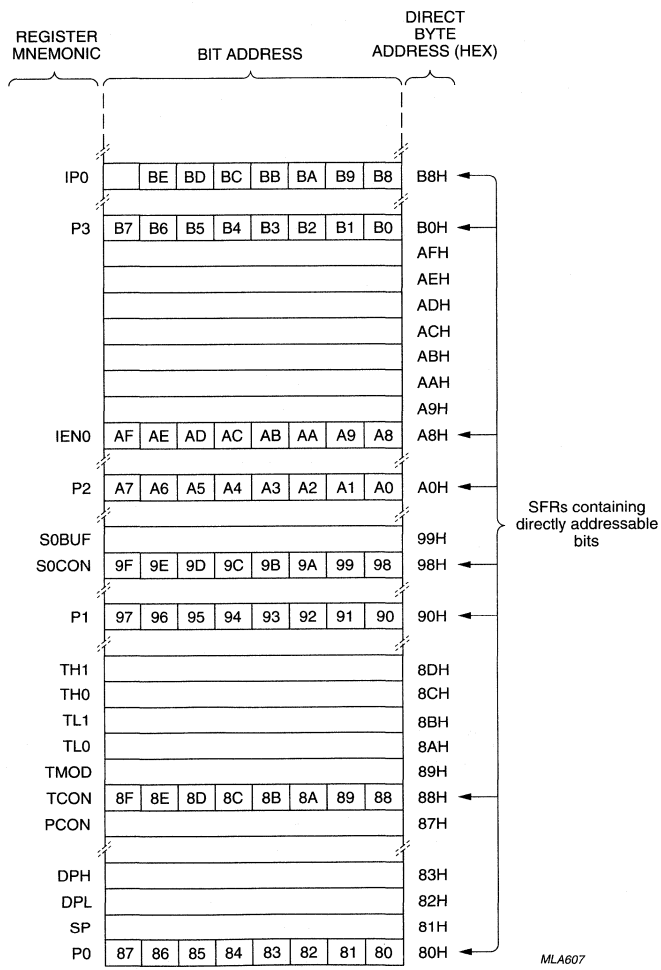


Fig.8 Special Function Register memory map (continued from Fig.7).

10 I/O FACILITIES

10.1 Ports

The P83CL78x has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit ports. To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1. The alternative functions are detailed below:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the eight external interrupts: INT2 to INT9
- External activation of Timer 2: T2
- The I²C-bus interface: SCL and SDA.

Port 2 Provides the high-order address when expanding the device with external Program or Data memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{INT1}$ and $\overline{INT0}$
- Timer/counter inputs: T1 and T0
- Control signals to read and write to external memories: $\overline{RD}$ and $\overline{WR}$
- UART asynchronous input and output (RXD and TXD); or UART synchronous I/O and clock lines (data and clock).1

Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Ports 1, 2 and 3 have internal pull-ups (except P1.6 and P1.7). Figure 9(a) shows that the strong transistor 'p1' is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter. This inverter and p3 form a latch which holds the logic 1. In Port 0 the pull-up 'p1' is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 1 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

10.2 Port options

30 of the 32 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.9.

Option 1 **Standard Port;** quasi-bidirectional I/O with pull-up. The strong booster pull-up 'p1' is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.9(a).

Option 2 **Open-drain**; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; Fig.9(b).

Option 3 **Push-Pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs; Fig.9(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 External memory accesses

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up 'p1' will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.9(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.9(c).

10.4 SET/RESET options

Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending 'S' or 'R' to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

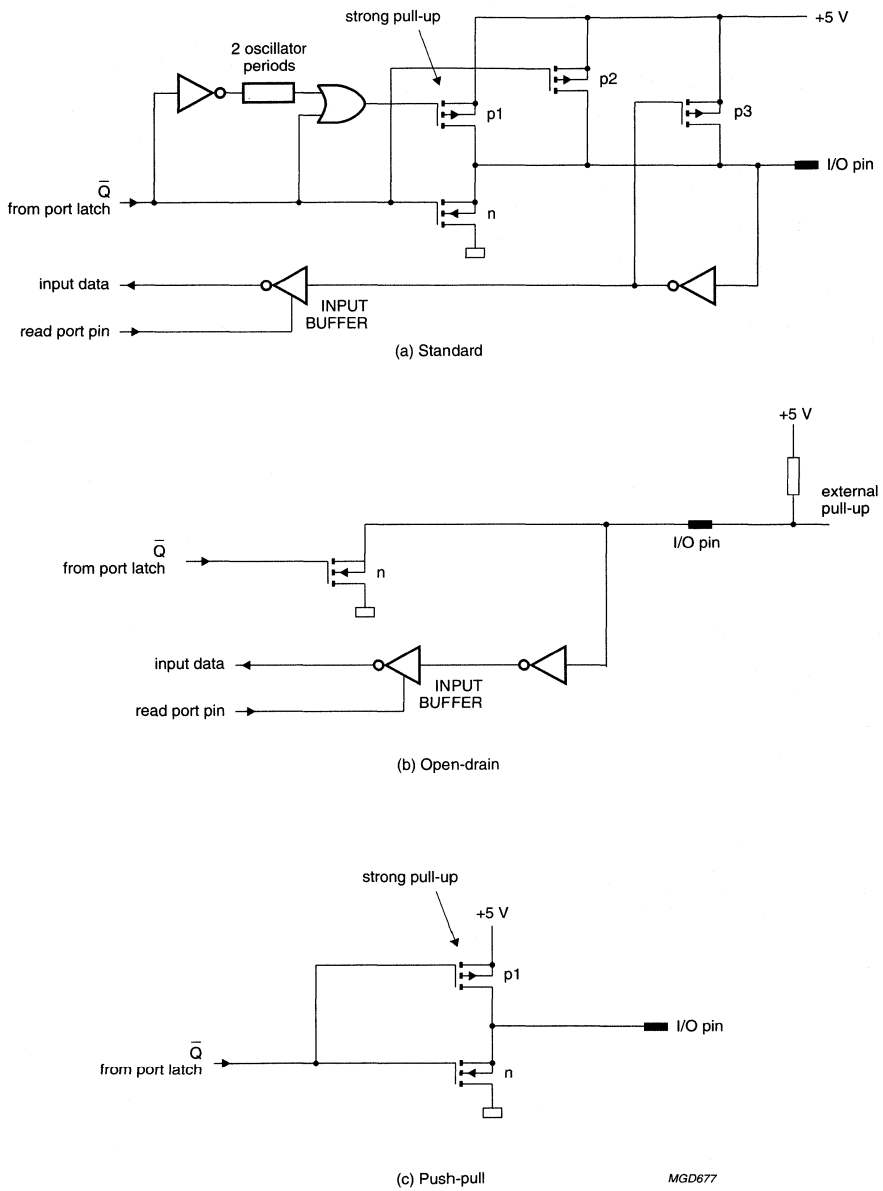


Fig.9 Port configuration options.

11 TIMER/EVENT COUNTERS

The P83CL78x contains three 16-bit timer/event counter registers; Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12 \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/24 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

11.2 Timer T2

Timer T2 is a 16-bit timer/counter that can operate (like Timer 0 and 1) either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register; see Tables 1 and 2.

Three operating modes are available Capture, Auto-reload and Baud Rate Generator, which also are selected via the T2CON register; see Table 3.

11.2.1 Capture mode

Figure 10 shows the Capture mode. Two options in this mode, may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

11.2.2 Auto-reload mode

Figure 11 shows the Auto-reload mode. Also two options in this mode are selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

11.2.3 Baud Rate Generator mode

The Baud Rate Generator mode is selected when RTCLK = 1. It will be described in conjunction with the serial port (UART); see Section 14.3.2.

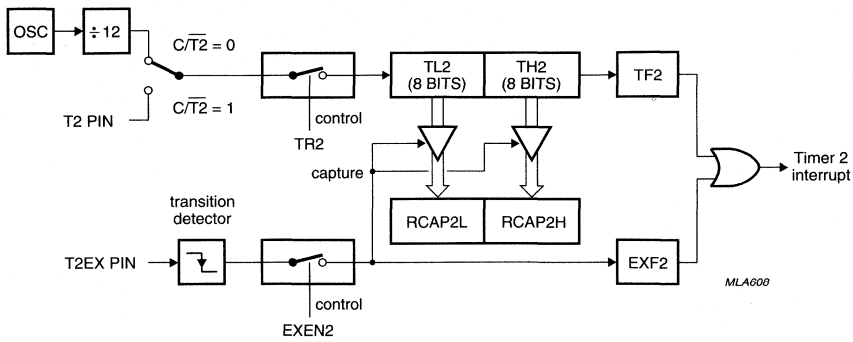


Fig.10 Timer 2 in Capture mode.

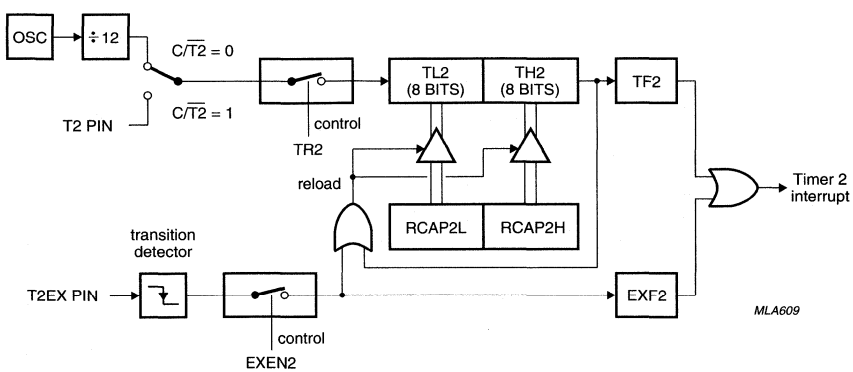


Fig.11 Timer 2 in Auto-Reload mode.

11.3 Timer/Counter 2 Control Register (T2CON)

Table 1 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 2 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag**. Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
6	EXF2	**Timer 2 external flag.** Set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	GF2	**General purpose flag** bit.
4	RTCLK	**Receive/transmit clock flag**. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
3	EXEN2	**Timer 2 external enable flag**. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0, causes Timer 2 to ignore events at T2EX.
2	TR2	**Start/stop control for Timer 2**. TR2 = 1 starts the timer.
1	C/$\overline{T2}$	**Timer or counter select for Timer 2**. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $^1/_{12} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge triggered.
0	CP/$\overline{RL2}$	**Capture/Reload flag**. When set, captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 3 Timer 2 operating modes; X = don't care

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	Off

12 REDUCED POWER MODES

There are two software-selectable modes which further reduce power consumption: 'Idle' and 'Power-down'.

12.1 Idle mode

Operation in Idle mode permits the interrupt, serial ports and timer blocks to continue to function while the clock to the CPU is halted.

Idle mode is entered by setting the IDL bit in the Power Control Register (PCON.0, see Table 5). The instruction that sets IDL is the last instruction executed in the normal operating mode before the Idle mode is activated.

Once in the Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 4.

The following functions remain active during the Idle mode:

- Timer 0, Timer 1 and Timer 2
- UART, I²C-bus interface
- External interrupt.

These functions may generate an interrupt or reset; thus ending the Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

12.2 Power-down mode

Operation in Power-down mode freezes the oscillator. The internal connections which link both Idle and Power-down signals to the clock generation circuit are shown in Fig.12.

Power-down mode is entered by setting the PD bit in the Power Control Register (PCON.1, see Table 5).
The instruction that sets PD is the last executed prior to going into the Power-down mode.

Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{PSEN}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

12.3 Wake-up from Power-down mode

When in Power-down mode the controller can be woken-up with either the external interrupts INT2 to INT9, or a reset operation. The wake-up operation has two basic approaches as explained in Section 12.3.1; 12.3.2 and illustrated in Fig.13.

12.3.1 WAKE-UP USING INT2 TO INT9

If any of the interrupts INT2 to INT9 are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

12.3.2 WAKE-UP USING RST

To wake-up the P83CL78x, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

12.4 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 4. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor 'p1'; see Fig.9(a).

Table 4 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

12.5 Power Control Register (PCON)

The reduced power modes are activated by software using this Special Function Register. PCON is not bit addressable.

Table 5 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	–	GF1	GF0	PD	IDL

Table 6 Description of PCON bits

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Double Baud rate bit. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
PCON.6	–	Reserved
PCON.5	–	Reserved
PCON.4	–	Reserved
PCON.3	GF1	General purpose flag bit
PCON.2	GF0	General purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates the Power-down mode; see note 1.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode; see note 1.

Note

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

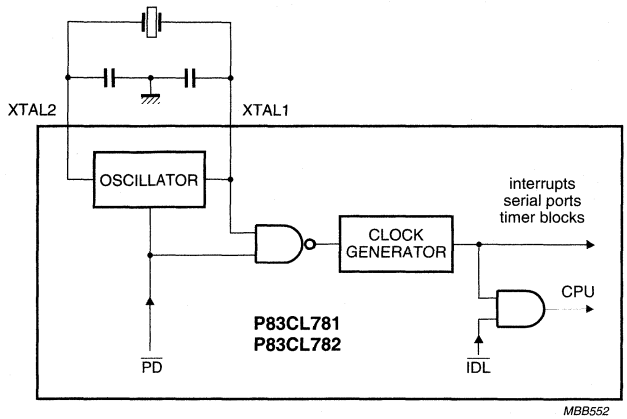


Fig.12 Internal clock control in Idle and Power-down modes.

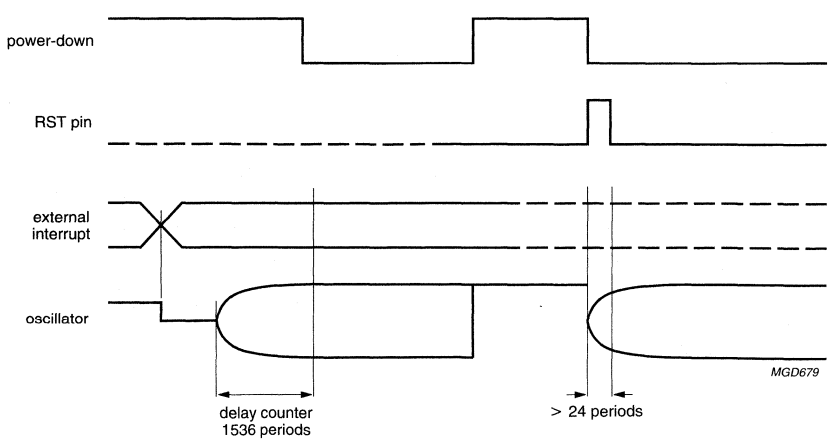


Fig.13 Wake-up operation.

13 I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus, which consists of a serial data line (SDA) and a serial clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the Serial Control Register S1CON. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR is the Slave Address Register. Slave address recognition is performed by on-chip hardware.

Figure 14 is the block diagram of the I²C-bus serial I/O.

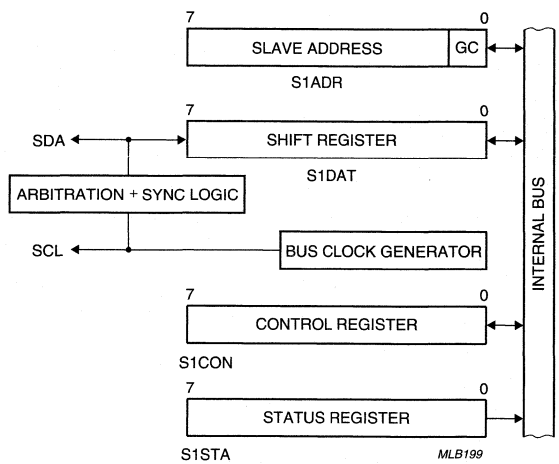


Fig.14 Block diagram of I²C-bus serial I/O.

13.1 Serial Control Register (S1CON)

Table 7 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 8 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
7	CR2	This bit along with bits CR1 (S1CON.1) and CR0 (S1CON.0) determines the serial clock frequency when SIO is in the Master mode. See Table 9.
6	ENS1	**ENABLE serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
5	STA	**START flag**. When this bit is set in Slave mode, the SIO hardware checks the status of the I²C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
4	STO	**STOP flag**. With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I²C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I²C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while GC (S1ADR.0) = 1 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A Stop or Start condition is received as selected slave receiver or transmitter.
2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received; GC (S1ADR.0) = 1 • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
1	CR1	These two bits along with the CR2 (S1CON.7) bit determine the serial clock frequency when SIO is in the Master mode. See Table 9.
0	CR0	

Table 9 Selection of the serial clock frequency SCL in a Master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) AT f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100.0
1	1	0	60	59.7	100.0	–
1	1	1	not allowed	–	–	–

13.2 Serial Status Register (S1STA)

S1STA is a read-only register.The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given in Tables 12 to 16.

Table 10 Serial Status Register (address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 11 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
3 to 7	SC4 to SC0	5-bit status code.
0 to 2	–	These three bits are always zero.

Table 12 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 13 MST/REC mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
38H	Arbitration lost while returning $\overline{ACK}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{ACK}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{ACK}$ returned.

Table 14 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{ACK}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 15 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{ACK}$ received.
C8H	Last DATA byte has been transmitted (AA = 0), ACK received.

Table 16 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.
F8H	No relevant state information available, SI = 0.

Table 17 Symbols used in Tables 12 to 16

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit is logic 0)
$\overline{ACK}$	No acknowledgement (acknowledge bit is logic 1)
DATA	8-bit data byte to or from I²C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

13.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. The MSB (bit 7) is transmitted or received first; i.e. data shifted from right to left.

Table 18 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

13.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 19 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 20 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	Own slave address.
0	GC	This bit is used to determine whether the general call address is recognized. When GC = 0, the general call address is not recognized; when GC = 1, the general call address is recognized.

14 STANDARD SERIAL INTERFACE SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted/received (LSB first). The baud rate is fixed at $1/12 \times f_{osc}$.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of a logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64 \times f_{osc}$.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

14.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

14.2 Serial Port Control and Status Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 21 Serial Port Control Register (address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 22 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
7	SM0	These bits are used to select the serial port mode; see Table 23.
6	SM1	
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be a logic 0.
4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (except see SM2). Must be cleared by software.

Table 23 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	Mode 0	Shift register	$1/12 \times f_{osc}$
0	1	Mode 1	8-bit UART	variable
1	0	Mode 2	9-bit UART	$1/32$ or $1/64 \times f_{osc}$
1	1	Mode 3	9-bit UART	variable

14.3 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as:

$$\text{Baud Rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON and may be calculated as:

$$\text{Baud Rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

- If SMOD = 0 (value on reset), the baud rate is $1/64 \times f_{osc}$
- If SMOD = 1, the baud rate is $1/32 \times f_{osc}$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

14.3.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the Baud Rate Generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow Rate.}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either 'timer' or 'counter' operation in any of its 3 running modes. In most typical applications, it is configured for 'timer' operation, in the Auto-reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{\{12 \times (256 - TH1)\}}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 24 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 24 Commonly used baud rates generated by Timer 1

BAUD RATE (kb/s)	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
1000.0(1)	12.000	X(2)	X	X	X
375.0(3)	12.000	1	X	X	X
62.5(4)	12.000	1	0	Mode 2	FFH
19.2	11.059	1	0	Mode 2	FDH
9.6	11.059	0	0	Mode 2	FDH
4.8	11.059	0	0	Mode 2	FAH
2.4	11.059	0	0	Mode 2	F4H
1.2	11.059	0	0	Mode 2	E8H
137.5	11.986	0	0	Mode 2	1DH
110.0	6.000	0	0	Mode 2	72H
110.0	12.000	0	0	Mode 1	FEEBH

Notes

1. Maximum in Mode 0.
2. X = don't care.
3. Maximum in Mode 2.
4. Maximum in Modes 1 and 3.

14.3.2 Using Timer 2 to generate baud rates

Timer 2 is selected as a Baud Rate Generator by setting the RTCLK bit in T2CON. The Baud Rate Generator mode is similar to the Auto-reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer 2 can be configured for either 'timer' or 'counter' operation. In the most typical applications, it is configured for 'timer' operation ($C/\overline{T2} = 0$). 'Timer' operation is slightly different for Timer 2 when it is being used as a Baud Rate Generator. Normally, as a timer it would increment every machine cycle at a frequency of $^1/_{12} \times f_{osc}$. However, as a Baud Rate Generator it increments every state time at a frequency of $^1/_2 \times f_{osc}$. In this case the baud rate in Modes 1 and 3 is determined as:

$$\text{Baud Rate} = \frac{f_{osc}}{32 \times \{65536 - (\text{RCAP2H; RCAP2L})\}}$$

Where (RCAP2H; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Baud Rate Generator mode for Timer 2 is shown in Fig.15. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the Baud Rate Generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2, TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the Baud Rate Generator mode, registers TH2 and TL2 should not be accessed (read or write). Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The registers RCAP2H and RCAP2L however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 or RCAP2H/RCAP2L should first be turned off by clearing the TR2 bit.

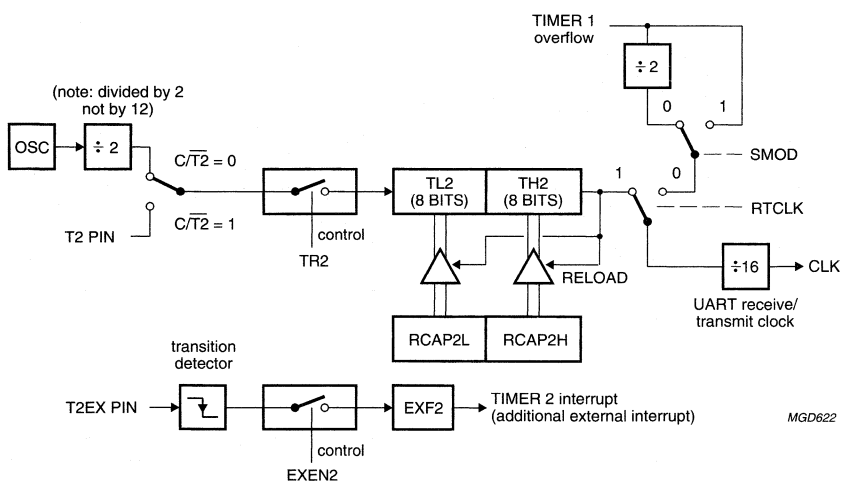


Fig.15 Timer 2 in Baud Rate Generator mode.

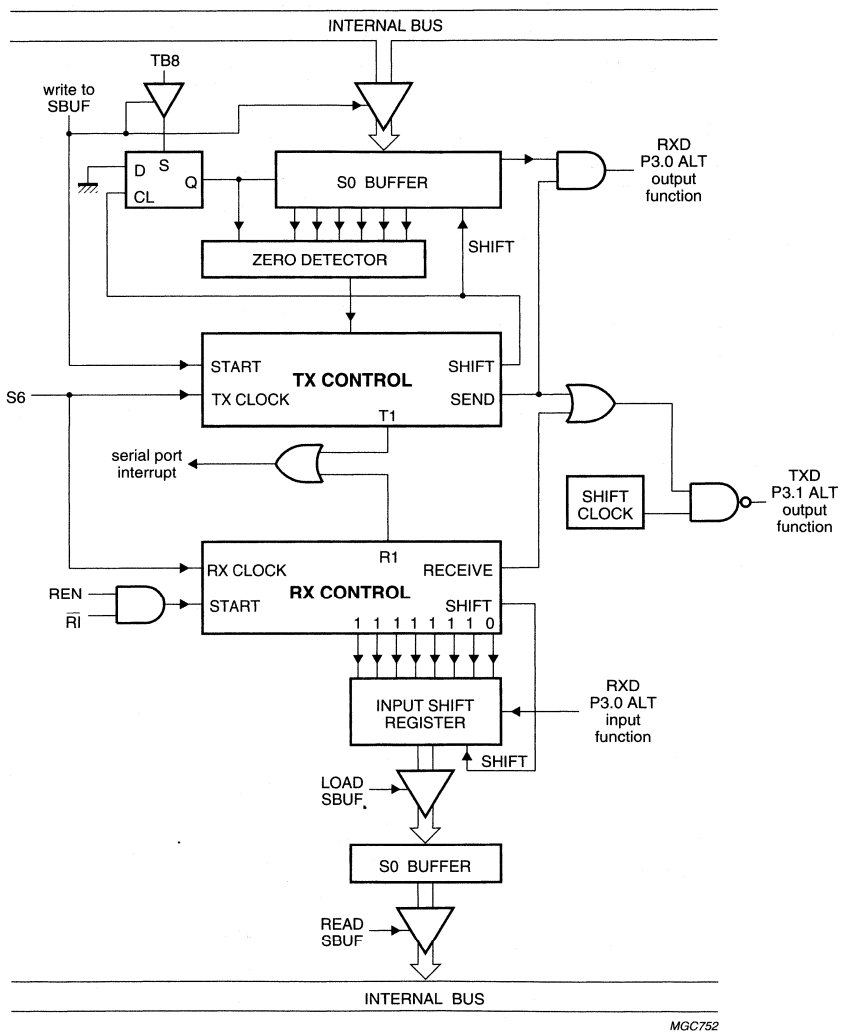


Fig.16 Serial port Mode 0.

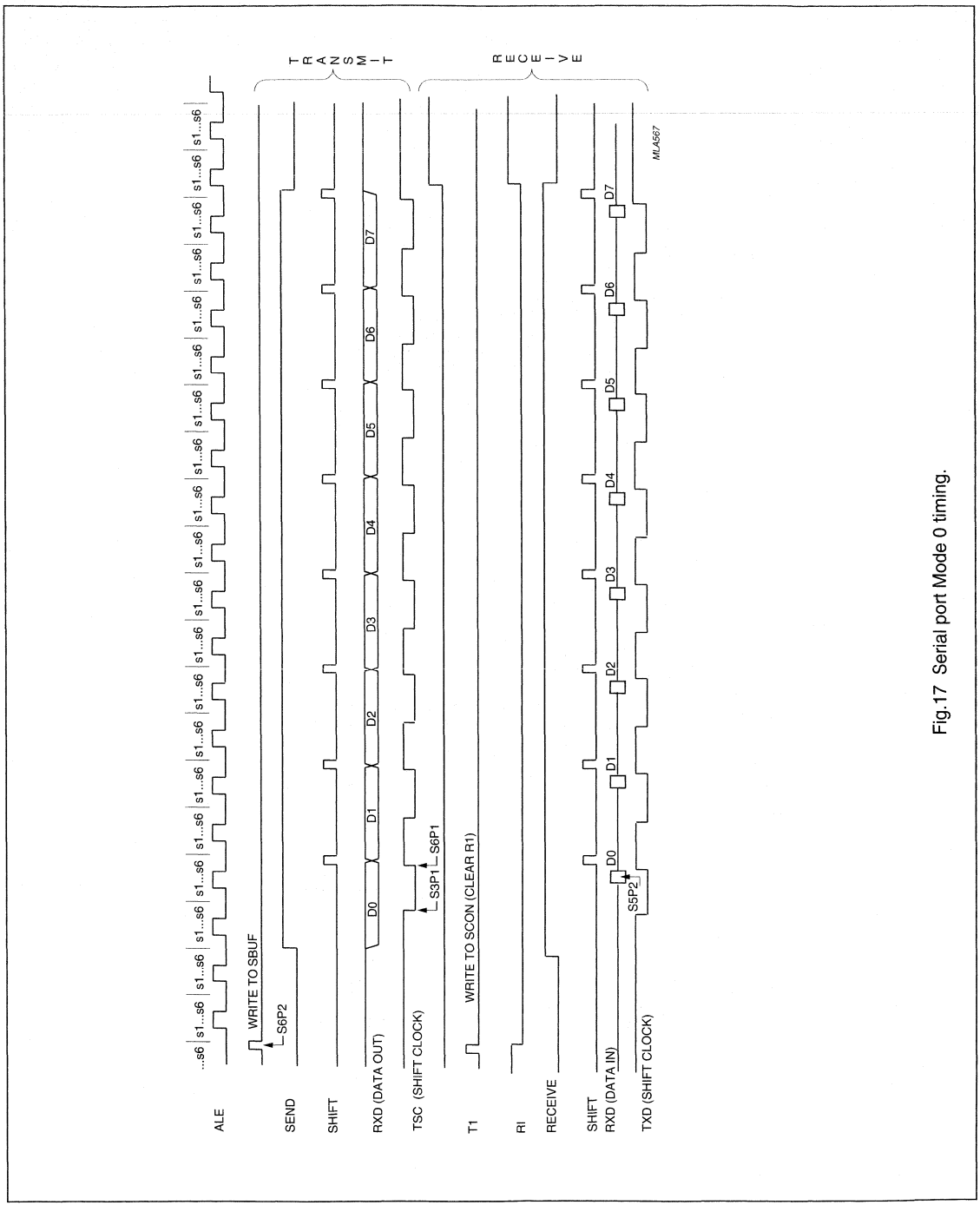


Fig.17 Serial port Mode 0 timing.

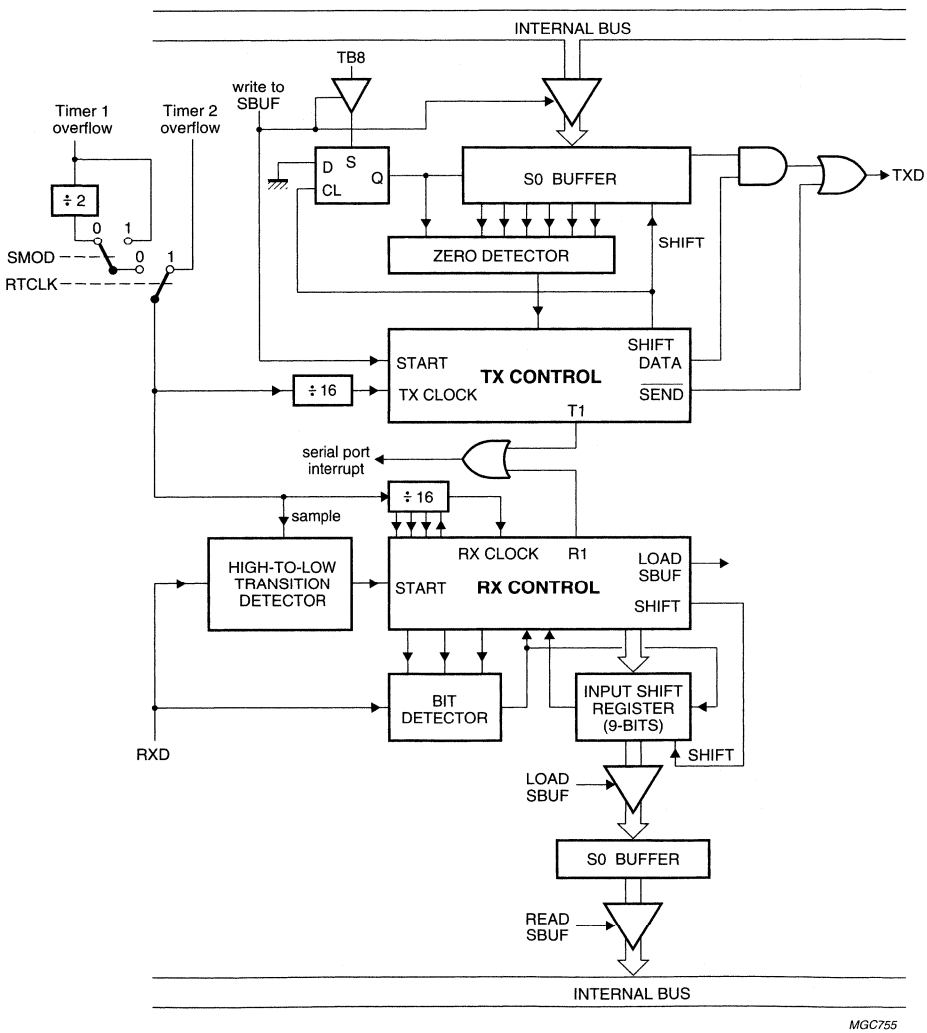


Fig.18 Serial port Mode 1.

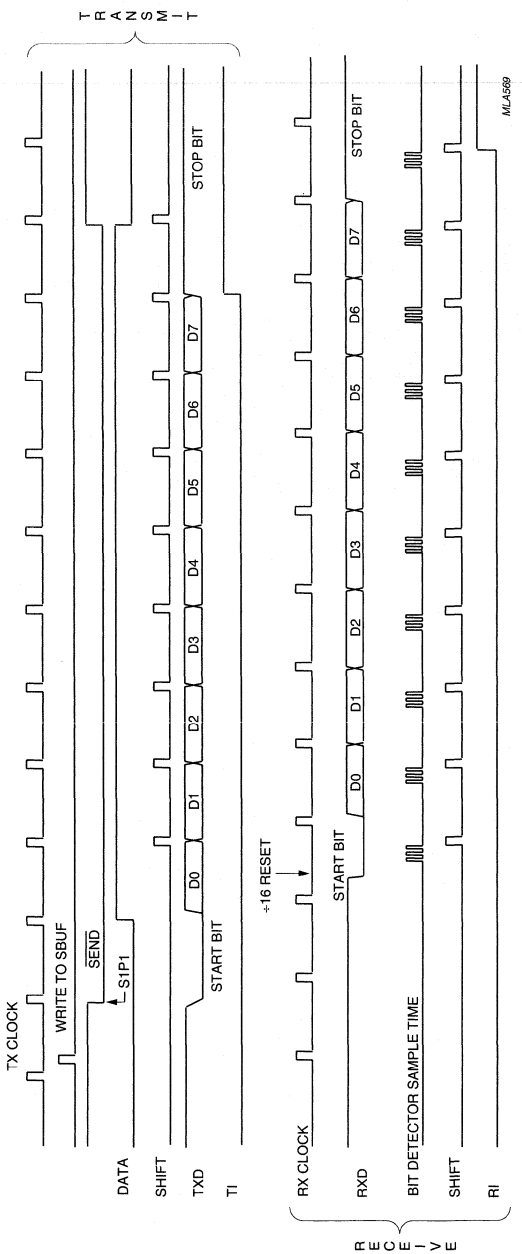


Fig.19 Serial port Mode 1 timing.

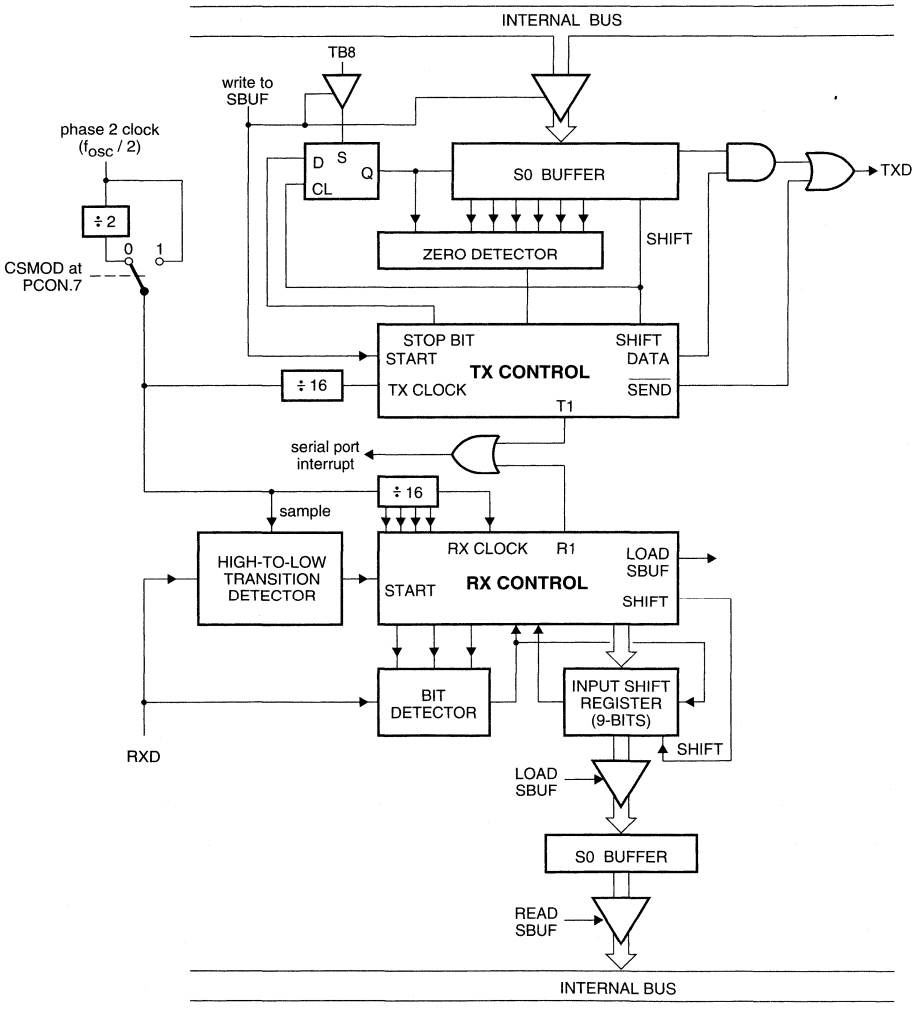


Fig.20 Serial port Mode 2.

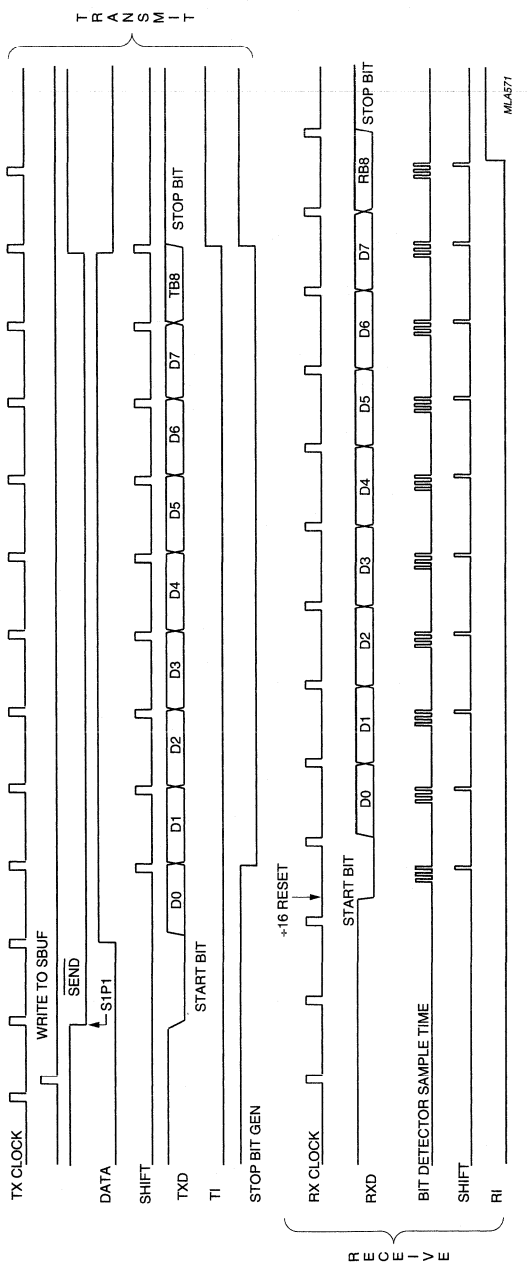


Fig.21 Serial port Mode 2 timing.

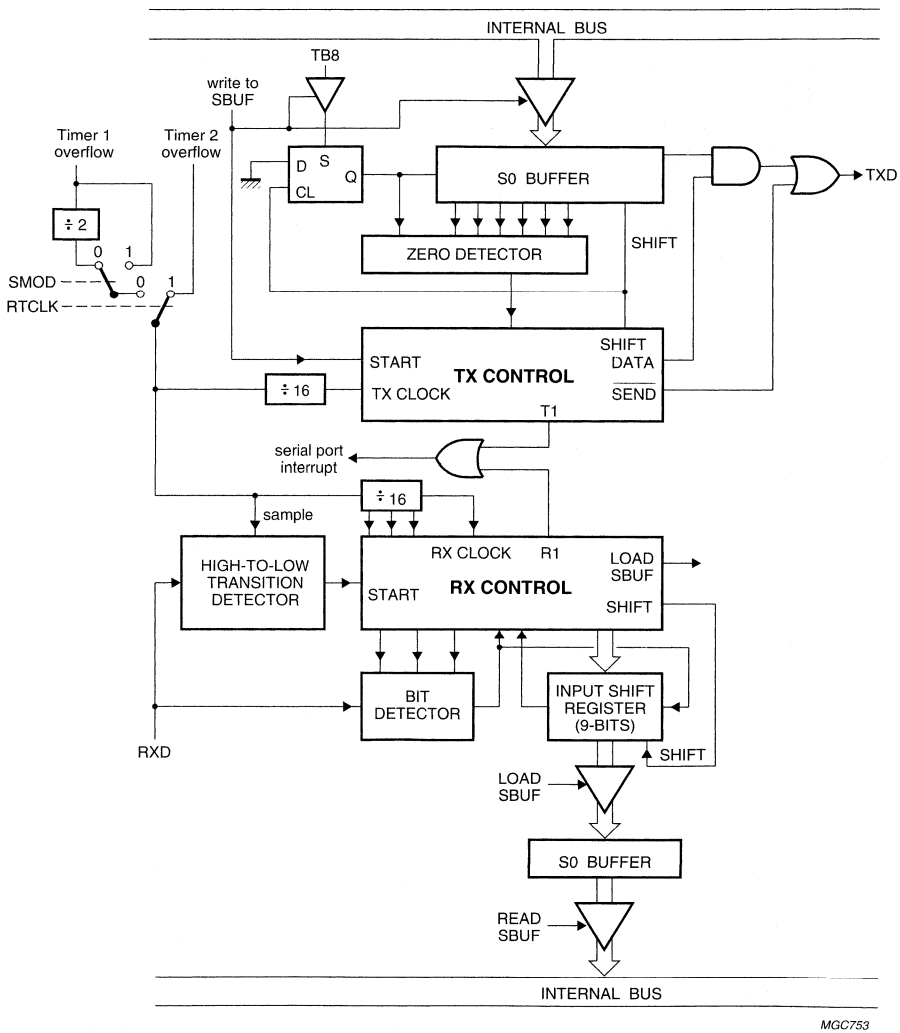


Fig.22 Serial port Mode 3.

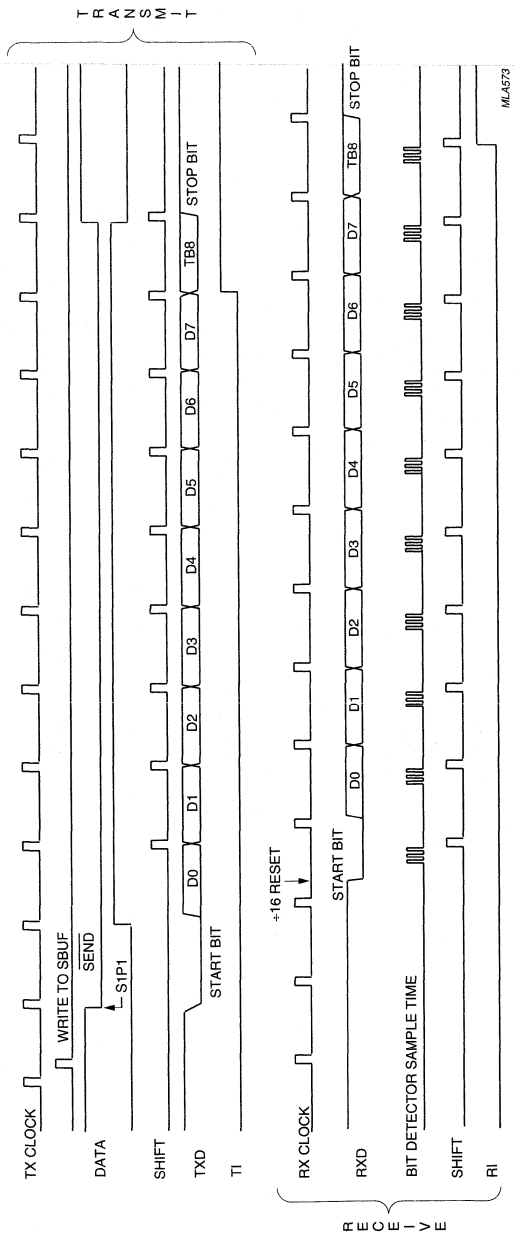


Fig.23 Serial port Mode 3 timing.

15 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU at unpredictable times. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The system is shown in Fig.24. The P83CL78x acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT9
- Timer 0, Timer 1 and Timer 2
- I²C-bus serial I/O
- UART.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

15.1 External interrupts INT2 to INT9

Port 1 lines serve an alternative purpose as eight additional interrupts INT2 to INT9. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level-sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 25 shows the external interrupt system.

15.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If a low priority interrupt is received simultaneously with a high priority interrupt, the high priority interrupt will be dealt with first.

If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to the sequence shown in Table 25 and in Fig.24. The 'vector address' is the ROM location where the appropriate interrupt service routine starts.

Table 25 Interrupt vector polling sequence

SYMBOL	VECTOR ADDRESS (HEX)	SOURCE
X0 (first)	0003	External 0
S1	002B	I²C port
X5	0053	External 5
T0	000B	Timer 0
T2	0033	Timer 2
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
SO	0023	UART
X4	004B	External 4
X9 (last)	0073	External 9

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

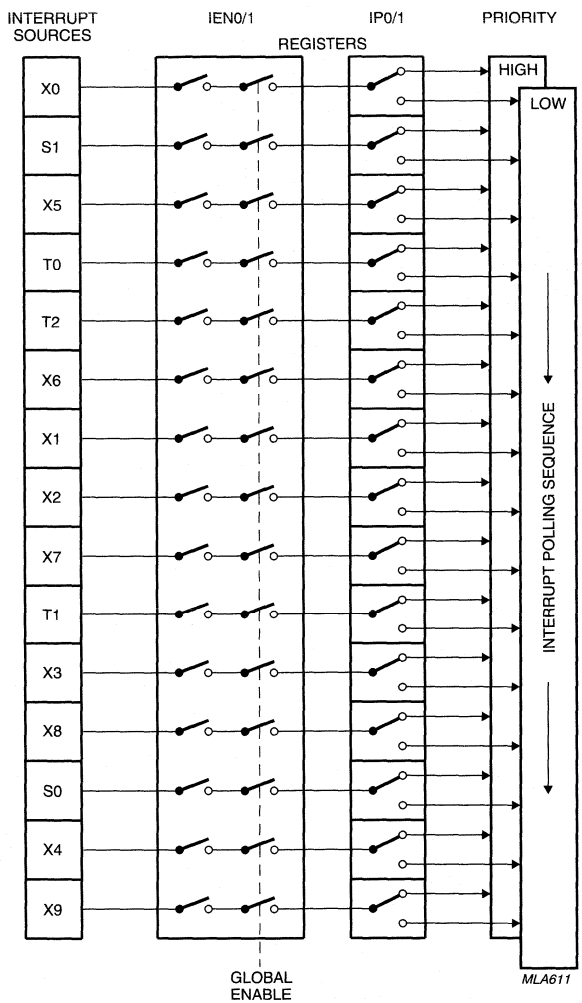


Fig.24 Interrupt system.

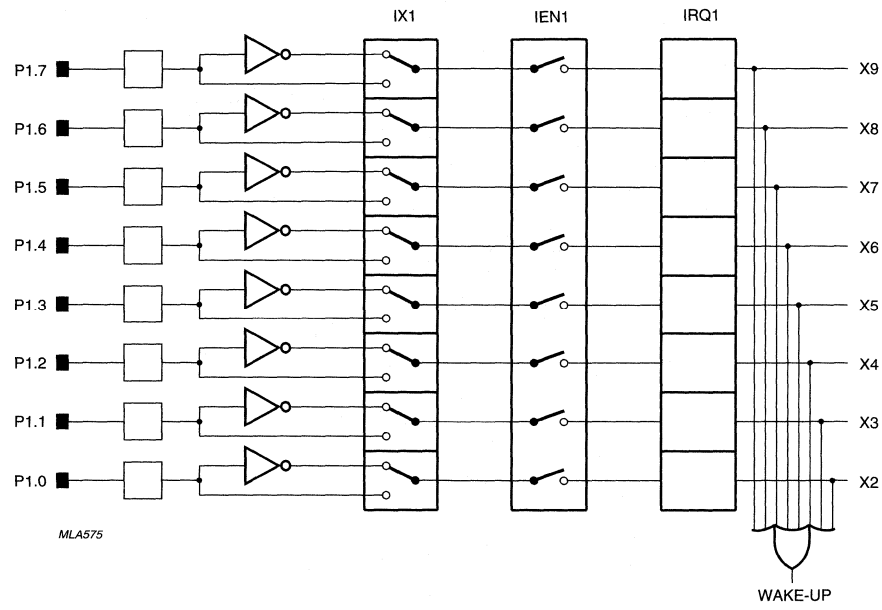


Fig.25 External interrupt configuration.

15.3 Interrupt registers

The registers used in the interrupt system are listed in Table 26. Tables 27 to 38 describe the contents of these registers.

Table 26 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register (INT2 to INT9)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register (INT2 to INT9)
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

15.3.1 Interrupt Enable Register (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 27 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 28 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
6	ET2	enable T2 interrupt
5	ES1	enable I²C interrupt
4	ES0	enable UART SIO interrupt
3	ET1	enable Timer 1 interrupt (T1)
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt (T0)
0	EX0	enable external interrupt 0

15.3.2 Interrupt Enable Register (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 29 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 30 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EX9	enable external interrupt 9
6	EX8	enable external interrupt 8
5	EX7	enable external interrupt 7
4	EX7	enable external interrupt 6
3	EX5	enable external interrupt 5
2	EX4	enable external interrupt 4
1	EX3	enable external interrupt 3
0	EX2	enable external interrupt 2

15.3.3 Interrupt Priority Register (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 31 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 32 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	PT2	Timer 2 interrupt priority level
5	PS1	I²C interrupt priority level
4	PS0	UART SIO interrupt priority level
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

15.3.4 Interrupt Priority Register (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 33 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 34 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PX9	external interrupt 9 priority level
6	PX8	external interrupt 8 priority level
5	PX7	external interrupt 7 priority level
4	PX6	external interrupt 6 priority level
3	PX5	external interrupt 5 priority level
2	PX4	external interrupt 4 priority level
1	PX3	external interrupt 3 priority level
0	PX2	external interrupt 2 priority level

15.3.5 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 35 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 36 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	IL9	external interrupt 9 polarity level
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

15.3.6 Interrupt Request Flag Register (IRQ1)

Table 37 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 38 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	IQ9	external interrupt 9 request flag
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

16 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCL580 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.26. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 39 and Fig.26).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.26.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.26(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 40 and shown in Fig.26. The required option should be stated when ordering.

Table 39 Oscillator options

OPTION	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.26(c).
Oscillator 2	Low-power, low-frequency operations using LC components; see Fig.26(e).
Oscillator 3	Medium frequency range applications.
Oscillator 4	High frequency range applications.
RC oscillator	RC oscillator configuration; see Figs 26(g) and 28.

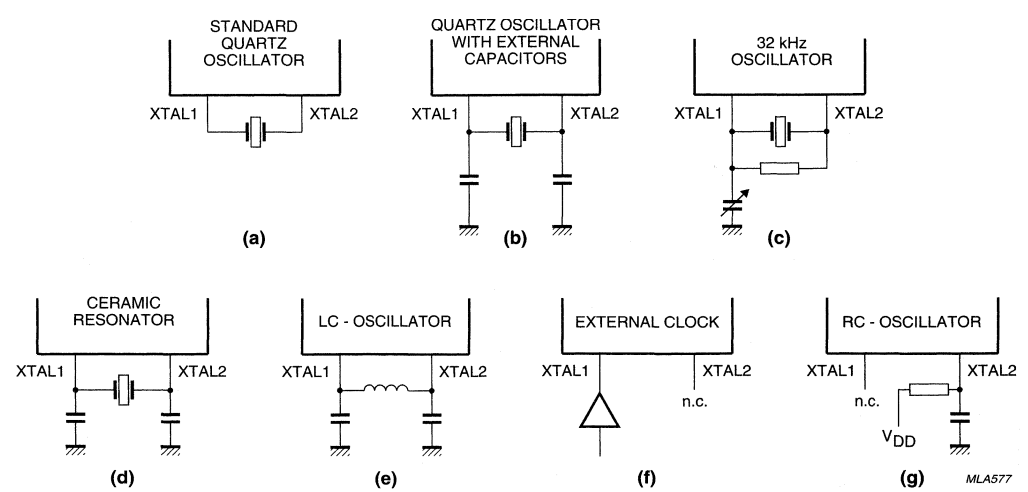


Fig.26 Oscillator configurations.

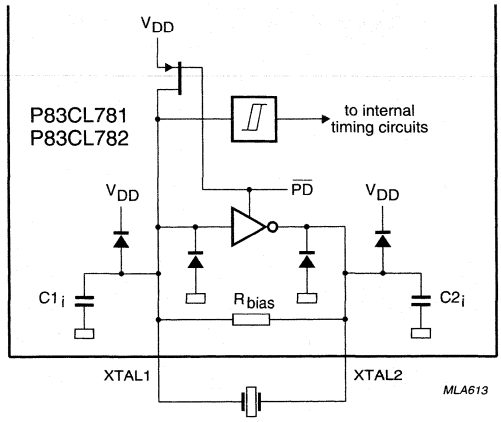
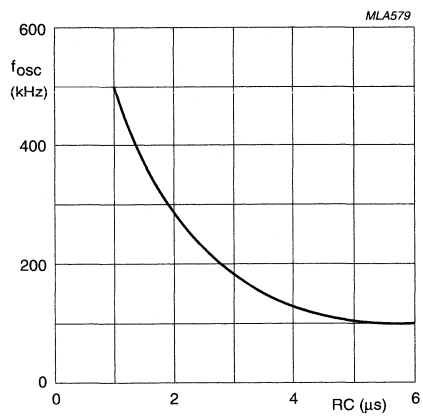


Fig.27 Standard oscillator.



RC oscillator frequency is externally adjustable; 100 kHz ≤ f_{osc} ≤ 500 kHz.

Fig.28 RC oscillator; frequency as a function of RC.

Table 40 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 39)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ; note 1
	1.0	Oscillator 2	0	30	0	30	600 Ω
	3.58		0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0	Oscillator 4	0	15	0	15	60 Ω
	12.0		0	10	0	10	40Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455	Oscillator 2	40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58		0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC		Oscillator 2	20	90	20	90	10 μH = 1 Ω 100 μH = 5 Ω 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

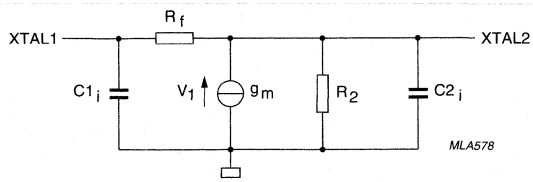


Fig.29 Oscillator equivalent circuit diagram.

Table 41 Oscillator equivalent circuit parameters

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Oscillator 1; 32 kHz	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
		Oscillator 2		200	600	1000	µS
		Oscillator 3		400	1500	4000	µS
		Oscillator 4		1000	4000	10000	µS
$C1_i$	input capacitance	Oscillator 1; 32 kHz		–	3.0	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
$C2_i$	output capacitance	Oscillator 1; 32 kHz		–	23	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
R2	output resistance	Oscillator 1; 32 kHz		–	3800	–	kΩ
		Oscillator 2		–	65	–	kΩ
		Oscillator 3		–	18	–	kΩ
		Oscillator 4		–	5.0	–	kΩ

17 RESET

To initialize the P83CL78x a reset is performed by either of two methods:

- Applying an external signal to the RST pin
- Via Power-on reset circuitry.

The reset state of the port pins is mask-programmable and can be defined by the user. The standard reset value for Ports 0 to 3 is FFH. A reset leaves the internal registers as shown in Chapter 18.

17.1 External reset using the RST pin

The reset input for the P83CL78x is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

17.2 Power-on reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation. See Fig.32.

The on-chip Power-on reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on reset circuitry is shown in Fig.31.

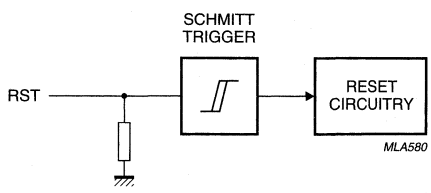


Fig.30 Reset configuration.

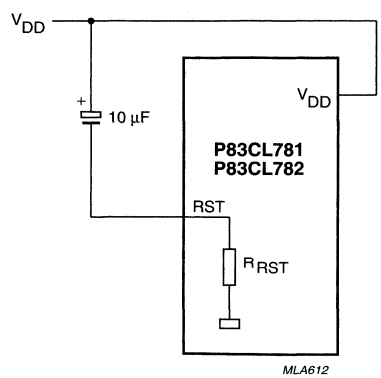


Fig.31 Power-on reset circuitry.

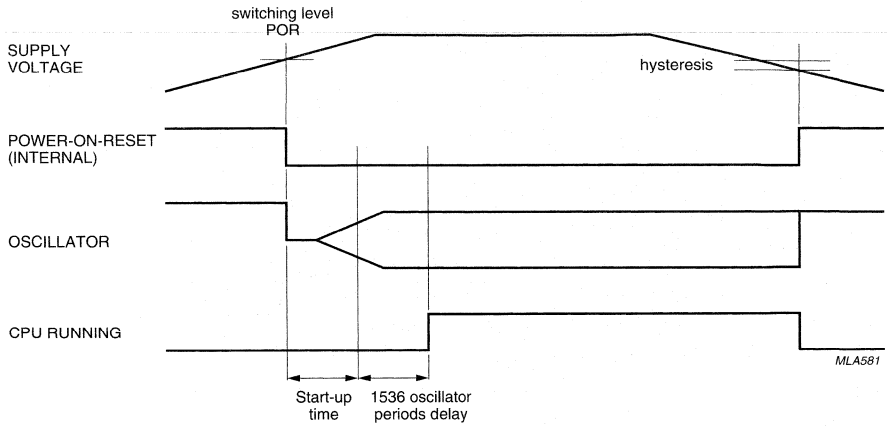


Fig.32 Power-on reset switching level.

18 SPECIAL FUNCTION REGISTERS OVERVIEW

The P83CL78x has 34 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
F8	IP1[1]	00000000	Interrupt Priority Register (INT2 to INT9)
F0	B[1]	00000000	B Register
E9	IX1	00000000	Interrupt Polarity Register
E8	IEN1[1]	00000000	Interrupt Enable Register 1
E0	ACC[1]	00000000	Accumulator
DB	S1ADR	00000000	I²C-bus Slave Address Register
DA	S1DAT	00000000	I²C-bus Data Shift Register
D9	S1STA	11111000	I²C-bus Serial Status Register
D8	S1CON[1]	00000000	I²C-bus Serial Control Register
D0	PSW[1]	00000000	Program Status Word
CD	TH2	00000000	Timer 2 High byte
CC	TL2	00000000	Timer 2 Low byte
CB	RCAP2H	00000000	Timer 2 Reload/Capture Register High byte
CA	RCAP2L	00000000	Timer 2 Reload/Capture Register Low byte
C8	T2CON[1]	00000000	Timer/Counter 2 Control Register
C0	IRQ1[1]	00000000	Interrupt Request Flag Register
B8	IP0[1]	X0000000	Interrupt Priority Register 0
B0	P3[1]	XXXXXXXX[2]	Digital I/O Port Register 3
A8	IEN0[1]	00000000	Interrupt Enable Register
A0	P2[1]	XXXXXXXX[2]	Digital I/O Port Register 2
99	S0BUF	XXXXXXXX	Serial Data Buffer Register 0
98	S0CON[1]	00000000	Serial Port Control Register 0
90	P1[1]	XXXXXXXX[2]	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON[1]	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	0XX00000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0[1]	XXXXXXXX[2]	Digital I/O Port Register 0

Notes

1. Bit addressable register.
2. Port reset state determined by the customer.

19 INSTRUCTION SET

The P83CL78x uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 46.

Table 42 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 43 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 44 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 45 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 46 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	111-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 47 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	1	MOV direct,Rr 0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	1	SUB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	1	MOV Rr,direct 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	1	CJNE Rr,#data,rel 0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	1	DJNZ Rr,rel 0	1	2	3	4	5	6	7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV direct,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

Note

1. MOV A, ACC is not a valid instruction.

20 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
I_I	DC current on any input	−5.0	+5.0	mA
I_O	DC current on any output	−5.0	+5.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature - P83CL781	−40	+85	°C
	operating ambient temperature - P83CL782	−25	+55	°C
T_j	operating junction temperature	–	+125	°C

21 DC CHARACTERISTICS

The DC characteristics apply to both the P83CL781 and the P83CL782 unless otherwise stated. V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C for the P83CL781 and −25 to +55 °C for the P83CL782; all voltages with respect to V_{SS} unless otherwise specified. See notes 1, 2 and 3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	–	6.0	V
V_{DD}	RAM retention voltage in Power-down mode		1.0	–	6.0	V
I_{DD}	supply current operating; P83CL781	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 4	–	17	25	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	2.4	5	mA
	supply current operating; P83CL782	V_{DD} = 3.1 V; f_{CLK} = 12 MHz; note 4	–	8.4	12	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	2.4	5	µA
$I_{DD(idle)}$	supply current Idle mode; P83CL781	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 5	–	5.1	12	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 5	–	0.75	3	mA
	supply current Idle mode; P83CL782	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 5	–	2.7	5	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 5	–	0.75	3	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 6	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage	note 7	V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 7	$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	LOW level input current	V_{DD} = 5 V; V_{IN} = 0.4 V; note 7	–	–	–100	µA
		V_{DD} = 2.5 V; V_{IN} = 0.4 V; note 7	–	–	–50	µA
$I_{IL(T)}$	LOW level input current (HIGH-to-LOW transition)	V_{DD} = 5 V; V_{IN} = $0.5V_{DD}$; note 7	–	–	–1.0	mA
		V_{DD} = 2.5 V; V_{IN} = $0.5V_{DD}$; note 7	–	–	–500	µA
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$; note 7	–	–	±10	µA
Outputs						
I_{OL}	LOW level output current; except SDA and SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	–	–	mA
I_{OL1}	LOW level output current; SDA and SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
I_{OH}	HIGH level output current (push-pull options only)	V_{DD} = 5 V; V_{OH} = V_{DD} – 0.4 V	–1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} – 0.4 V	–0.7	–	–	mA
R_{RST}	RST pull-down resistor		10	–	200	kΩ

Notes

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these make a HIGH-to-LOW transition during bus operations. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse conditions (capacitive loading >100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
2. Capacitive loading on Ports 0 and 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9% of V_{DD} specification when the address bits are stabilizing.
3. Circuits with Power-on reset option 'OFF' are tested at V_{DDmin} = 1.8 V; with the 'ON' option (typically 1.3 V) they are tested at V_{DDmin} = 2.3 V.
4. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ =10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
5. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
6. The Power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
7. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I²C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.

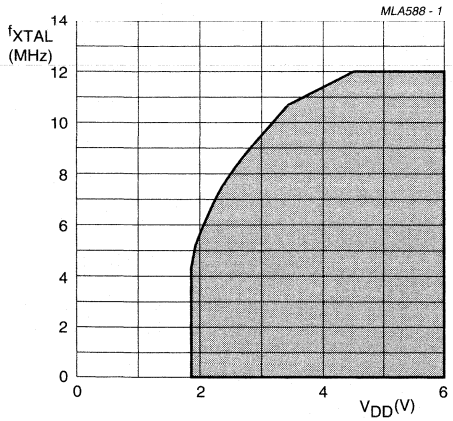


Fig.33 Frequency operating range - P83CL781.

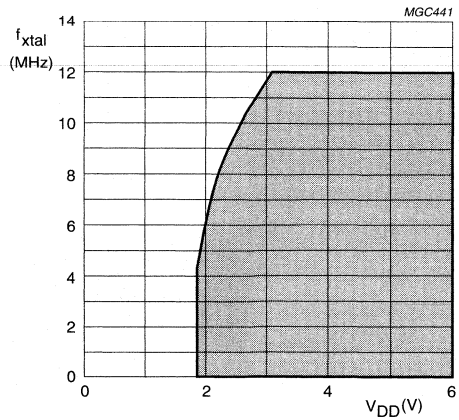
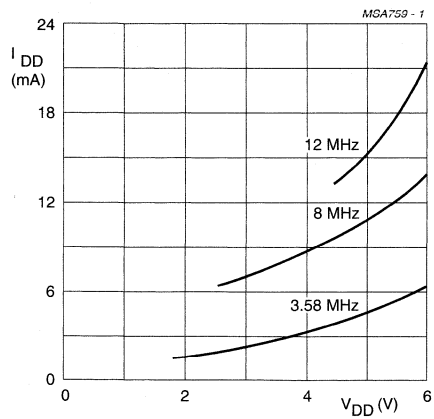
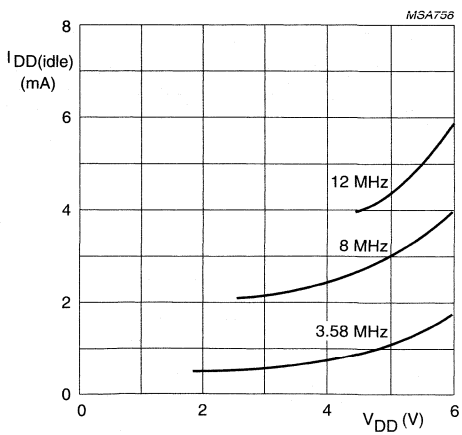


Fig.34 Frequency operating range - P83CL782.



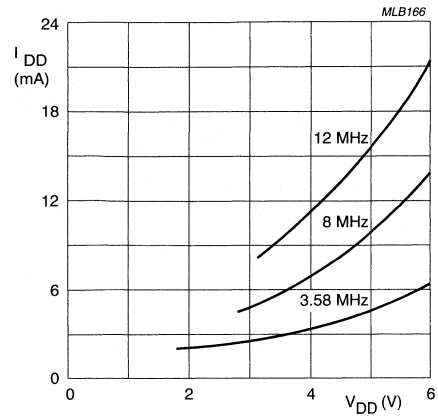
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.35 P83CL781: typical operating current as a function of frequency and V_{DD}.



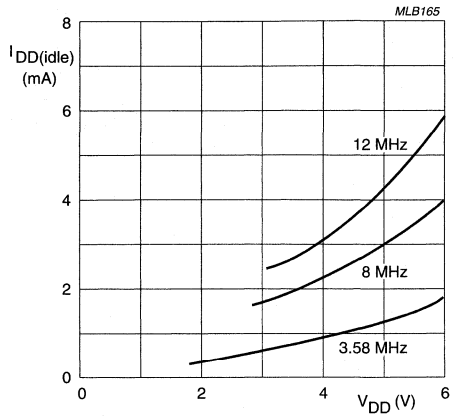
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.36 P83CL781: typical Idle current as a function of frequency and V_{DD}.



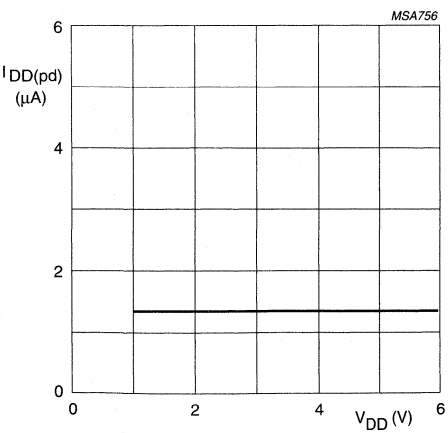
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.37 P83CL782: typical operating current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.38 P83CL782: typical Idle current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.

Fig.39 Typical Power-down current as a function of V_{DD}.

22 AC CHARACTERISTICS

The following AC characteristics apply to both the P83CL781 and P83CL782 unless otherwise stated.

22.1 Program memory

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C for the P83CL781 and −25 to +55 °C for the P83CL782; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless specified. See Fig.40.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{LL}	ALE pulse duration	127	–	$2t_{CK} - 40$	–	ns
t_{AL}	Address set-up time to ALE	43	–	$t_{CK} - 40$	–	ns
t_{LA}	Address hold time after ALE	48	–	$t_{CK} - 35$	–	ns
t_{LIV}	Time from ALE to valid instruction input	–	233	–	$4t_{CK} - 100$	ns
t_{LC}	Time from ALE to control pulse $\overline{PSEN}$	58	–	$t_{CK} - 25$	–	ns
t_{CC}	Control pulse duration $\overline{PSEN}$	215	–	$3t_{CK} - 35$	–	ns
t_{CIV}	Time from $\overline{PSEN}$ to valid instruction input	–	125	–	$3t_{CK} - 125$	ns
t_{CI}	Input instruction hold time after $\overline{PSEN}$	0	–	0	–	ns
t_{CIF}	Input instruction float delay after $\overline{PSEN}$	–	63	–	$t_{CK} - 20$	ns
t_{AC}	Address valid after $\overline{PSEN}$	75	–	$t_{CK} - 8$	–	ns
t_{AIV}	Address to valid instruction input	–	302	–	$5t_{CK} - 115$	ns
t_{AFC}	Address float delay after $\overline{PSEN}$	12	–	0	–	ns

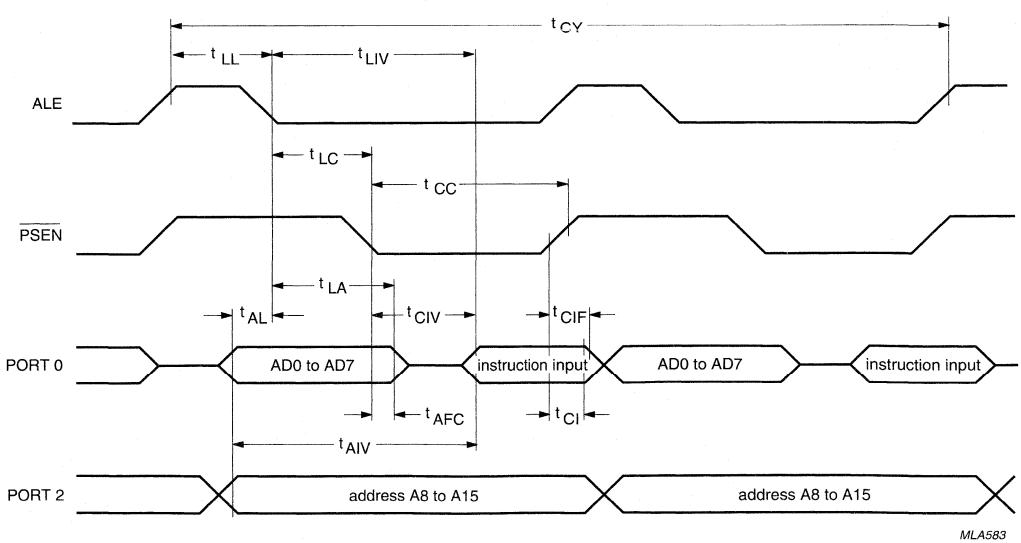


Fig.40 Read from Program Memory.

22.2 External Data Memory

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C for P83CL781 and −25 to +55 °C for the P83CL782; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified. See note 1 and Figs 41 and 42.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RR}	$\overline{RD}$ pulse duration	400	–	$6t_{CK} - 100$	–	ns
t_{WW}	WR pulse duration	400	–	$6t_{CK} - 100$	–	ns
t_{LA}	Address hold time after ALE	48	–	$t_{CK} - 35$	–	ns
$t_{\overline{RD}}$	$\overline{RD}$ to valid data input	–	150	–	$5t_{CK} - 165$	ns
t_{DFR}	Data float delay after $\overline{RD}$	–	97	–	$2t_{CK} - 70$	ns
t_{LD}	Time from ALE to valid data input	–	517	–	$8t_{CK} - 150$	ns
t_{AD}	Address to valid data input	–	585	–	$9t_{CK} - 165$	ns
t_{LW}	Time from ALE to $\overline{RD}$ or $\overline{WR}$	200	300	$3t_{CK} - 50$	$3t_{CK} + 50$	ns
t_{AW}	Time from address to $\overline{RD}$ or $\overline{WR}$	203	–	4	–	ns
t_{WHLH}	Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	$t_{CK} - 40$	$t_{CK} + 40$	ns
t_{DWX}	Data valid to $\overline{WR}$ transition	23	–	$t_{CK} - 60$	–	ns
t_{DW}	Data set-up time before $\overline{WR}$	433	–	$7t_{CK} - 150$	–	ns
t_{WD}	Data hold time after $\overline{WR}$	33	–	$t_{CK} - 50$	–	ns
t_{AFR}	Address float delay after $\overline{RD}$	–	12	–	12	ns

Note

1. Interfacing the P83CL781 or the P83CL782 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

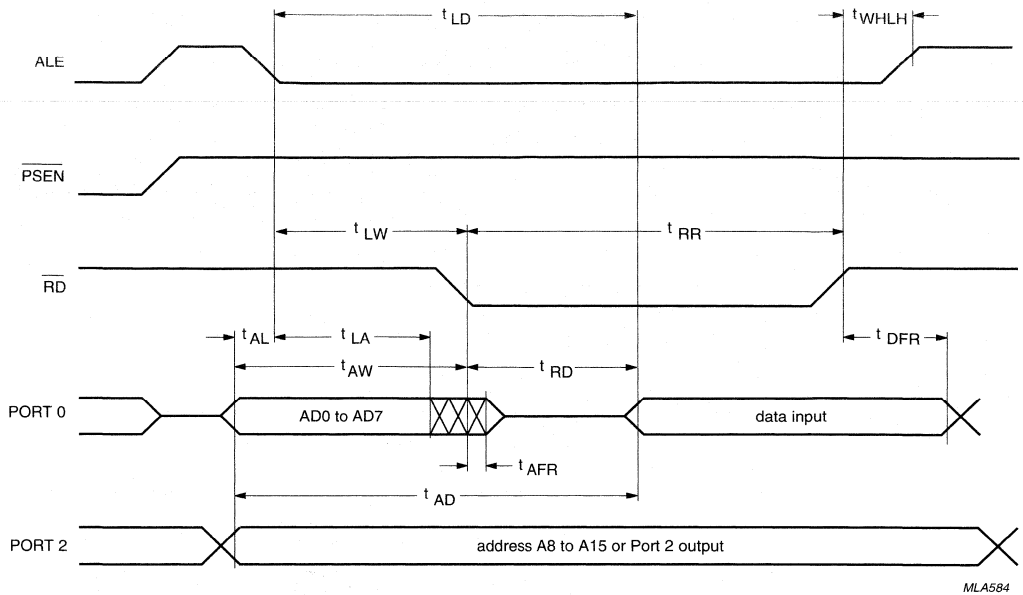


Fig.41 Read from Data Memory.

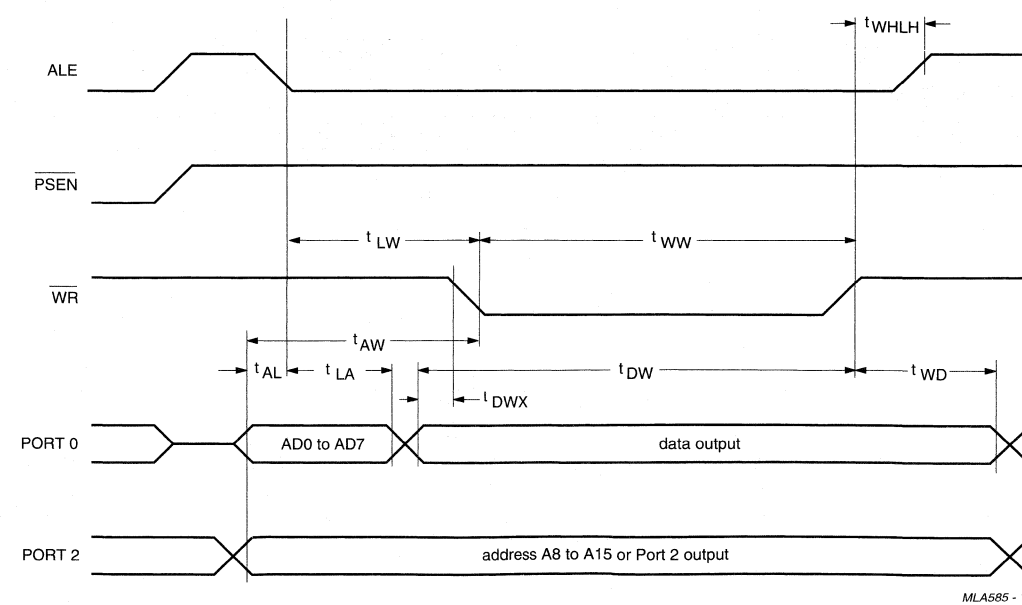


Fig.42 Write to Data Memory.

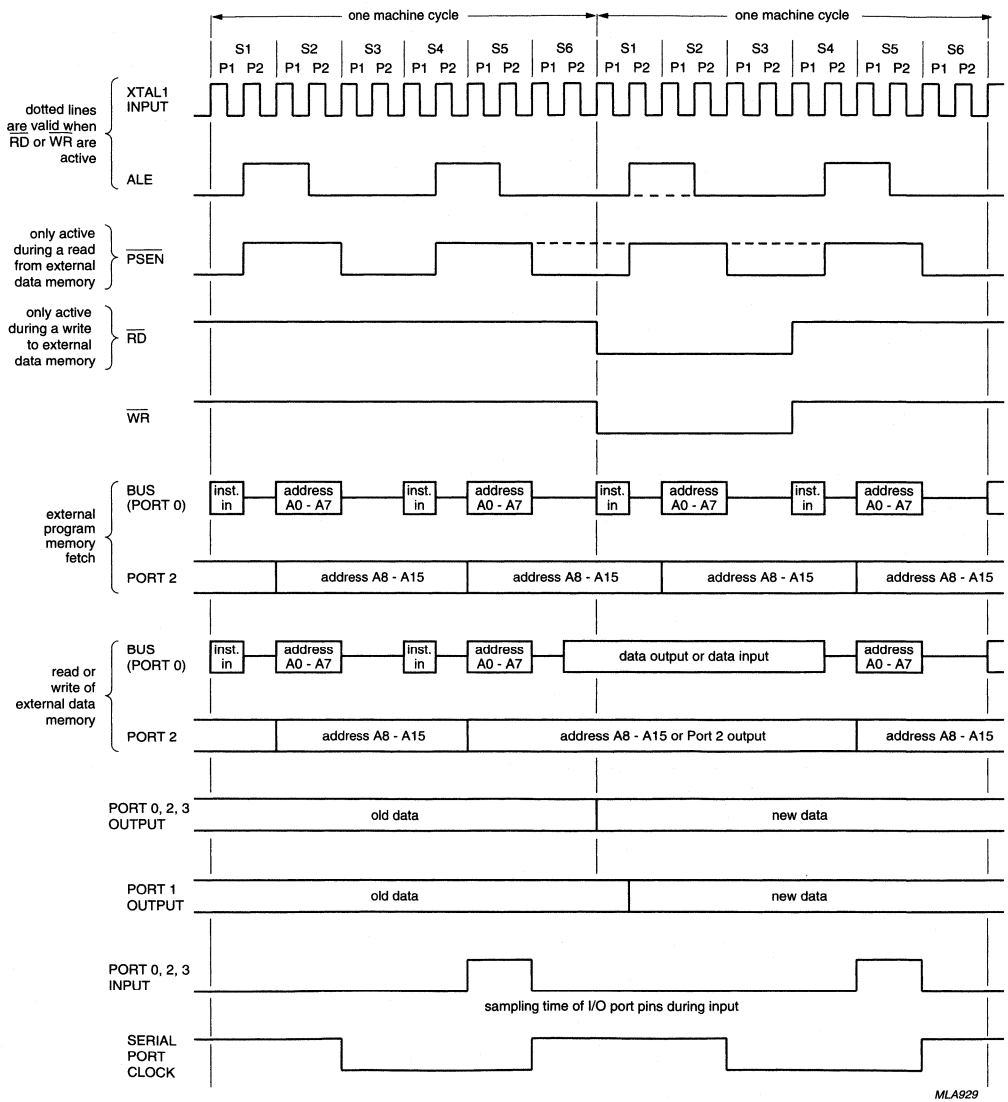


Fig.43 Instruction cycle timing.

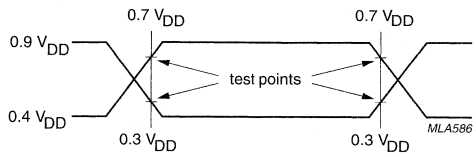


Fig.44 AC testing input waveform.

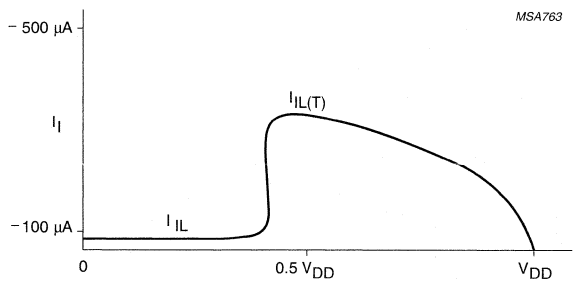


Fig.45 Input current.

CONTENTS

Low-voltage microcontroller with 63-kbyte OTP program memory and 2-kbyte RAM

P87CL881H

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions.
- Very low current consumption
- Single supply voltage of 2.7 to 3.6 V
- Frequency: 1 to 10 MHz
- Operating temperature: –25 to +70 °C
- 44-pin LQFP package
- Four 8-bit ports (32 I/O lines)
- 63-kbyte One-Time Programmable (OTP) program memory; programmable in parallel mode or in-system via I²C-bus interface.
- 256-byte internal RAM
- 1792-byte internal AUX-RAM
- External address range: 64 kbytes of ROM and 64 kbytes of RAM
- Amplitude Controlled Oscillator (ACO) suitable for use with a quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset circuitry (POR)
- Low Voltage Detection (LVD) with 11 software programmable levels
- 8 interrupts on Port 1, edge or level sensitive triggering selectable via software power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- Two 16-bit timer/event counters
- Additional 16-bit timer/event counters, with capture, compare and PWM function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum operating frequency 400 kHz.

2 GENERAL DESCRIPTION

The P87CL881 is an 8-bit microcontroller especially suited for pager applications.

The P87CL881 is manufactured in an advanced CMOS technology and is based on single chip technology.

The device is optimized for low power consumption and has two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks switch off their clock if they are inactive.

The instruction set of the P87CL881 is based on that of the 80C51. The P87CL881 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

This data sheet details the specific properties of the P87CL881; for details of the P87CL881 core and the derivative functions see the *"TELX family"* data sheet and *"8051-Based 8-bit Microcontrollers; Data Handbook IC20"*.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
P87CL881H/000	Blank OTP	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P87CL881H/xxx	Factory-programmed OTP			

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and options.

4 BLOCK DIAGRAM

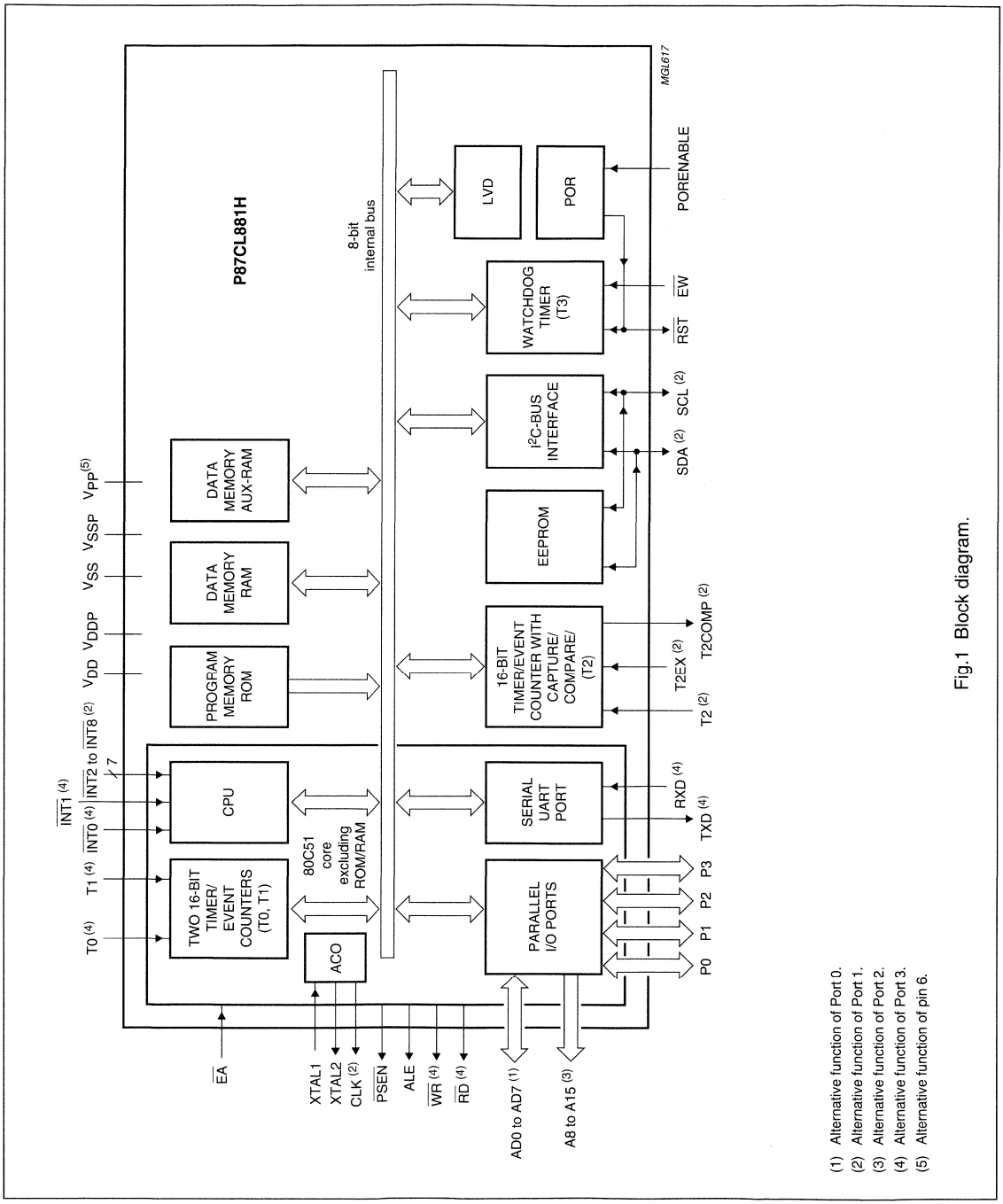


Fig.1 Block diagram.

(1) Alternative function of Port 0.
(2) Alternative function of Port 1.
(3) Alternative function of Port 2.
(4) Alternative function of Port 3.
(5) Alternative function of pin 6.

5 PINNING INFORMATION

5.1 Pinning

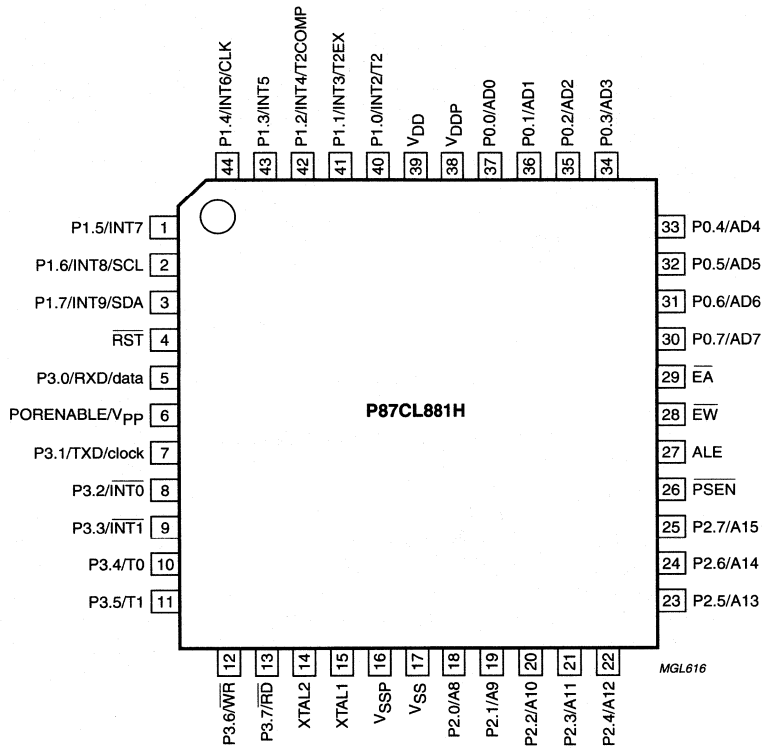


Fig.2 Pin configuration.

5.2 Pin description

Table 1 LQFP package

SYMBOL	PIN	DESCRIPTION
V_{DD}	39	**Power supply** for core.
V_{DDP}	38	**Power supply** for I/O ring.
V_{SS}	17	**Ground** for core.
V_{SSP}	16	**Ground** for I/O ring.
$\overline{RST}$	4	**RESET.** A LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
PORENABLE/V_{PP}	6	**PORENABLE.** If set to a logic 1, the internal Power-on reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE LOW in order to achieve the lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.
$\overline{EW}$	28	Enable Watchdog Timer.
XTAL2	14	**Crystal output.** Output of the amplitude controlled oscillator. If an external oscillator clock is used this pin not used.
XTAL1	15	**Crystal input.** Input to the amplitude controlled oscillator. Also the input for an externally generated clock source.
$\overline{PSEN}$	26	**Program Store Enable.** Read strobe to external program memory. When executing code out of external program memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{PSEN}$ activations are skipped. During Power-down mode the $\overline{PSEN}$ pin stays HIGH.
ALE	27	**Address Latch Enable.** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes. For improved EMC behaviour, the toggle of the ALE pin can be disabled by setting the RFI bit in the PCON register by software. This bit is cleared on reset and can be set and cleared by software. When set, the ALE pin will be pulled-down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE if external memory is accessed. ALE will retain its normal HIGH state during Idle mode and a LOW state during the Power-down mode while in the EMC mode. Additionally, during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the RFI bit is set or not.
$\overline{EA}$	29	**External Access.** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal program memory (unless the program counter exceeds the highest address for internal program memory). When $\overline{EA}$ is held LOW, the CPU executes out of external program memory regardless of the value of the program counter. The state of the $\overline{EA}$ pin is internally latched at reset.

SYMBOL	PIN	DESCRIPTION
P0.0/AD0	37	**Port 0.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory.
P0.1/AD1	36	
P0.2/AD2	35	
P0.3/AD3	34	
P0.4/AD4	33	
P0.5/AD5	32	
P0.6/AD6	31	
P0.7/AD7	30	
P1.0/INT2/T2	40	**Port 1.** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 1 also serves the alternative functions INT2 to INT9 interrupts, Timer 2 external input and Timer 2 compare output, external clock output CLK and I^2C-bus clock and I^2C-bus data in/outputs.
P1.1/INT3/T2EX	41	
P1.2/INT4/ T2COMP	42	
P1.3/INT5	43	
P1.4/INT6/CLK	44	
P1.5/INT7	1	
P1.6/INT8/SCL	2	
P1.7/INT9/SDA	3	
P2.0/A8	18	**Port 2.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 2 emits the high order address byte during accesses to external memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
P2.1/A9	19	
P2.2/A10	20	
P2.3/A11	21	
P2.4/A12	22	
P2.5/A13	23	
P2.6/A14	24	
P2.7/A15	25	
P3.0/RXD/data	5	**Port 3.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous). TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous). $\overline{INT0}$ and $\overline{INT1}$ are external interrupt lines. T0 and T1 are external inputs for Timers 0 and 1 respectively. $\overline{WR}$ is the external memory write strobe and $\overline{RD}$ is the external memory read strobe.
P3.1/TXD/clock	7	
P3.2/$\overline{INT0}$	8	
P3.3/$\overline{INT1}$	9	
P3.4/T0	10	
P3.5/T1	11	
P3.6/$\overline{WR}$	12	
P3.7/$\overline{RD}$	13	

6 FUNCTIONAL DESCRIPTION

For the functional and block descriptions of the P87CL881, refer to the *"TELX family"* data sheet.

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values; note 1

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
XRAM Page Register	XRAMP	FAH	XXXX X000
Timers 0 and 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 output data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 output data Register	P1	90H	0111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0000 1000
Port P1 Configuration B Register	P1CFGB	9FH	0111 1111
Port P2 output data Register	P2	A0H	1111 1111
Port P2 Configuration A Register	P2CFGA	AEH	1111 1111
Port P2 Configuration B Register	P2CFGB	AFH	0000 0000
Port P3 output data Register	P3	B0H	1111 1111
Port P3 Configuration A Register	P3CFGA	BEH	1111 1110
Port P3 Configuration B Register	P3CFGB	BFH	1111 1111

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
PORACO			
Reset Status Register	RSTAT	E6H	XXX1 1000
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I²C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
OTP interface			
OTP Address High Register	OAH	D5	X00X XXXX
OTP Address Low Register	OAL	D4	XXXX XXXX
OTP Data Register	ODATA	D6	XXXX XXXX
OTP In-System Programming Register	OISYS	DC	000X 0000
OTP Test Register	OTEST	D7	0000 0000

Notes

1. E7H and FDH are reserved locations and must not be written to.
2. Where: X = undefined state.

6.2 I/O facilities

6.2.1 PORTS

The P87CL881 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.0/T2 and P1.1/T2EX for external inputs of Timer 2
- P1.2/T2COMP for external activation and compare output of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock which are serial port receiver input and transmitter output (UART)
- P3.2/$\overline{INT0}$ and P3.3/$\overline{INT1}$ are external interrupt request inputs
- P3.4/T0 and P3.5/T1 as counter inputs
- P3.6/$\overline{WR}$ and P3.7/$\overline{RD}$ are control signals to write and read to external memories.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3(a) shows that the strong transistor P1 is turned on for only 1 oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on P3 (a weak pull-up) through the inverter IN1. This inverter and transistor P3 form a latch which holds the logic 1.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. Each port has two associated SFRs: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins.
For example, the output type of P1.3 is controlled by setting bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via the SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}).

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output (e.g. Port 0 for external memory accesses ($\overline{EA}$ = 0) or access above the built-in memory boundary) requires the connection of an external pull-up resistor. The ESD protection diodes against V_{DD} and V_{SS} are still present. Except for the I^2C-bus pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}. See Fig.3a.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up p1 is turned on for only one oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through p2 and 'very weakly' driven through p3. See Fig.3b.

Mode 2 High-impedance; this mode turns all port output drivers off. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome. See Fig.3c.

Mode 3 Push-pull; output with drive capability in both polarities. In this mode, pins can only be used as outputs. See Fig.3d.

Tables 2 and 3 show the configuration register settings for the four output configurations. The electrical characteristics of each output configuration are specified in Chapter 8. The default port configuration after reset is given in Table 2.

In case of external memory access, the appropriate options for ports P0, P2 and P3.6/P3.7 ($\overline{WR}/\overline{RD}$, only in case of external data memory access) must be set by software.

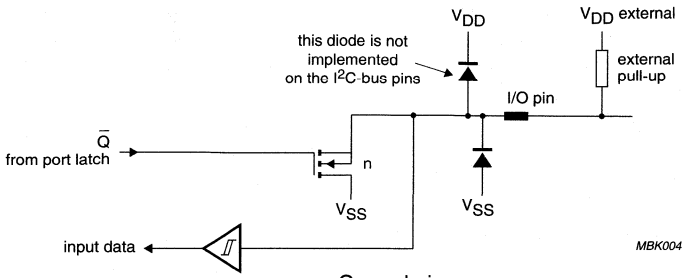
For Special Function Registers for port configurations/data please refer to Table 2, note 1.

Table 3 Port configuration register settings

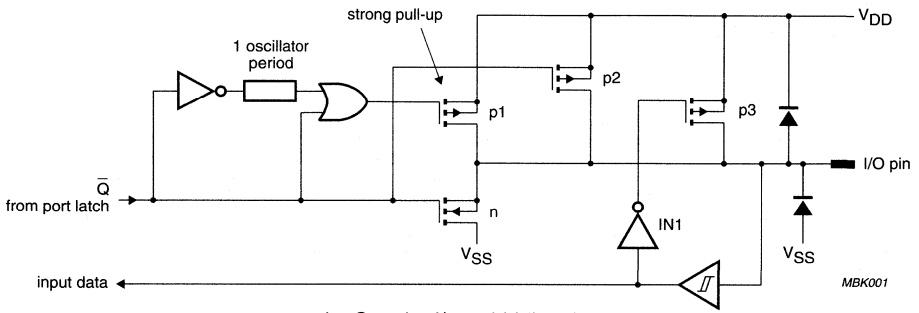
MODE(1)	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
0	0	0	open-drain	open-drain
1	1	0	quasi-bidirectional	open-drain
2	0	1	high-impedance	high-impedance
3	1	1	push-pull	open-drain

Note

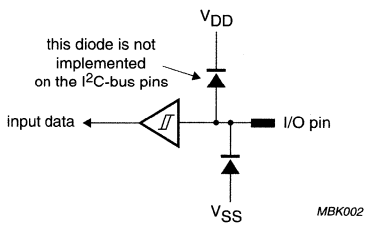
1. Mode changes may cause glitches to occur during transitions. When modifying both registers, write instructions should be carried out consecutively.



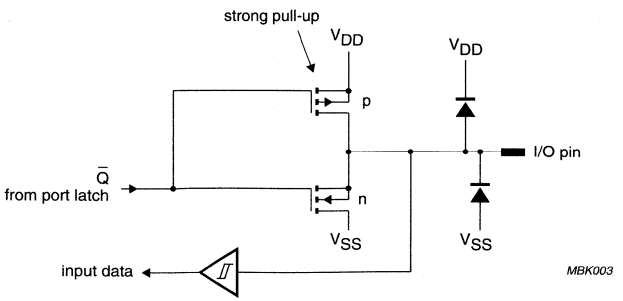
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Internal data memory

The internal data memory is divided into three physically separated parts:

256 bytes of RAM, 128 bytes of Special Function Registers and 1792 bytes of AUX-RAM. These can be addressed each in a different way (see also Table 4).

1. RAM 0 to 127 can be addressed directly and indirectly as in the 80C51; address pointers are R0 and R1 of the selected register-bank
2. RAM 128 to 255 can only be addressed indirectly; address pointers are R0 and R1 of the selected register bank
3. AUX-RAM 0 to 1791 is indirectly addressable via the AUX-RAM Page Register (XRAMP) and MOVX-Ri instructions, unless it is disabled by setting ARD = 1. AUX-RAM 0 to 1791 is also indirectly addressable as external data memory via MOVX-datapointer instruction, unless it is disable by setting ARD = 1. When executing from internal program memory, an access to AUX-RAM 0 to 1791 when ARD = 0 will not affect the ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 1791 will be performed with the MOVX @ DPTR instructions in the same way as in the 80C51 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that the external data memory cannot be accessed with R0 and R1 as address pointer if the AUX-RAM is enabled (ARD = 0, default after reset).

The Special Function Registers (SFR) can only be addressed directly in the address range from 128 to 255.

Four register banks, each 8 registers wide, occupy locations 0 through 31 in the lower RAM area. Only one of these banks may be enabled at a time. The next 16 bytes, locations 32 through 47, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal 256 bytes RAM. The stack depth is only limited by the available internal RAM space of 256 bytes (see Fig.4).

Table 4 Internal data memory map

LOCATION	ADDRESS	ADDRESSING
RAM	0 to 127	direct and indirect
AUX-RAM	0 to 1791	indirect only with MOVX
RAM	128 to 255	indirect only
SFR	128 to 255	direct only

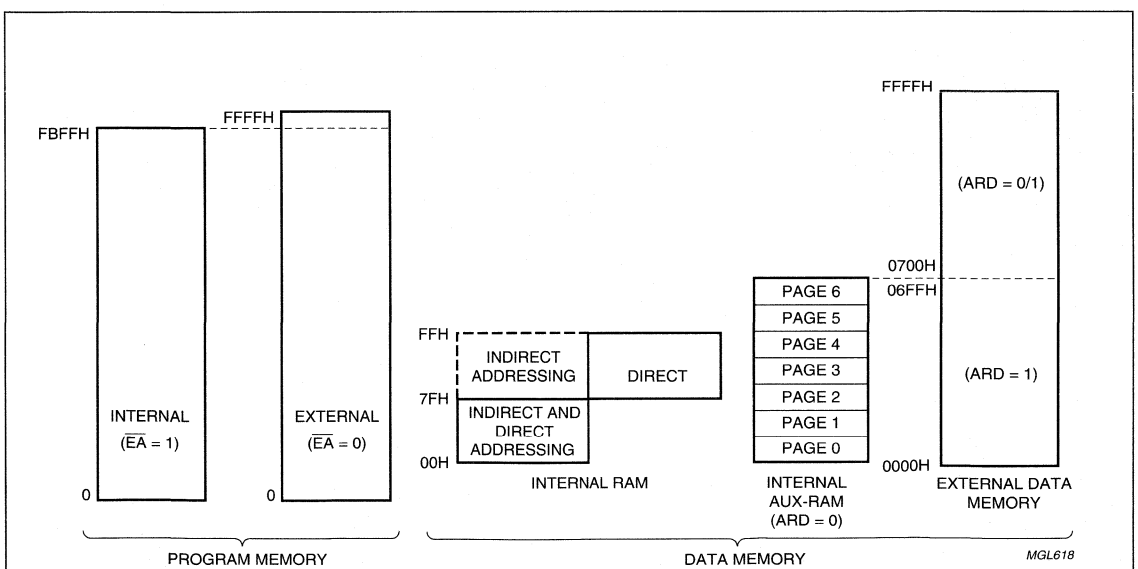


Fig.4 Memory map.

6.3.1 AUX-RAM PAGE REGISTER (XRAMP)

The AUX-RAM Page Register is used to select one of the seven 256 bytes pages of the internal 1792-byte AUX-RAM for MOVX-accesses via R0 or R1. Its reset value is 'XXXX X000' (AUX-RAM page 0).

Table 5 AUX-RAM Page Register (SFR address FAH)

7	6	5	4	3	2	1	0
–	–	–	–	–	XRAMP2	XRAMP1	XRAMP0

Table 6 Description of XRAMP bits

BIT	SYMBOL	FUNCTION
7 to 3	–	reserved, undefined during read, a write operation must write logic 0 to these locations
2	XRAMP2	AUX-RAM page select bit 2
1	XRAMP1	AUX-RAM page select bit 1
0	XRAMP0	AUX-RAM page select bit 0

Table 7 Memory locations for all possible MOVX accesses

ARD[1]	XRAMP2	XRAMP1	XRAMP0	ACCESS	INSTRUCTION TYPE
0	0	0	0	AUX-RAM page 0 (address 0 to 255)	MOVX @ Ri, A and MOVX @ A, Ri
0	0	0	1	AUX-RAM page 1 (address 256 to 511)	
0	0	1	0	AUX-RAM page 2 (address 512 to 767)	
0	0	1	1	AUX-RAM page 3 (address 768 to 1023)	
0	1	0	0	AUX-RAM page 4 (address 1024 to 1279)	
0	1	0	1	AUX-RAM page 5 (address 1280 to 1535)	
0	1	1	0	AUX-RAM page 6 (address 1536 to 1791)	
0	1	1	1	no valid memory access	
1	X	X	X	external RAM locations 0 to 255	
0	X	X	X	AUX-RAM locations 0 to 1791 external RAM locations 1792 to 65535	MOVX @ DPTR, A and MOVX A, DPTR
1	X	X	X	external RAM locations 0 to 65535	

Note

1. ARD (AUX-RAM Disable) corresponds to bit 6 in the Special Function Register PCON (address 87H).

6.4 OTP programming

6.4.1 OTP PROGRAMMING

The 63-kbyte One-Time Programmable (OTP) memory can be programmed by using an OM4260 programmer together with a programmer adapter OM5510. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.4.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space. The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = D6H, indicates P87CL881H

(060H) = 00H, currently not used.

6.4.2 IN-SYSTEM PROGRAMMING MODE

In the In-System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In-System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In-System Programming four SFRs are used to control the OTP.

Table 8 SFRs for In-System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In-System Register

6.4.2.1 OTP In-System Programming Register (OISYS)

The OISYS SFR controls the In-System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 9 OTP In-System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	0	SIG	WE	InSysMode

Table 10 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	These bits are reserved.
4	VPon	V_{PP} status (read only).
3	0	This bit is reserved and must be kept to logic 0.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In-System Programming status bit.

6.4.2.2 *Mode entry*

The In-System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In-System program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

The program voltage has to be available and stable for at least 10 µs before the mode is entered and has to be stable until the circuit has left the In-System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.4.2.3 *Program cycle*

The data and address must be supplied to the microcontroller and the control program has to write the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 µs cycle and the WE bit of the OISYS SFR must be set. Now the core has to be set into Idle mode. As long as the circuit is in Idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 63 kbytes address space.

6.4.2.4 *Verify for In-System Programming*

Verify is done in similar way as programming. The circuit is put into Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 µs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way. To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.4.2.5 *Signature bytes*

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed.

The signature bytes (and other test addresses) are always readable independent of the security.

6.4.2.6 *How to connect the PORENABLE/V_{PP} pin in the In-System Programming mode*

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE must be able to withstand up to 13 V, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.5.

In the example (see Fig.5) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee a minimum 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

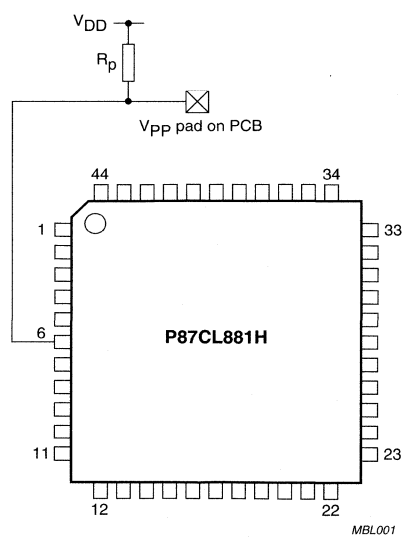


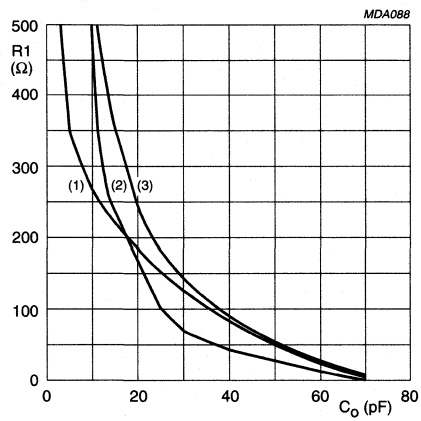
Fig.5 Example of PORENABLE/V_{PP} connection on a PCB.

6.5 Oscillator circuitry

General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.5.1 RESONATOR REQUIREMENTS

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.6a. The value of the parallel resistor R_0 must be less than 47 kΩ. The wiring between chip and resonator should be kept as short as possible.



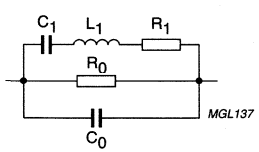
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves for 3.58 MHz.



b. Resonator equivalent circuit.

Fig.6 Resonator requirements for the ACO.

6.6 Non-conformance

6.6.1 PROGRAMMING INTERFACE/TRANSPARENT MODE

The transparent mode is a special operating mode of the microcontroller used for parallel and In-System OTP programming.

For certain combinations of data written to Port 2 (used for control signal during parallel programming mode) the Transparent mode may be incorrectly active during normal operation of the microcontroller. In this case, a transition on any of the Port 0 pins can influence the read out of the on-chip program memory resulting in incorrect code execution.

To avoid this problem, the InSysMode bit in the OTP In-System Programming Register (SFR address DCH) **must** be set in the start-up sequence of the program code.

Apart from preventing incorrect operation as described above, the setting of this bit does not affect the normal operation.

6.6.2 MOVC INSTRUCTION LIMITATION

The 'MOVC' access to a data or program byte stored in internal ROM/OTP-memory is inhibited while fetching code from external program memory in roll-over mode.

Roll-over mode means that the CPU executes code out of the external program memory because the program counter exceeds the highest address for internal program memory. The affected address range is FC00H to FFFFH.

6.6.3 LOW VOLTAGE DETECTION

The LVDI bit (LVDCON.6) may be incorrectly set due to a glitch on the LVD output when the LVD is enabled by changing the bits LVDCON<3:0> from '0000' to any value within the range '0001' to '0101'. If bit EA in register IEN0 is enabled, an unwanted interrupt may occur.

A software workaround for this problem exist. During the initialisation sequence:

- Enable LVD by writing to register LVDCON
- Enable LVD interrupt by writing to register IEN2
- Clear the LVDI bit by writing to LVDCON a second time
- Set bit EA in register IEN0 (ensures LVDI to be cleared after initialisation).

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 DC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 1 to 10 MHz; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	supply current operating	V_{DD} = 3 V; f_{xtal} = 7 MHz; note 1	–	–	4.8	mA
		T_{amb} = 25 °C	–	3.7	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; f_{xtal} = 7 MHz; note 2	–	–	0.7	mA
		T_{amb} = 25 °C	–	0.58	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3				
		POR and LVD enabled	–	2	5	µA
		POR and LVD disabled	–	50	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; f_{xtal} = 7 MHz; T_{amb} = 25 °C; notes 4 and 5				
	Watchdog		–	220	–	µA
	I^2C-bus		–	180	–	µA
	UART		–	180	–	µA
	Timer T2		–	180	–	µA
	Timer T0 or T1		–	10	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (ports, $\overline{RST}$ and PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8 and Fig.8	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.2V_{DD}$; note 8 and Fig.8	–	200	1000	µA
$\lvert I_{ILEAK} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Outputs (ports and $\overline{RST}$)						
I_{OL}	LOW-level output current; except SDA and SCL	V_{OL} = 0.4 V	2	–	–	mA
I_{OL2}	LOW-level output current; SDA and SCL	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except (push-pull options only)	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up current source	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	0.05	0.2	–	µA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	0.6	2.5	µA
POR (Power-on reset) for the LVD (Low Voltage Detection), see note 10						
V_{PORH}	trip level HIGH	(option 5 in *"TELX family specification"*)	2.13	2.37	2.61	V
V_{PORL}	trip level LOW	(option B in *"TELX family specification"*)	–	1.30	–	V
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 11	–	10	–	pF
In-System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
$t_{prog(security)}$	program cycle time security	note 12	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{VPP(setup)}$	program voltage setup time		10	–	–	µs
$t_{VPP(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{VPP}	program voltage current	In-System Programming	–	–	40	mA

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (3.7 + 0.220 + 0.18) mA = 4.1 mA at V_{DD} = 3 V and f_{XTAL} = 7 MHz.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For pin PORENABLE the V_{IL} max is $0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$ and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the *"TELX family specification, Chapter - Low voltage detection"*.
11. C_{1i}/C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).
12. Can also be done by two 100 µs pulses.

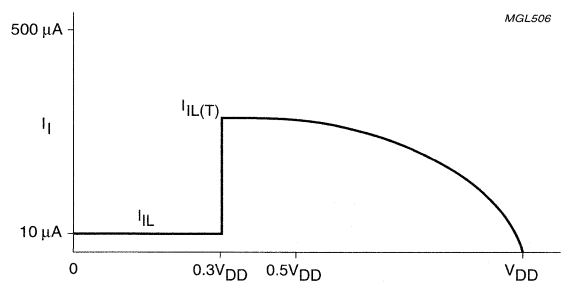


Fig.7 Input current.

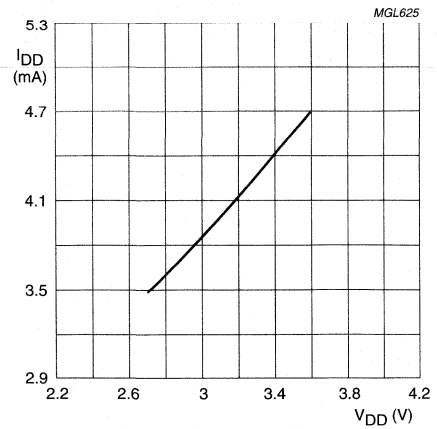


Fig.8 Typical operating current as a function of V_{DD}; T_{amb} = 25 °C; f_{xtal} = 7 MHz.

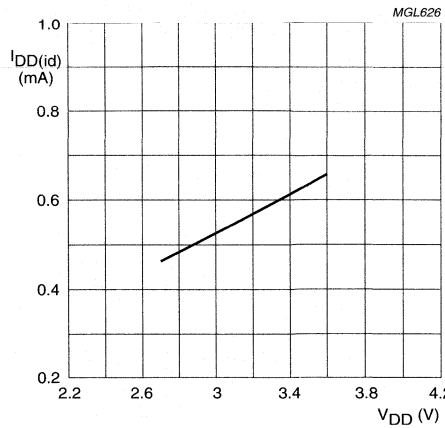
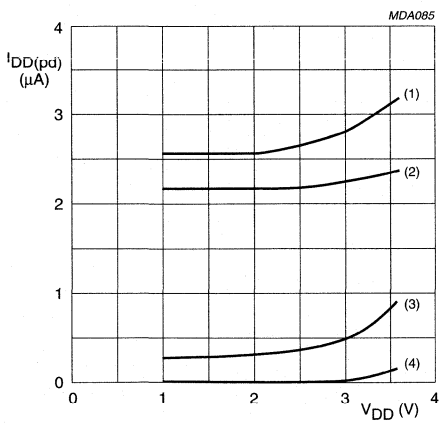


Fig.9 Typical Idle current as a function of V_{DD}; T_{amb} = 25 °C; f_{xtal} = 7 MHz.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.10 Typical power-down current as a function of V_{DD}.

9 AC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified. All values verified on sampling basis.

SYMBOL	PARAMETER	VARIABLE CLOCK		UNIT
		MIN.	MAX.	
External program memory				
t_{LHLL}	ALE pulse width	t_{CLK}	–	ns
t_{AVLL}	address valid to ALE LOW	$0.5t_{CLK} - 10$	–	ns
t_{LLAX}	address hold after ALE LOW	$0.5t_{CLK}$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	$2t_{CLK} - 25$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	$0.5t_{CLK}$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	$1.5t_{CLK}$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	$1.5t_{CLK} - 35$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	$0.5t_{CLK}$	ns
t_{AVIV}	address to valid instruction in	–	$2.5t_{CLK} - 35$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	–	5	ns
External data memory				
t_{RLRH}	$\overline{RD}$ pulse width	$3t_{CLK}$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	$3t_{CLK}$	–	ns
t_{AVLL}	address valid to ALE LOW	$0.5t_{CLK}$	–	ns
t_{LLAX}	address hold after ALE LOW	$0.5t_{CLK}$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	$2.5t_{CLK}$	ns
t_{RHDX}	data hold after $\overline{RD}$	0	–	ns
t_{RHDZ}	data float after $\overline{RD}$	–	t_{CLK}	ns
t_{LLDV}	ALE LOW to valid data in	–	$4t_{CLK}$	ns
t_{AVDV}	address to valid data in	–	$4.5t_{CLK} - 30$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	$1.5t_{CLK} - 15$	$1.5t_{CLK} + 15$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	$2t_{CLK}$	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	$0.5t_{CLK}$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	$3.5t_{CLK}$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	$0.5t_{CLK}$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	0	ns

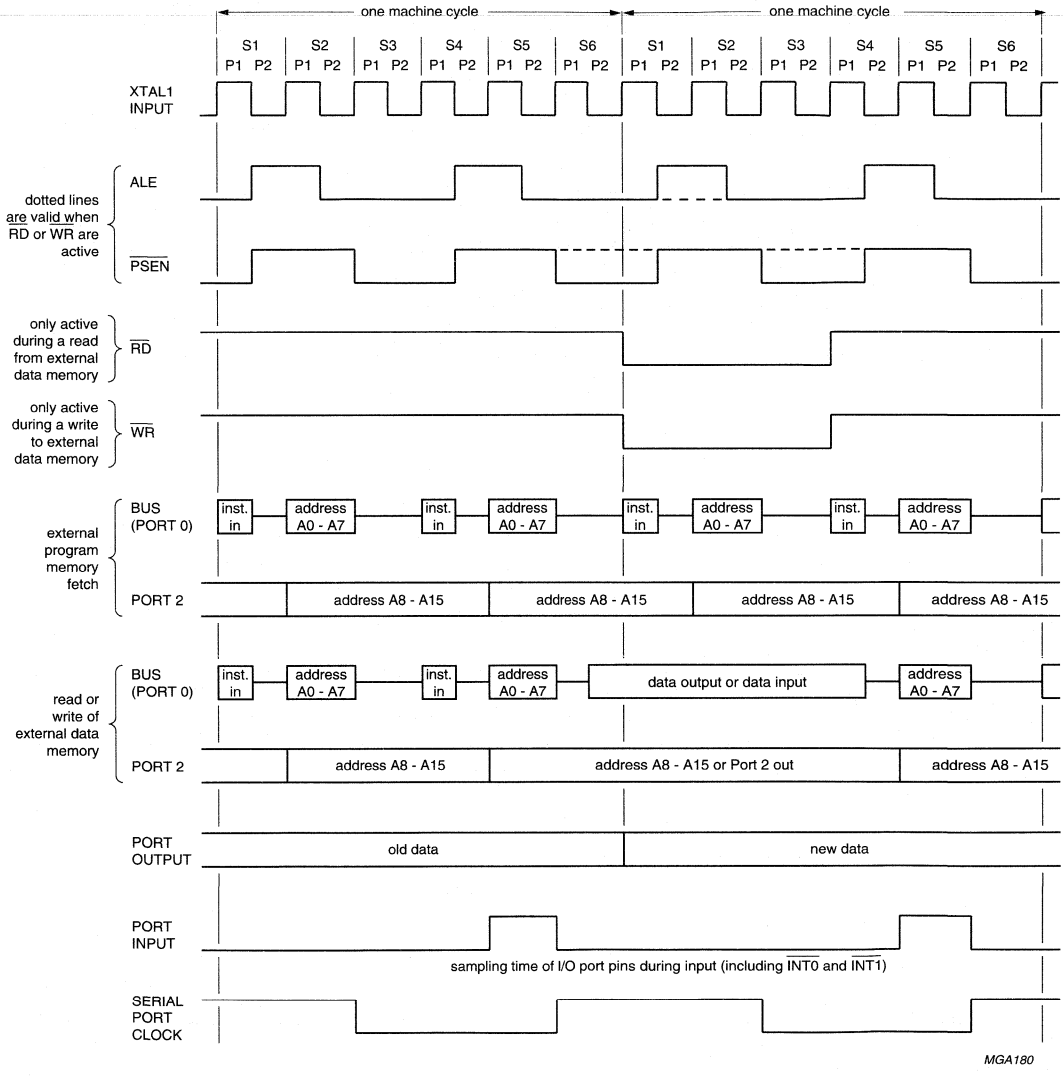


Fig.11 Instruction cycle timing.

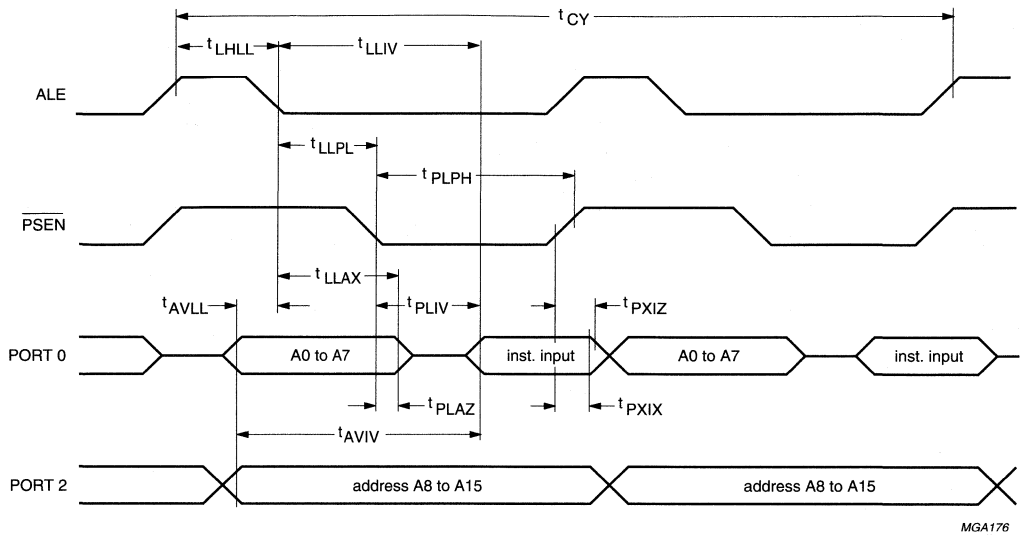


Fig.12 Read from external program memory.

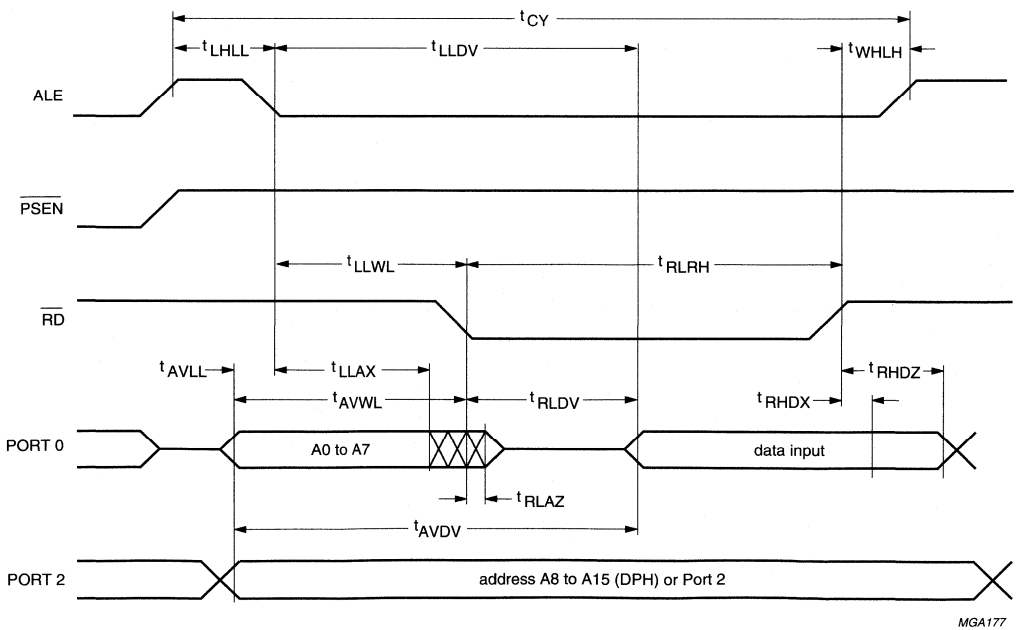


Fig.13 Read from external data memory.

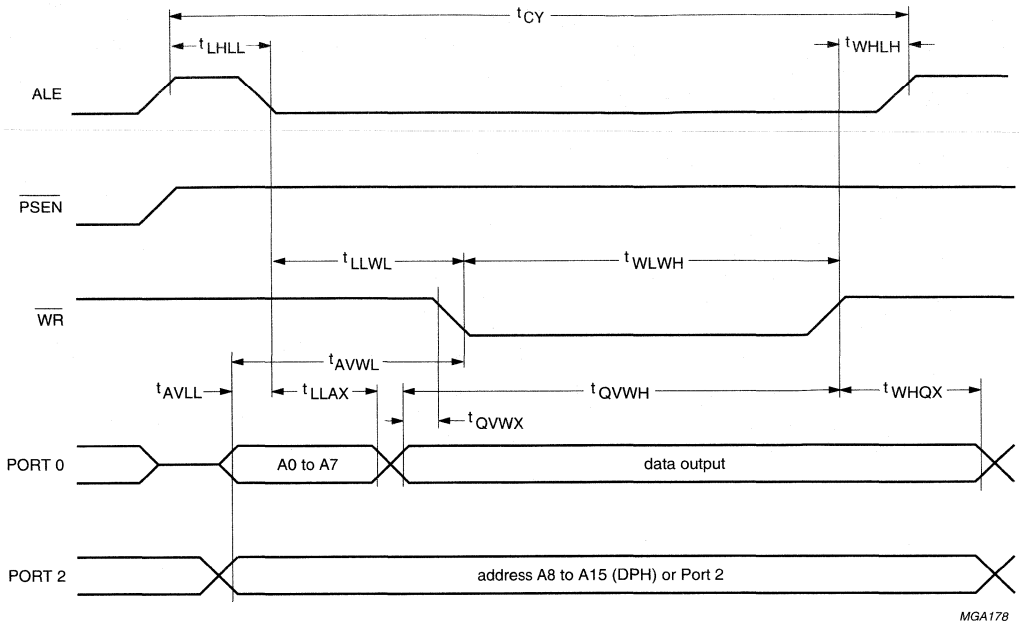
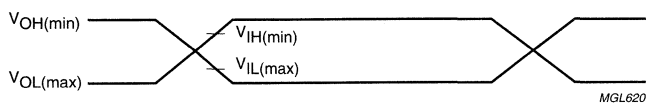


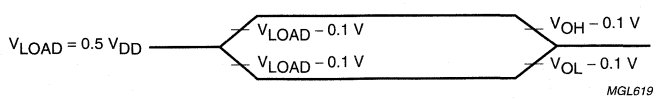
Fig.14 Write to external data memory.

9.1 AC testing

AC testing inputs are driven at 2.4 V for a HIGH level and 0.45 V for a LOW level. Timing measurements are taken at 2.0 V for a HIGH level and 0.8 V for a LOW level, see Fig.15a. The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels, see Fig.15b.



a. AC inputs during testing are driven at $V_{OH(min)}$ for a logic 1 and $V_{OL(max)}$ for a logic 0. Timing measurements are made at $V_{IH(min)}$ for a logic 1 and $V_{IL(max)}$ for a logic 0.



b. For timing purposes, a port is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} > 1.6$ mA.

Fig.15 AC testing input, output waveform (a) and float waveform (b).

CONTENTS

TELX microcontrollers for CT0 handset/basestation applications

P8xCL883; P8xCL884

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions.
- 8-bit ports:
  - P8xCL883: 3 (19 I/O lines)
  - P8xCL884: 3 (18 I/O lines).
- Program Memory:
  - P8xCL883/P8xCL884: 8-kbyte One Time Programmable (OTP).
- 256-byte RAM
- 128-byte EEPROM Data Memory, accessed internally via I²C-bus interface (P8xCL884 only)
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control.
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator (P8xCL884 only)
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: −25 to +70°C
- 28 pin SO package.

2 GENERAL DESCRIPTION

The P8xCL883/P8xCL884 are manufactured in an advanced CMOS technology. The P8xCL883 is based on single-chip technology and the P8xCL884 is based on MCM (Multi-Chip-Module) technology as the EEPROM is integrated on a separate chip.

The P8xCL883/P8xCL884 are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1, CT1+ standards). For this purpose, features like DTMF, EEPROM, MSK modem and POR/LVD are integrated on-chip.

The device is optimized for low power consumption. The P8xCL883/P8xCL884 have two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL883/P8xCL884 is based on that of the 80C51. The P8xCL883/P8xCL884 also function as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. Due to the missing port P2, there is no external data or memory access and the MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL883/P8xCL884; for details of the P8xCL883/P8xCL884 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

3 ORDERING INFORMATION

TYPE NUMBER	OTP TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
P87CL883T/000	Blank OTP	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL884T/000				
P87CL883T/xxx	Factory-programmed OTP			
P87CL884T/xxx				
P83CL883T/xxx	Pre-programmed OTP			
P83CL884T/xxx				

4 BLOCK DIAGRAM

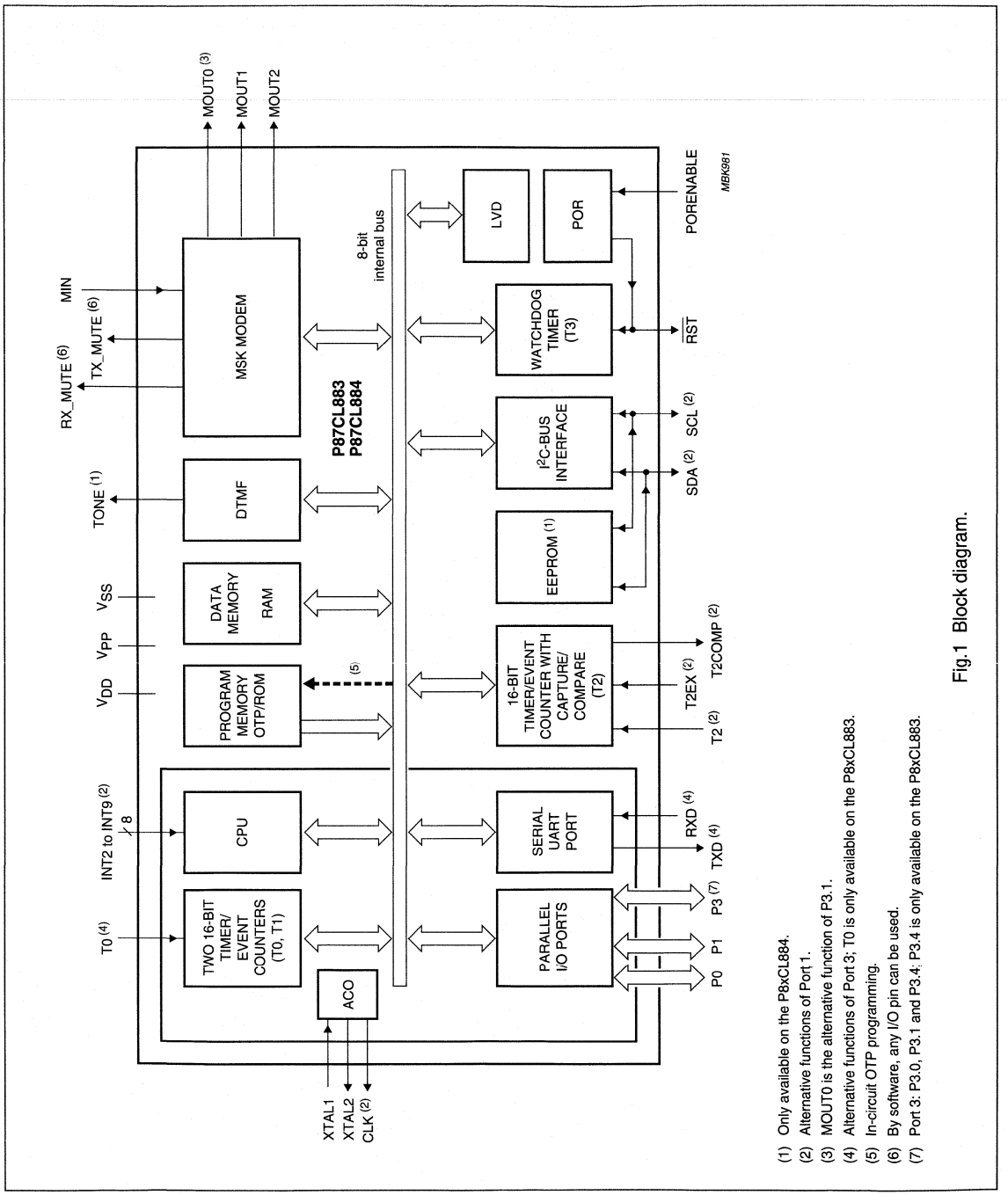
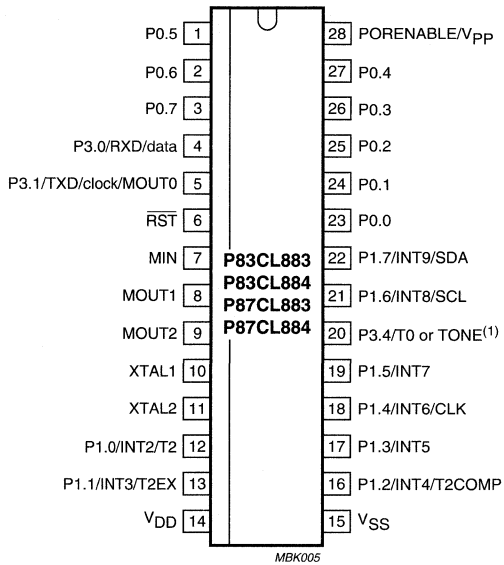


Fig.1 Block diagram.

(1) Only available on the P8xCL884.
(2) Alternative functions of Port 1.
(3) MOUT0 is the alternative function of P3.1.
(4) Alternative functions of Port 3; T0 is only available on the P8xCL883.
(5) In-circuit OTP programming.
(6) By software, any I/O pin can be used.
(7) Port 3: P3.0, P3.1 and P3.4; P3.4 is only available on the P8xCL883.

5 PINNING INFORMATION

5.1 Pinning



(1) **Pin 20**: P3.4/T0 on the P8xCL883; TONE on the P8xCL884.

Fig.2 Pin configuration.

5.2 Pin description

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active LOW reset.** A LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input.** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output.** Output of the Amplitude Controlled Oscillator. To be left unconnected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0.** 8-bit bidirectional I/O port. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1**. 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3.** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**; **T0** is an external input for Timer 0. **P3.4/T0** is only available on the P8xCL883.
P3.1/TXD/clock/ MOUT0	5	
P3.4/T0	20	
TONE	20	**DTMF** output; **TONE** is only available on the P8xCL884.
PORENABLE/V_{PP}	28	**PORENABLE**. Power-on reset circuit enable. If PORENABLE = 1, the internal Power-on reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers (SFRs)

Table 1 List of SFRs

REGISTER	ADDRESS (HEX)	RESET VALUE[1]
80C51 core		
ACC	E0	0000 0000
B	F0	0000 0000
DPL	82	0000 0000
DPH	83	0000 0000
PCH	no SFR	0000 0000
PCL	no SFR	0000 0000
PCON	87	0000 0000
PRESC	F3	0000 0000
PSW	D0	0000 0000
SP	81	0000 0111
T0/T1		
TCON	88	0000 0000
TH0	8C	0000 0000
TH1	8D	0000 0000
TL0	8A	0000 0000
TL1	8B	0000 0000
TMOD	89	0000 0000
Port		
ALTP	A3	0000 0000
P0	80	1111 1111
P0CFGA	8E	1111 1111
P0CFGB	8F	0000 0000
P1	90	1111 1111
P1CFGA	9E	0011 1111
P1CFGB	9F	0000 0000
P3	B0	XXX1 XX11
P3CFGA	BE	XXX1 XX11
P3CFGB	BF	XXX0 XX00
P4	C1	XXXX XXX0
TIMER2		
COMP2H	AB	0000 0000
COMP2L	AA	0000 0000
RCAP2H	CB	0000 0000
RCAP2L	CA	0000 0000

REGISTER	ADDRESS (HEX)	RESET VALUE[1]
T2CON	C8	0000 0000
TH2	CD	0000 0000
TL2	CC	0000 0000
EEPROM interface		
EECON	FB	0000 0000
DTMF		
HGF	A2	0000 0000
LGF	A1	0000 0000
Interrupt logic		
IEN0	A8	0000 0000
IEN1	E8	0000 0000
IEN2	F1	0000 0000
IP0	B8	0000 0000
IP1	F8	0000 0000
IP2	F9	0000 0000
ISE1	E1	0000 0000
IX1	E9	0000 0000
IRQ1	C0	0000 0000
LVD		
LVDCON	F2	0000 0000
POR/ACO		
RSTAT	E6	XXX0 1000
MSK		
MCON	D3	0000 0000
MBUF	D1	XXXX XXXX
MSTAT	D2	XX00 0000
UART		
S0BUF	99	0000 0000
S0CON	98	0000 0000
I²C-bus interface		
S1ADR	DB	0000 0000
S1CON	D8	0000 0000
S1DAT	DA	0000 0000
S1STA	D9	1111 1000

REGISTER	ADDRESS (HEX)	RESET VALUE[1]
WDT		
WDCON	A5	1010 0101
WDTIM	FF	0000 0000
OTP interface		
OAH	D5	X00X XXXX
OAL	D4	XXXX XXXX
ODATA	D6	XXXX XXXX
OISYS	DC	000X 0000
OTEST	D7	0000 0000
Reserved locations; do not write		
reserved	E7, FD	–

Note

1. Where: X = undefined state or not implemented bit.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL883/P8xCL884 have 19 and 18 I/O lines respectively, treated as 19 and 18 individually addressable bits or as three parallel 8-bit addressable ports.
The alternative functions are detailed below:

Port 0 Offers no alternative functions.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 which are serial port receiver input and transmitter output (UART)
- P3.4/T0 as counter input; available only in P8xCL883.

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor 'p1' is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter IN1. This inverter and transistor 'p3' form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in port configuration SFRs. There are 2 SFRs for each port: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For example, the output type of P1.3, is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b. Except for the I^2C-bus pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up 'p1' is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through 'p2' and 'very weakly' driven through 'p3' (see Fig.3b).

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome (see Fig.3c).

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs (see Fig.3d).

Tables 2 and 3 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 3.

Table 2 Port Configuration Registers PnCFGA and PnCFGB (n = 0 to 3) settings

MODE[1]	PnCFGA	PnCFGB	PORT OUTPUT MODE	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 3 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 output data[1]	P0	80	1111 1111
Port P0 configuration A	P0CFGA	8E	1111 1111
Port P0 configuration B	P0CFGB	8F	0000 0000
Port P1 output data[1]	P1	90	1111 1111
Port P1 configuration A	P1CFGA	9E	0011 1111
Port P1 configuration B	P1CFGB	9F	0000 0000
Port P3 output data[1]	P3	B0	XXX1 XX11[2]
Port P3 configuration A	P3CFGA	BE	XXX1 XX11[2]
Port P3 configuration B	P3CFGB	BF	XXX0 XX00[2]

Notes

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).
2. Port pin P3.4 is only available on P8xCL883.

6.2.3 Alternative Port Function Register (ALTP)

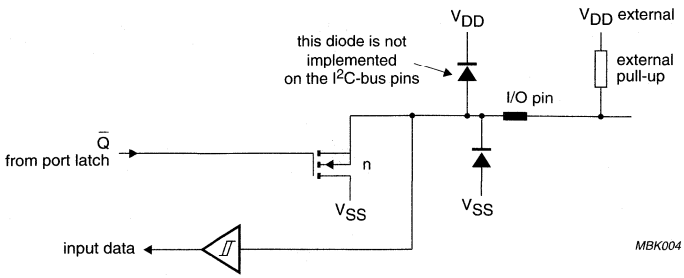
This 4-bit register selects the alternative function of certain port pins.

Table 4 Alternative Port Function Register (SFR address A3H)

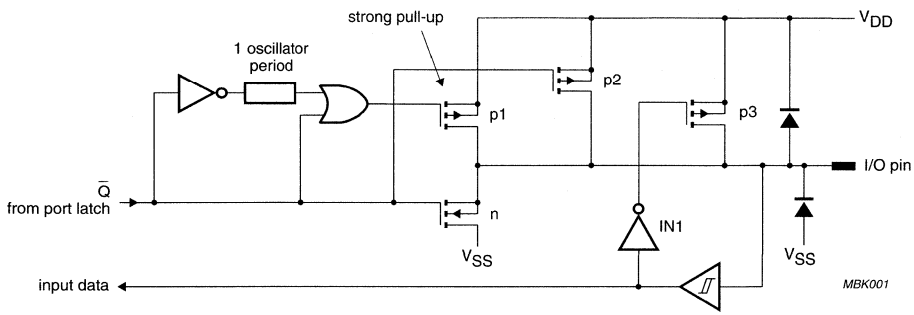
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 5 Description of ALTP bits

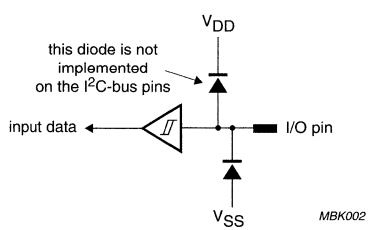
BIT	SYMBOL	DESCRIPTION
7 to 4	–	These 4 bits are reserved.
3	EMOUT0	If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	If this bit is set, the TONE output of the DTMF generator is enabled.



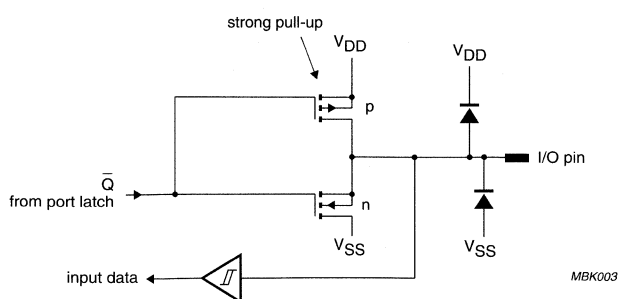
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL883/P8xCL884 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $\frac{1}{6}f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{6}f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

Note that the T0 input is only available on P8xCL883.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL883/P8xCL884 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L is compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a chip reset will set the flag COMP.
The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can also be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

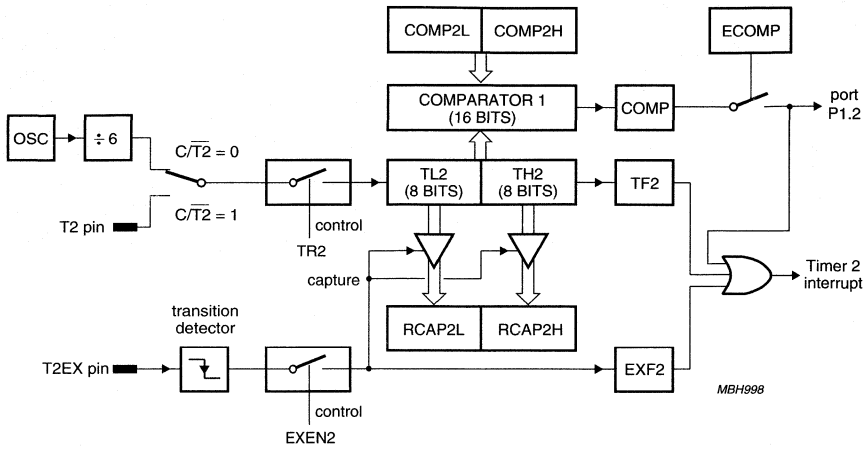


Fig.4 Timer 2 in Capture and/or Compare mode.

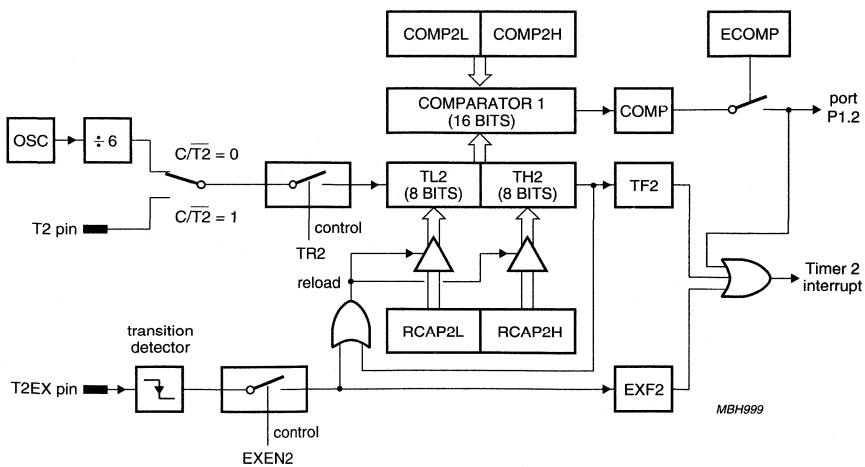


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 Timer/Counter 2 Control Register (T2CON)

Table 6 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 7 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag**. When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6}f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 8 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL883/P8xCL884, MIN is no longer the alternative function of P4.0, but MIN is a separate pin. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as an alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer

The Watchdog Timer differs from the description in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL883/P8xCL884.

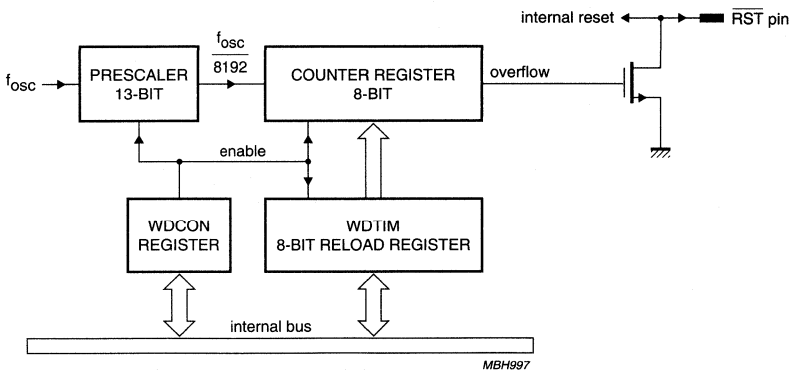


Fig.6 Functional diagram of the Watchdog Timer (T3).

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 8 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C5H, indicates P8xCL883/P8xCL884

(060H) = 00H, currently not used.

6.6.2 IN-SYSTEM PROGRAMMING MODE

In the In-System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In-System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In-System Programming four SFRs are used to control the OTP.

Table 9 SFRs for In-System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In-System Register

6.6.2.1 OTP In-System Programming Register (OISYS)

The OISYS SFR controls the In-System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data is held in the SFRs OAH and OAL.

Table 10 OTP In-System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 11 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	These bits are reserved.
4	VPon	V_{PP} status (read only).
3	–	This bit is reserved.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In-System Programming status bit.

6.6.2.2 *Mode entry*

The In-System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In-System Program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

This paragraph is valid for version 2 ('2' ending on type number). During In-System Programming the OTP memory must be in the DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In-System Programming mode is left, 00H must be written into the OTEST SRF.

The program voltage must be available and stable for at least 10 µs before the mode is entered and has to be stable until the circuit has left the In-System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.3 *Program cycle*

The data and address must be supplied to the microcontroller and the control program must write to the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 µs cycle and the WE bit of the OISYS SFR must be set. Now the core has to be set into Idle mode. As long as the circuit is in idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 8 kbytes address space.

6.6.2.4 *Verify for In-System Programming*

Verify is done in similar way as programming. The circuit is put into Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer must be initialized for a cycle of at least 1 µs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way.
To ensure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.5 *Signature bytes*

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed.

6.6.2.6 *How to connect the PORENABLE/V_{PP} pin in the In-System Programming mode*

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. One possible implementation is presented in Fig.7 where POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), the V_{PP} source must supply enough current in R_p in order to guarantee a minimum 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

6.7 Oscillator circuitry

General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.7.1 Resonator requirements

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

6.7.2 Recommended resonator types

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).

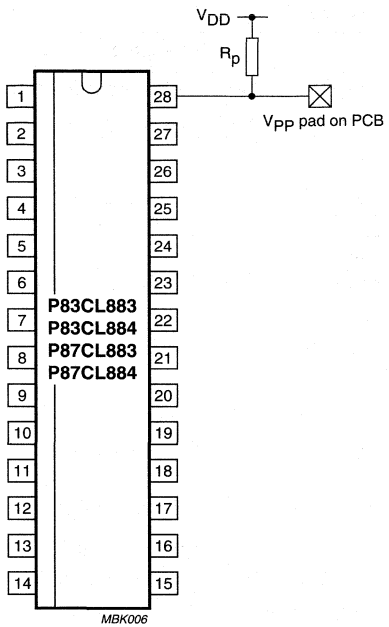
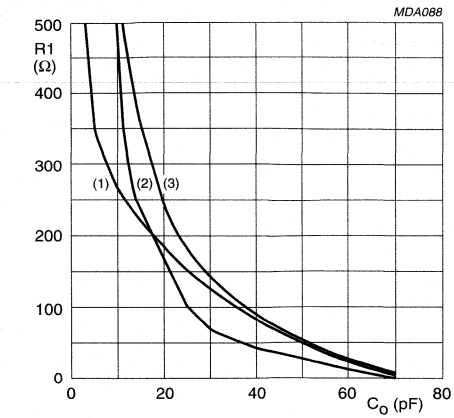


Fig.7 PORENABLE/V_{PP} connection on a PCB.



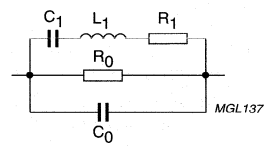
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL883/P8xCL884 uses the P87CL880 microcontroller in emulation mode. The P87CL880 is a super-set of the P8xCL883/P8xCL884, i.e. it contains all the functions of the P8xCL883/P8xCL884 plus a number of other additional functions. It should be noted that some functional differences between P87CL880 and P8xCL883/P8xCL884 exist; see Table 12.

Table 12 Differences between functions existing in P87CL880 and P8xCL883/P8xCL884

FUNCTION	P87CL880	P8XCL883/P8XCL884
Timer 2	see P87CL880 specification	see P8xCL883/P8xCL884 specification
OTP Program Memory	32 kbytes AFPROM	8 kbytes EPROM or pre-programmed ROM
RAM	512 bytes	256 bytes
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL883/P8xCL884 specification
In-System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL883/P8xCL884 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Package	QFP64	SO28

6.9 Non-conformance

6.9.1 Programming interface/Transparent mode

The Transparent mode is a special operating mode of the microcontroller used for parallel and In-System OTP programming.

For certain combinations of data written to Port 1 (used for control signal during parallel programming mode) the Transparent mode may be incorrectly active during normal operation of the microcontroller. In this case, a transition on any of Port 0 pins can influence the read out of the on-chip program memory, resulting in incorrect code execution.

To avoid this problem, the InSysMode bit in the OTP In-System Programming Register (SFR address DCH) **must** be set in the start-up sequence of the program code.

Apart from preventing incorrect operation as described above, the setting of this bit does not affect the normal operation.

6.9.2 Low Voltage Detection

The LVDI bit (LVDCON.6) may incorrectly be set due to a glitch on the LVD output, when the LVD is enabled, by changing the bits LVDCON(3:0) from '0000' to any value within the range '0001' to '0101'. If bit EA in register IEN0 is enabled, an unwanted interrupt may occur.

A software workaround for this problem exists. During the initialisation sequence:

- Enable LVD by writing to register LVDCON
- Enable LVD interrupt by writing to register IEN2
- Clear the LVDI bit by writing to LVDCON a second time
- Set bit EA in register IEN0 (ensures LVDI to be cleared after initialisation).

6.9.3 Edge detection on UART

In receive mode 1, 2 and 3 it is possible that an internal setup/hold condition of a flip-flop is violated. This results in a not detected start bit (start condition) during receive mode. The probability of occurrence (verified on sampling basis) is below 3%.

There is no workaround for this problem other than to use the UART only in Mode 0 for reception.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	−65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = −25 to +70 °C;
T_{amb} (during In-System Programming) = +20 to +40 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In-System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	–	3.0	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1; see Fig.10	–	1.8	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	–	–	0.55	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 2; see Fig.11	–	0.38	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3; see Fig.12				
		POR and LVD enabled	–	2	5	µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; T_{amb} = 25 °C; notes 4 and 5				
	EEPROM erase/write		–	460	–	µA
	DTMF	no load on TONE output	–	240	–	µA
	MSK modem		–	140	–	µA
	Watchdog		–	110	–	µA
	I^2C-bus		–	90	–	µA
	UART		–	90	–	µA
	Timer T2		–	90	–	µA
	Timer T0 or T1		–	5	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (Ports, MIN, $\overline{RST}$, MOUT0 to MOUT2, PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.9	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.9	–	200	1000	µA
$\lvert I_{LI} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Port outputs (Ports, $\overline{RST}$, MOUT0 to MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	–	–	mA
I_{OL1}	LOW-level output current; P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	0.05	0.2	–	µA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	0.6	2.5	µA
Power-on reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.13)						
$V_{HG(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} = 3 V; T_{amb} = 25 °C; notes 5 and 12	–	25	–	dB
EEPROM (notes 5 and 13)						
$t_{E/W}$	erase/write time		8	10	12	ms
$N_{E/W}$	erase/write cycles		10^5	–	–	
t_{DR}	data retention time	T_{amb} = +70 °C	10	–	–	years

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
In-System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In-System Programming	–	–	40	mA
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 15	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected;.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (1.8 + 0.11 + 0.09) mA = 2.0 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For pin PORENABLE the $V_{IL(max)} = 0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the specification in the data sheet *"TELX family; Chapter: Low Voltage Detection"*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. After final testing the value of each EEPROM bit is typically logic 1.
14. Can also be done by two 100 µs pulses.
15. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance, leadframe capacitance).

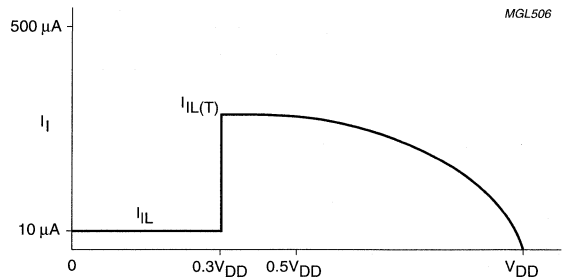


Fig.9 Input current.

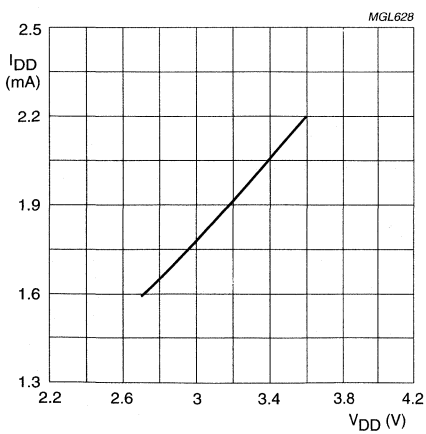


Fig.10 Typical operating current as a function of V_{DD}, T_{amb} = 25 °C.

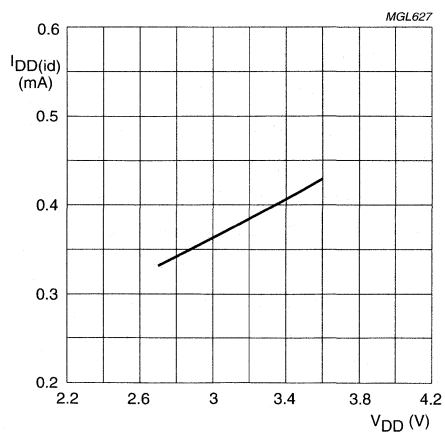
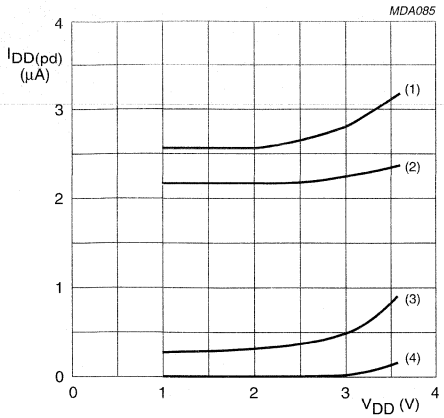
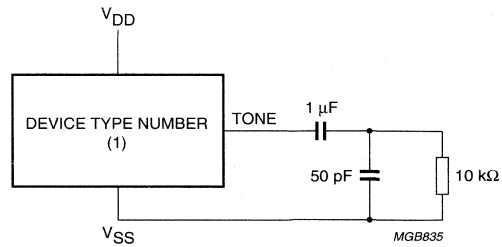


Fig.11 Typical Idle current as a function of V_{DD}, T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.12 Typical Power-down current as a function of V_{DD}.



(1) P8xCL883/P8xCL884.

Fig.13 TONE output test circuit.

16-bit microcontroller P90CE201

FEATURES

- CMOS technology
- Full 68000 software compatibility
- 32-bit internal structure
- 16-bit internal data transfer
- 8-bit access to external ROM/RAM
- External addressing range 16 Mbytes for ROM and 16 Mbytes for RAM
- Unused address pins can be used as quasi-bidirectional ports
- On-chip address decoder for ROM/RAM
- 8 edge triggered programmable interrupts that can also be used as quasi-bidirectional ports
- Reset control
- Built-in clock generator
- 2 fully independent fast I^2C-bus serial interfaces
- UART serial interface (4 modes)
- 3 fully independent 16-bit timers
- Watchdog timer
- 8-bit quasi-bidirectional port, 4-bits with high drive capability
- EMC optimized layout and pinning
- 64-pin QFP package.

GENERAL DESCRIPTION

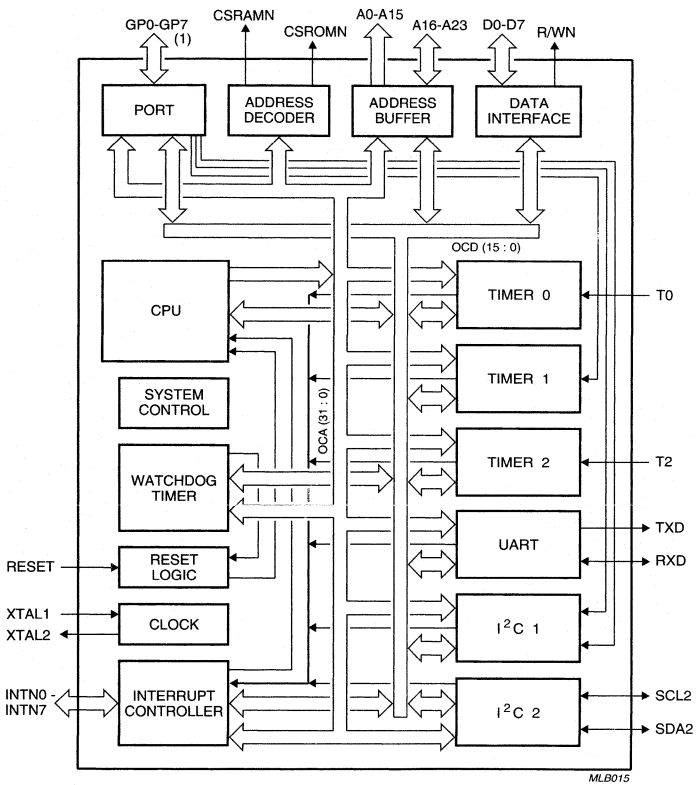
The P90CE201 is a member of the P9XCXXX family of highly integrated 16-bit microcontrollers for use in a wide variety of applications. It is fully software compatible with the 68070/68000. The complete set of system functions available on the chip results in reduced system cost. Additionally, its modular design concept permits future extension to the family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				CLOCK FREQUENCY (MHz)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE		
P90CE201AEB	64	QFP	plastic	SOT319[1]	24.0	–25 to 85

Note

1. SOT319-2; 1996 November 28.



1. The General Port lines GP5, GP6 and GP7 have alternate functions for Timer 1, SCL1 and SDA1 respectively; see Table 1.

Fig.1 Block diagram.

PINNING INFORMATION

Pinning

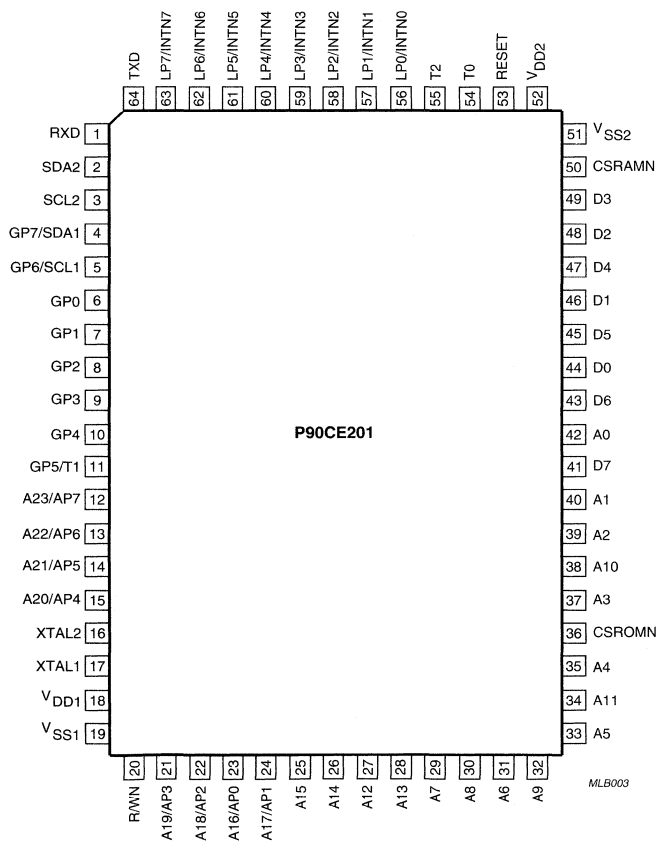


Fig.2 Pin configuration for QFP64.

Pin description

Table 1 QFP64 package.

MNEMONIC	TYPE	PIN NO.	FUNCTION
RXD	I/O	1	**Receive Data.** RXD is the data input for the UART interface.
SDA2	I/O	2	**Serial Data 2** (open drain). SDA2 is the data signal for the second I^2C-bus serial interface.
SCL2	I/O	3	**Serial Clock 2** (open drain). SCL2 is the clock signal for the second I^2C-bus serial interface.
GP7/SDA1 GP6/SCL1 GP0 GP1 GP2 GP3 GP4 GP5/T1	I/O	4 5 6 7 8 9 10 11	**General Purpose Port** (active HIGH, 3-state). The alternative functions are as follows. SCL1 is the clock signal for the first I^2C-bus serial interface. SDA1 is the data signal for the first I^2C-bus serial interface. T1 is the input pin for Timer 1.
A23/AP7 to A16/AP0	I/O	12 to 15, 21, 22, 24, 23	**Address Bus.** Upper 8-bits of the address bus (A23 to A16). The unused address bits can be selected as a quasi-bidirectional port (AP).
A15 to A0	O	25, 26, 28, 27, 34, 38, 32, 30, 29, 31, 33, 35, 37, 39, 40, 42	**Address Bus.** Lower 16-bits of the address bus.
XTAL2	O	16	**Oscillator output.** Not connected if an external clock generator is used.
XTAL1	I	17	**Oscillator input.** XTAL1 can also be used as an external clock input if an external clock generator is used.
V_{DD1}	–	18	**Supply voltage.** For internal logic, address bus, data bus, RWN, CSRAMN, CSROMN, XTAL1 and XTAL2.
V_{SS1}	–	19	**Ground.** For internal logic, address bus, data bus, RWN, CSRAMN, CSROMN, XTAL1 and XTAL2.
R/WN	O	20	**Read** (active HIGH)/**Write** (active LOW). This controls the direction of data flow.
CSROMN	O	36	**Chip Select ROM** (active LOW). This signal selects external ROM.
D0 to D7	O	44, 46, 48, 49, 47, 45, 43, 41	**Data Bus.** 8-bit data bus.
CSRAMN	O	50	**Chip Select RAM** (active LOW). This signal enables external RAM.
V_{SS2}	–	51	**Ground.** For all other periphery pins (quiet port).
V_{DD2}	–	52	**Supply voltage.** For all other periphery pins (quiet port).
RESET	I	53	**Reset** (active HIGH). Input pin for an external reset.
T0	I	54	**Timer 0.** Input pin for cycle and event counting using Timer 0.
T2	I	55	**Timer 2.** Input pin for cycle and event counting using Timer 2.

MNEMONIC	TYPE	PIN NO.	FUNCTION
LP0/INTN0 LP1/INTN1 LP2/INTN2 LP3/INTN3 LP4/INTN4 LP5/INTN5 LP6/INTN6 LP7/INTN7	I/O	56 57 58 59 60 61 62 63	**Latched Interrupt inputs** (active LOW). A LOW level of ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable. Unused interrupt inputs can be used as a quasi-bidirectional port (LP).
TXD	O	64	**Transmit Data.** TXD is the data output for the UART serial interface.

Low voltage 16-bit microcontroller P90CL301BFH (C100)

FEATURES

- Fully 68000 software compatible
- Static design with 32-bit internal structure
- Power saving modes: Power-down, Standby and Idle mode
- External clock input: 27 MHz at 2.7 V
- Single supply voltage of 2.7 to 3.6 V; down to 1.8 V for RAM retention
- 68000 compatible bus interface
- Intel 8051 compatible bus interface
- 16 Mbytes program/data address range
- 8 programmable chip-selects
- Dynamic bus sizing, 16 or 8-bit memory bus port size
- 56 powerful instruction types:
  - 5 basic data types, and
  - 14 addressing modes
- 7 programmable interrupt inputs:
  - a Non-Maskable Interrupt input (NMIN)
  - 14 auto-vectored interrupts and 7 interrupt priority levels
- 24 port pins (multiplexed with other functions)
- 2 UART serial interfaces; an independent baud rate generator with two programmable outputs (UART0 and UART1)
- UART queue with maximum 256 bytes
- I²C-bus serial interface 100 kbaud
- 2 timer arrays including:
  - two 16-bit reference counters and 8-bit programmable prescalers
  - six 16-bit match/capture registers with equality comparators
- Watchdog Timer with 21-bit resolution
- Two 8-bit Pulse Width Modulation (PWM) outputs with 8-bit prescaler
- Four 8-bit Analog-to-Digital Converter (ADC) inputs with Power-down mode
- 512 bytes RAM on-chip
- On-Circuit Emulation (ONCE) mode and internal Test-ROM (256 bytes) for on-board testing
- 80-pin LQFP package
- Temperature range –40 to +85 °C
- 0.5 micron CMOS low voltage technology.

DESCRIPTION

The P90CL301BFH is a highly integrated low-voltage 16/32-bit microcontroller especially suitable for digital mobile systems such as GSM, DCS1900, IS54/95 and other applications requiring low voltage, low power consumption and high computing power. It is fully software compatible with the 68000.

The P90CL301BFH optimizes system cost by providing both standard as well as advanced peripheral functions on-chip. The P90CL301BFH has a full static design and special Idle, Standby and Power-down modes which allow further reduction of the total system power consumption. An 80-pin LQFP package dramatically reduces system size requirements.

Compatibility between P90CL301AFH and P90CL301BFH

For functional compatibility between P90CL301AFH (SAC1 process) and P90CL301BFH (C100 process), the following points should be considered when using the P90CL301BFH:

- **Wake-up**; to wake-up the processor from Power-down mode via the activation of an external SPn pin, it is necessary to enable the interrupt mode first by setting the corresponding bit in the SPCON register.
- **SYSCON register**; for the P90CL301AFH bits 11 to 15 in the SYSCON register should not be set in order to keep additional functionality in the P90CL301BFH inactive.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
P90CL301BFH	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1	–40 to +85

BLOCK DIAGRAM

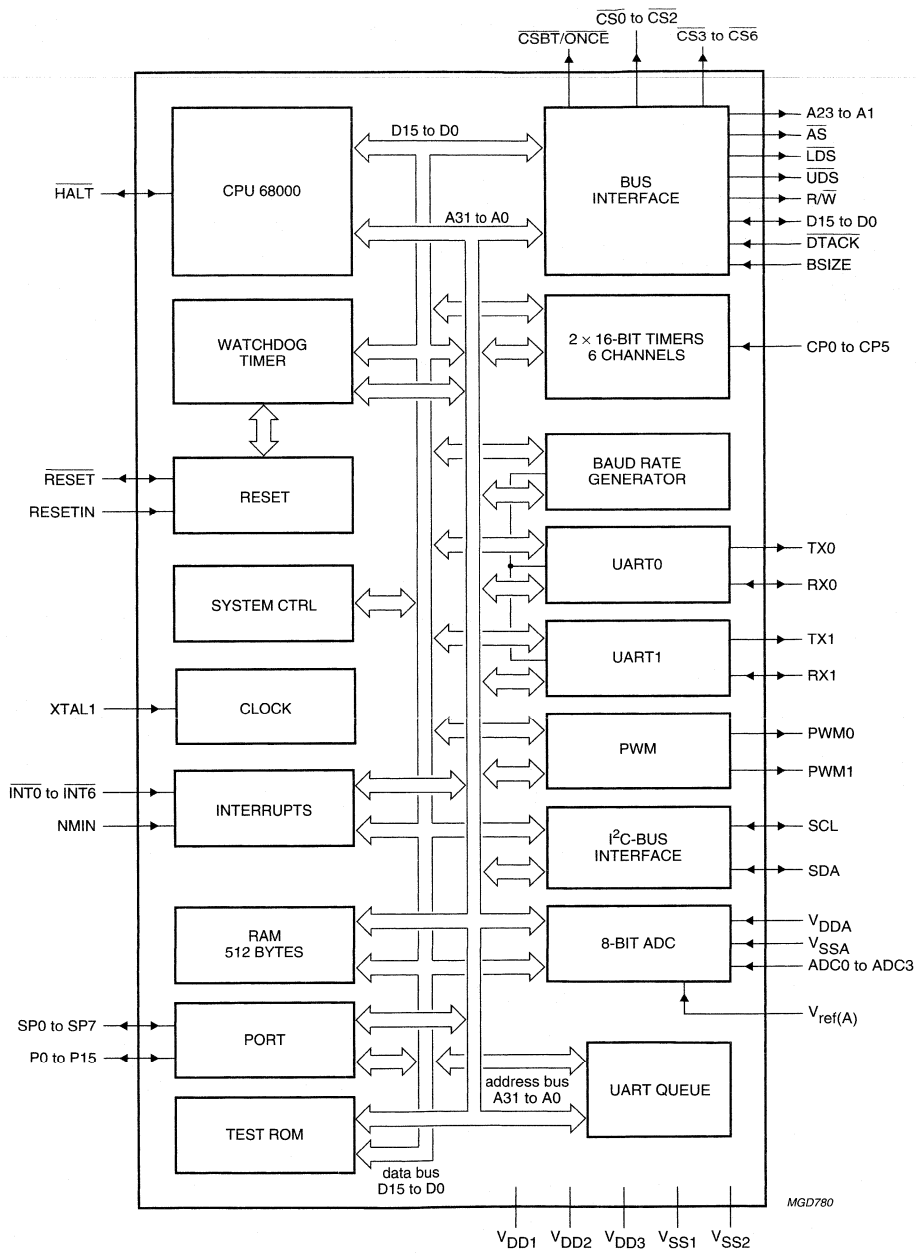


Fig.1 P90CL301BFH block diagram.

PINNING INFORMATION

Pinning

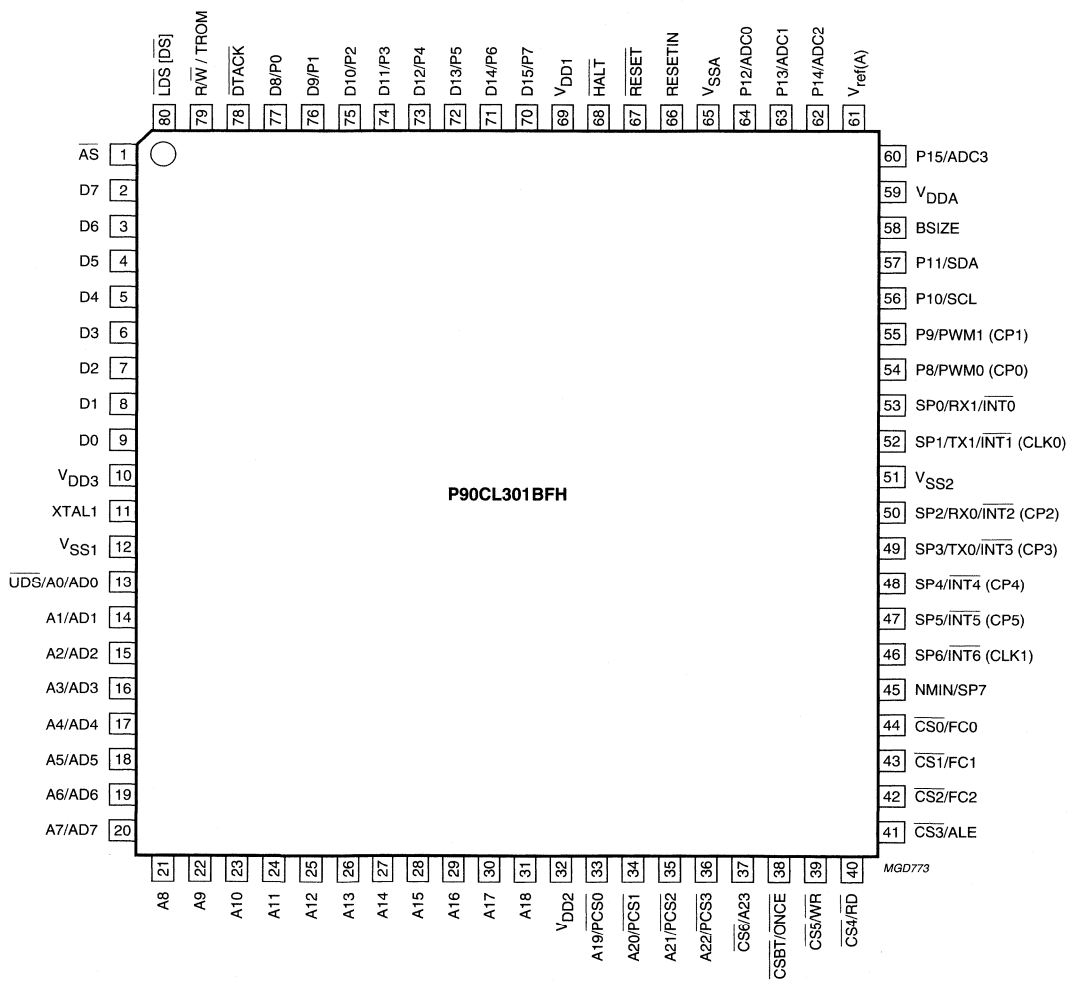


Fig.2 Pinning diagram of the P90CL301BFH (LQFP80).

Pin description

Table 1 Pin description for the P90CL301BFH

SYMBOL[1]	PIN	DESCRIPTION
$\overline{AS}$	1	address strobe
D7 to D0	2 to 9	lower 8-bits of data bus
V_{DD3}	10	supply voltage; third pin
XTAL1	11	external clock input
V_{SS1}	12	ground; first pin
$\overline{UDS}$/A0/AD0	13	upper data strobe or LSB of address bus or LSB of 8051 address/data
A1/AD1 to A7/AD7	14 to 20	lower 7-bits of the 68000 address bus or lower 7-bits of the 8051 bus
A8 to A18	21 to 31	upper 11-bits of the 68000 address bus
V_{DD2}	32	supply voltage; second pin
A19/$\overline{PCS0}$ to A22/$\overline{PCS3}$	33 to 36	upper 4-bits of the address bus or 8051 bus chip-select
$\overline{CS6}$/A23	37	chip-select 6 or address bit 23
$\overline{CSBT}$/$\overline{ONCE}$	38	chip-select boot or ONCE mode forced input
$\overline{CS5}$/$\overline{WR}$	39	chip-select 5 or 8051 bus write strobe
$\overline{CS4}$/$\overline{RD}$	40	chip-select 4 or 8051 bus read strobe
$\overline{CS3}$/ALE	41	chip-select 3 or 8051 bus address latch
$\overline{CS2}$/FC2 to $\overline{CS0}$/FC0	42 to 44	chip-select 2 to 0 or data bus function code 2 to 0
NMIN/SP7	45	Non-Maskable Interrupt or second port pin (bit 7)
SP6/$\overline{INT6}$ (CLK1)	46	second port pin (bit 6) external interrupt input 6 (external clock of timer 1)
SP5/$\overline{INT5}$ (CP5)	47	second port pin (bit 5) or external interrupt input 5 (Timer 1 capture input 5)
SP4/$\overline{INT4}$ (CP4)	48	second port pin (bit 4) or external interrupt input 4 (Timer 1 capture input 4)
SP3/TX0/$\overline{INT3}$ (CP3)	49	second port pin (bit 3) or Transmit data for UART0 or external interrupt input 3 (Timer 1 capture input 3)
SP2/RX0/$\overline{INT2}$ (CP2)	50	second port pin (bit 2) or Receive data for UART0 or external interrupt input 2 (Timer 0 capture input 2)
V_{SS2}	51	ground; second pin
SP1/TX1/$\overline{INT1}$ (CLK0)	52	second port pin (bit 1) or transmit data for UART1 or external interrupt input 1 (external clock of Timer 0)
SP0/RX1/$\overline{INT0}$	53	second port pin (bit 0) or receive data for UART1 or external interrupt input 0
P8/PWM0 (CP0)	54	port pin (bit 8) or PWM0 output (Timer 0 capture input 0)
P9/PWM1 (CP1)	55	port pin (bit 9) or PWM1 output (Timer 0 capture input 1)
P10/SCL	56	port pin (bit 10) or I^2C-bus Serial Clock.
P11/SDA	57	port pin (bit 11) or I^2C-bus Serial Data.
BSIZE	58	data bus size; 8 or 16-bit wide
V_{DDA}	59	ADC supply voltage
P15/ADC3	60	port pin (bit 15) or ADC input 3
$V_{ref(A)}$	61	ADC reference voltage
P14/ADC2 to P12/ADC0	62 to 64	port pin (bit 14 to bit 12) or ADC inputs 2 to 0
V_{SSA}	65	ADC ground
RESETIN	66	external Power-on-reset input

SYMBOL[1]	PIN	DESCRIPTION
$\overline{\text{RESET}}$	67	reset (bidirectional)
$\overline{\text{HALT}}$	68	halt (bidirectional)
V_{DD1}	69	supply voltage; first pin
D15/P7 to D8/P0	70 to 77	upper 8-bits of data bus or 8-bit Port 7 to Port 0; the selected function after reset is defined by pin BSIZE
$\overline{\text{DTACK}}$	78	data transfer acknowledge
R/$\overline{\text{W}}$ / TROM	79	read/write bus control or Test-ROM forced input
$\overline{\text{LDS}}$ [$\overline{\text{DS}}$]	80	lower data strobe [word data strobe]

Note

1. The following notation is used to describe the multiple pin definitions:
   a) Function1/Function2/Function3: multiplexed functions on the same pin. During and after reset the Function1 is selected.
   b) Function1 (Function2): function done in parallel.
   c) Function1 [Function2]: equivalent function.

CONTENTS

Pager baseband controller PCA5007

1 FEATURES

- Operating temperature from: −10 to +55 °C
- Supply voltage range with on-chip DC/DC converter: 0.9 to 1.6 V
- Low operating and standby current consumption
- On-chip DC/DC converter generates the supply voltage for the PCA5007 and external circuitry from a single cell battery
- Battery low detector
- Low electromagnetic noise emission
- Full static asynchronous 80C51 CPU (8-bit CPU)
- Recovery from lowest power standby Idle mode to full speed operation within microseconds
- 20 kbytes of One-Time Programmable (OTP) memory and 1-kbyte of RAM on-chip
- 27 general purpose I/O port lines (4 ports with interrupt possibility)
- 15 different interrupt sources with selectable priority
- 2 standard timer/event counters T0 and T1
- I²C-bus serial port (single 100 kHz master transmitter and receiver)
- Subset of standard UART serial port (8 and 9-bit transmission at 4800/9600 bits/s)
- 76.8 kHz crystal oscillator reference with digital clock correction for real time and paging protocol
- Real-Time Clock (RTC)
- Receiver and synthesizer control
  - Receiver control by software through general purpose I/Os
  - Synthesizer control by software through general purpose I/Os
  - 6-bit DAC for AFC to the receiver local oscillator
  - Dedicated protocol timer.
- Decoding of paging data
  - POCSAG or APOC phase 1, advanced high speed paging protocols are also supported
  - Supported data rates: 1200, 1600, 2400 and 3200 symbols/s using a 76.8 kHz crystal oscillator
  - Demodulation of Zero-IF I and Q 4 or 2 level FSK input or direct data input
  - Noise filtering of data input and symbol clock reconstruction
  - De-interleaving, error checking and correction, sync word detection address recognition, buffering and more is done in software
  - All user functions (keypad interface, alerter control, display, etc.) are implemented in software.
- Musical tone generator for beeper, controlled by the microcontroller
- Watchdog timer
- 48-pin LQFP package.

2 ORDERING INFORMATION

TYPE NUMBER[1]	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
PCA5007H/XXX	pre-programmed OTP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required OTP code.

3 GENERAL DESCRIPTION

The PCA5007 pager baseband controller is manufactured in an advanced CMOS/OTP technology.

The PCA5007 is an 8-bit microcontroller especially suited for pagers. For this purpose, features such as a 4 or 2 level FSK demodulator, filter, clock recovery, protocol timer, DC/DC converter optimized for small paging systems and RTC are integrated on-chip.

The device is optimized for low power consumption. The PCA5007 has several software selectable modes for power reduction: Idle and power-down mode of the microcontroller, and standby and off mode of the DC/DC converter.

The instruction set of the PCA5007 is based on that of the 80C51. The PCA5007 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

This data sheet details the properties of the PCA5007. For details of the I^2C-bus functions see *"The I^2C-bus and how to use it"*. For details on the basic 80C51 properties and features see *"Data Handbook IC20"*.

4 BLOCK DIAGRAM

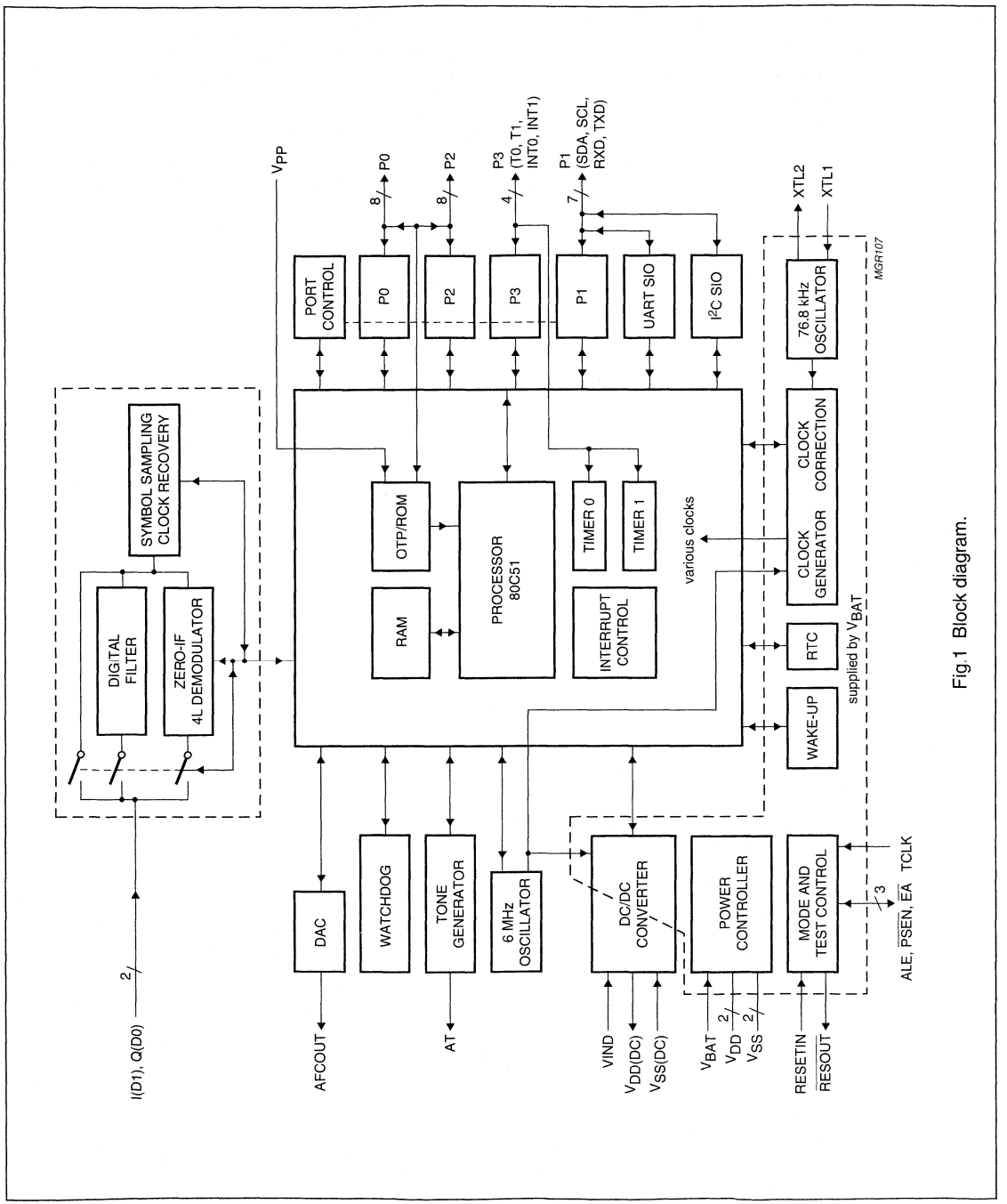


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
P3.4 and P3.5	1 and 2	I/O	**Port 3:** P3.4 and P3.5 are configured as push-pull output only (option 3R; see Section 6.6). Using the software input commands or the secondary port function is possible by driving the port 3 output lines accordingly: P3.4 secondary function: T0 (counter input for T0) P3.5 secondary function: T1 (counter input for T1)
AT	3	O	Beeper high volume control output. Used to drive external bipolar transistor.
P2.0 to P2.7	4 to 11	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups (option 1S; see Section 6.6.3). As inputs, port 2 pins that are externally pulled LOW will source current because of the internal pull-ups. (see Chapter "DC characteristics": I_{pu}). Port 2 emits the high-order address byte during fetches from external program memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 2 is also used to control the parallel programming mode of the on-chip OTP.
P0.0 to P0.4	12 to 16	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1S; see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during OTP programming verification.
V_{DDA}	17	S	supply voltage for the analog parts of the PCA5007 and the receiver/synthesizer control signals (Port 0 pins)
AFCOUT	18	O	Buffered analog output of DAC for automatic receiver frequency control. A voltage proportional to the offset of the receiver frequency can be generated. Can be enabled/disabled by software.
I(D1)	19	I	input from receiver: may be demodulated NRZ signal or Zero-IF. In phase limited signal
Q(D0)	20	I	input from receiver: may be demodulated NRZ signal or Zero-IF, Quadrature limited signal.
V_{SSA}	21	S	ground signal reference (for the analog parts) (connected to substrate)
P0.5 to P0.7	22 to 24	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1R,1R and 1S; see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during OTP programming verification.
P1.0 to P1.2	25 to 27	I/O	**Port 1:** Port 1 is an 8-bit quasi bidirectional I/O port with internal pull-ups. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled LOW will source current because of the internal pull-ups (see Chapter "DC characteristics": I_{pu}). P1.0 to P1.2 have external interrupts INT2 to INT4 assigned.
P1.3	28	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.3 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.3. This I/O then becomes the RXD/data line of the UART.

SYMBOL	PIN	TYPE	DESCRIPTION
P1.4	29	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.4 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.4. This I/O then becomes the TXD/clock line of the UART. P1.4 has external interrupt INT6 (X6) assigned.
V_{SS}	30	S	ground (connected to substrate)
V_{DD}	31	S	supply voltage for the core logic and most peripheral drivers of the PCA5007 (see V_{DDA})
ALE	32	I/O	**Address Latch Enable:** output pulse for latching the low byte of the address during an access to external memory.
$\overline{PSEN}$	33	I/O	**Program Store Enable:** the read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated for each code byte fetch.
$\overline{EA}$	34	I/O	**External Access Enable:** $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations 0000H to 4FFFH. If $\overline{EA}$ is held HIGH, the device executes from internal program memory unless the program counter contains an address greater the 4FFFH (20 kbytes).
TCLK	35	I	clock input for use as timing reference in external access mode and emulation
V_{PP}	36	S	Programming voltage (12.5 V) for the OTP. Is connected to V_{SS} in the application.
P1.6(SCL)	37	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.6 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.6. This I/O then becomes the clock line of the I^2C-bus. P1.6 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
P1.7(SDA)	38	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.7 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.7. This I/O then becomes the data line of the I^2C-bus. P1.7 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
XTL2	39	O	output from the current source oscillator amplifier
XTL1	40	I	input to the inverting oscillator amplifier and time reference for pager decoder, real-time clock and timers
V_{BAT}	41	S	Supply terminal from battery. Is used for supplying parts of the chip that need to operate at all times.
$V_{DD(DC)}$	42	O	Supply voltage output of the DC/DC converter. An external capacitor is required.
VIND	43	I	Current input for the DC/DC converter. The booster inductor needs to be connected externally.
$V_{SS(DC)}$	44	S	ground (connected to substrate) OTP
RESETIN	45	I	Schmitt trigger reset input for the PCA5007. External R and C need to be connected to the battery supply. All internal storage elements (except microcontroller RAM) are initialized when this input is activated.

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{\text{RESOUT}}$	46	O	Monitor output for the emulation system. Is active (LOW) whenever a reset is applied to the microcontroller. (a reset can be forced by RESETIN, watchdog or wake-up from DC/DC converter in off mode). A reset to the microcontroller initializes all SFRs and port pins; it has no impact on the blocks operating from V_{BAT}.
P3.2 to P3.3	47 and 48	I/O	**Port 3:** P3.2 and P3.3 are configured as push-pull output only (option 3R; see Section 6.6). Using the software input commands or the secondary port function is possible by driving the port 3 output lines accordingly: P3.2 secondary function: INT0 (external interrupt 0) P3.3 secondary function: INT1 (external interrupt 1)

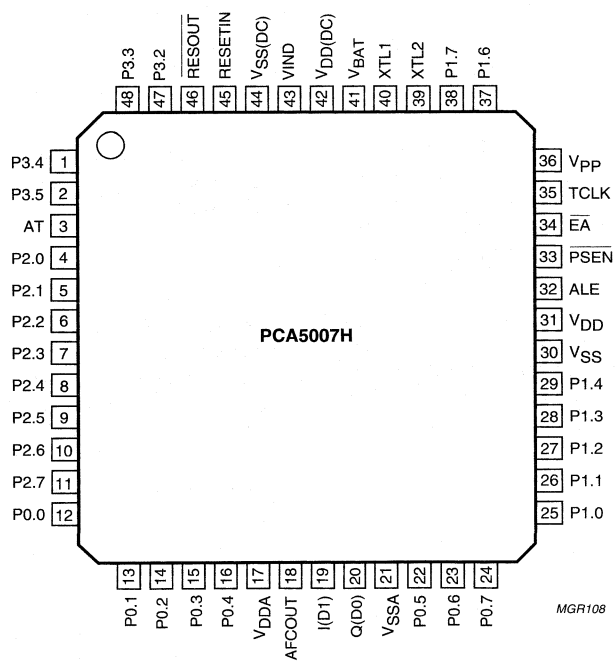


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCA5007 contains a high-performance CMOS microcontroller and the required peripheral circuitry to implement high-speed pagers for the modern paging protocols. For this purpose, features such as FSK demodulator, protocol timer, real-time clock and DC/DC converter have been integrated on-chip.

The microcontroller embedded within the PCA5007 implements the standard 80C51 architecture and supports the complete instruction set of the 80C51 with all addressing modes.

The PCA5007 contains 20 kbytes of OTP program memory; 1-kbyte of static read/write data memory, 27 I/O lines, two 16-bit timer/event counters, a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The PCA5007 devices have several software selectable modes of reduced activity for power reduction; Idle for the CPU and standby or off for the DC/DC converter. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The standby mode for the DC/DC converter allows a high efficiency of the latter at low currents and the off mode reduces the supply voltage to the battery level. In the off mode the RAM contents are preserved, the real-time clock and protocol timer are operating, but all other chip functions are inoperative.

Two serial interfaces are provided on-chip; a UART serial interface and an I^2C-bus serial interface. The I^2C-bus serial interface has byte oriented master functions allowing communication with a whole family of I^2C-bus compatible slave devices.

6.2 CPU timing

The internal CPU timing of the PCA5007 is completely different to other implementations of this core. The CPU is realized in asynchronous handshaking technology, which results in extremely low power consumption and low EMC noise generation.

6.2.1 BASICS

The implementation of the CPU of the PCA5007 as a block in handshake technology has become possible through the TANGRAM tool set, developed in the Philips Natlab in Eindhoven.

TANGRAM is a high level programming language which allows the description of parallel and sequential processes that can be compiled into logic on silicon. The CPU has the following features:

- No clock is needed. Every function within the CPU is self timed and always runs at the maximum speed that a given silicon die under the current operating conditions (supply voltage and temperature) allows.
- The CPU fetches opcodes with maximum speed until a special mode (e.g. Idle) is entered that stops this sequence.
- Only bytes that are required are fetched from the program memory. The dummy read cycles which exist in the standard 80C51 have been omitted to save power.
- To further speed up the execution of a program, the next sequential byte is always fetched from the code memory during the execution of the current command. In the event of jumps the prefetched byte is discarded.
- Since no clocks are required, the operating power consumption is essentially lower compared to conventional architectures and Idle power consumption is reduced to nearly zero (leakage only).
- Clocks are only required as timing references for timers/counters and for generating the timing to the off-chip world.

6.2.2 EXECUTION OF PROGRAMS FROM INTERNAL CODE MEMORY

When code is executed in internal access mode ($\overline{EA}$ = 1), the opcodes are fetched from the on-chip OTP. The OTP is a self timed block which delivers data at maximum speed. This is the preferred operating mode of the PCA5007.

6.2.3 EXECUTION OF PROGRAMS FROM EXTERNAL CODE MEMORY

When code is executed in external access mode ($\overline{EA}$ = 0), the opcodes are fetched from an off-chip memory using the standard signals ALE, $\overline{PSEN}$ and P0, P2 for multiplexed data and address information. In this mode the identical hardware configurations as for a standard 80C51 system can be used, even if the timing for ALE and $\overline{PSEN}$ is slightly different because it is generated from an internal oscillator.

6.3 Overview on the different clocks used within the PCA5007

Figure 3 gives an overview on the clocks available within the PCA5007 for the different functions.

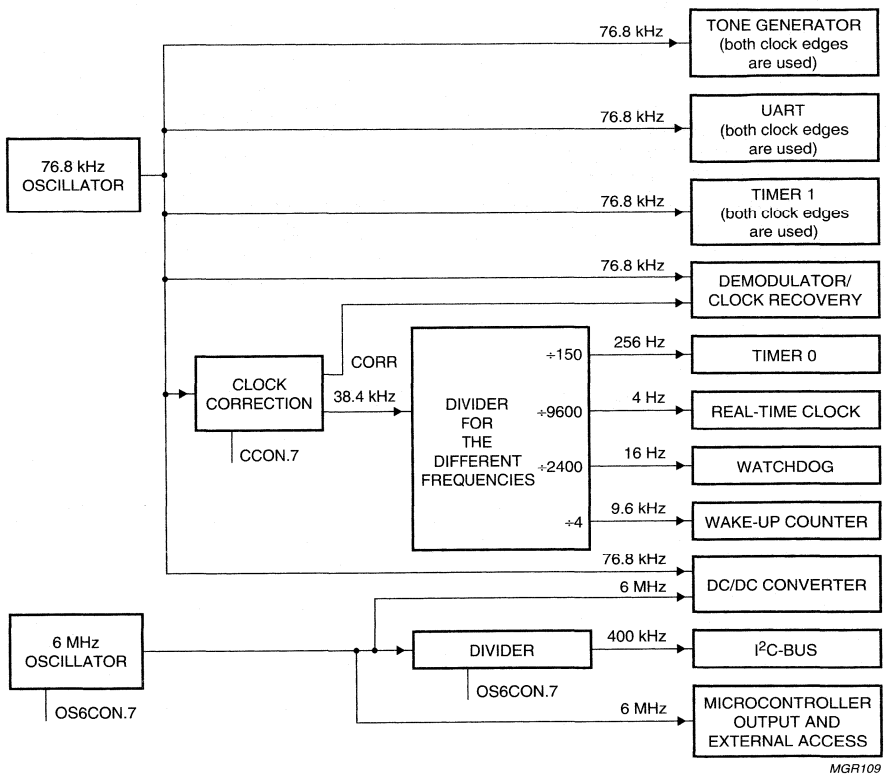


Fig.3 Overview on the clocks used within the PCA5007.

6.4 Memory organization

The PCA5007 has a program memory (OTP) plus data memory (RAM) on-chip. The device has separate address spaces for program and data memory (see Fig.4). If ports P0 and P2 are not used as I/O signals these pins can be used to address up to 64 kbytes of external program memory. In this case, the CPU generates the latch signal ($\overline{ALE}$) for an external address latch and the read strobe ($\overline{PSEN}$) for external program memory. External data memory is not supported.

6.4.1 PROGRAM MEMORY

After reset the CPU begins execution of the program memory at location 0000H. The program memory can be implemented in either internal OTP or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then program memory fetches are directed to the internal program memory. If the $\overline{EA}$ pin is strapped to V_{SS}, then program memory fetches are directed to external memory.

Programming the on-chip OTP is detailed in Chapter 15. Usually Philips will deliver programmed parts to a customer. Supply of blank engineering samples is possible, but then Philips cannot give any guarantee on the programmability and retention of the program memory.

6.4.2 DATA MEMORY

The PCA5007 contains 1024 bytes of internal RAM (consisting of 256 bytes standard RAM and 768 bytes AUX-RAM) and Special Function Registers (SFRs). Figure 4 shows the internal data memory space divided into the lower 128 bytes the upper 128 bytes and the SFR space and 768 bytes auxiliary RAM. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The SFR locations 128 to 255 are only directly addressable and the auxiliary RAM is indirectly addressable as external RAM (MOVX). External Data Memory (EDM) is not supported.

6.4.3 SPECIAL FUNCTION REGISTERS

The second 128 bytes are the address locations of the special function registers. Table 1 shows the special function registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 bit addressable locations in the SFR address space (those SFRs whose addresses are divisible by eight).

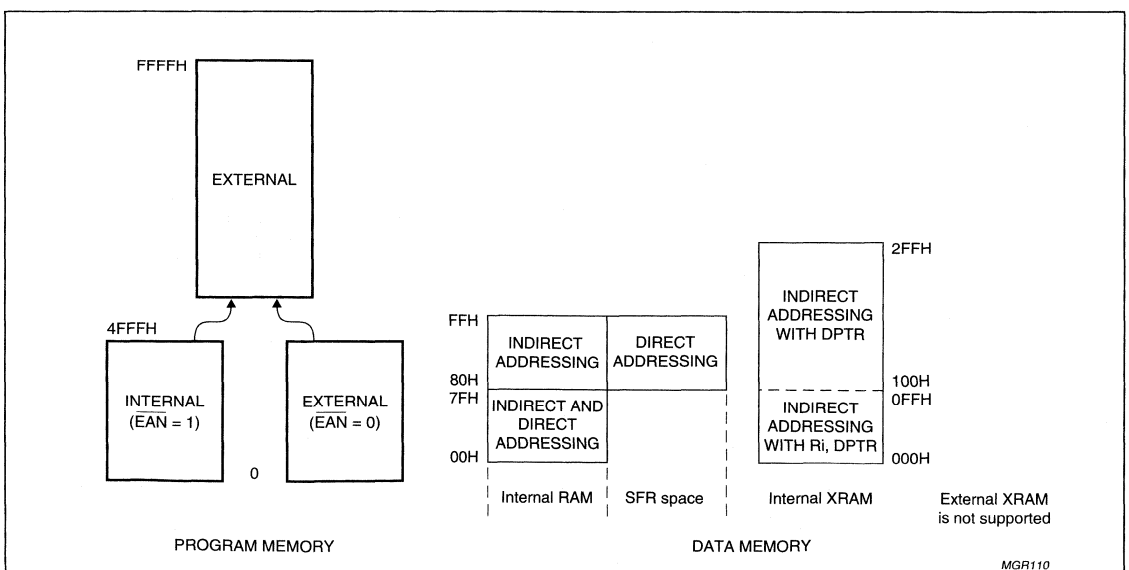


Fig.4 Memory map.

6.5 Addressing

The PCA5007 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register-Direct or Register-Indirect
- Maximum 1024 bytes of internal data RAM through Direct or Register-Indirect
  - Bytes 0 to 127 of internal RAM may be addressed directly/indirectly. Bytes 128 to 255 of internal RAM share their address location with the SFRs and so may only be addressed Register-Indirect as data RAM.
  - Bytes 0 to 768 of AUX-RAM can only be addressed indirectly via MOVX. Bytes 256 to 768 can only be addressed using indirect addressing with the data pointer, while bytes 0 to 255 may be also addressed using R0 or R1.
- Special function registers through Direct
- Program memory Look-Up Tables (LUTs) through Base-Register plus Index-Register-Indirect.

The PCA5007 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFRs), Arithmetic Logic Unit (ALU) and external data bus are all 8 bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

While the PCA5007 is executing code from the internal memory, ALE and $\overline{\text{PSEN}}$ pins are inactive with ALE = LOW and $\overline{\text{PSEN}}$ = HIGH.

External XRAM is not supported for this device, since P3.7 ($\overline{\text{RD}}$) and P3.6 ($\overline{\text{WR}}$) pins are not available. If the external XRAM is accessed accidentally, no $\overline{\text{PSEN}}$ or ALE cycle is done and actual P0 values are read. Internal XRAM access is not visible from outside the chip (no ALE, $\overline{\text{PSEN}}$, P0 and P2 activity).

Table 1 Special Function Registers Overview; note 1

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
80	P0									R/W	9FH	bit addressable
81	SP									R/W	07H	
82	DPL									R/W	00H	
83	DPH									R/W	00H	
87	PCON	SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL	R/W	00H	
88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	R/W	00H	bit addressable
89	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	R/W	00H	
8A	TL0									R/W	00H	
8B	TL1									R/W	00H	
8C	TH0									R/W	00H	
8D	TH1									R/W	00H	
90	P1									R/W	FFH	bit addressable
92	TGCON	ENB	CLK2	–	–	–	–	–	–	R/W	00H	
93	TG0									R/W	00H	
94	WUCON	RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET	R/W	00H	note 2
95	WUC0									R/W	00H	note 2
96	WUC1									R/W	00H	note 2
98	S0CON	SM0	SM1	–	REN	TB8	RB8	TI	RI	R/W	00H	bit addressable
99	S0BUF									R/W	00H	
9E	AFCON	ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0	R/W	00H	
A0	P2									R/W	FFH	bit addressable
A5	WDCON	COND	WD3	WD2	WD1	WD0	–	–	LD	R/W	00H	
A8	IEN0/IE	EA	EWU	ES1	ES0	ET1	EX1	ET0	EX0	R/W	00H	bit addressable
B0	P3									R/W	C3H	bit addressable
B8	IP/IP0	–	PWU	PS1	PS0	PT1	PX1	PT0	PX0	R/W	00H	bit addressable
C0	IRQ1	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2	R/W	00H	bit addressable
CD	RTCON	MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET	R/W	00H	note 2
CE	RTC0									R/W	00H	note 2
D0	PSW	CY	AC	F0	RS1	RS0	OV		P[3]	R/W	00H	bit addressable
D1	DCCON0	OFF	SBY	RXE	SBLI	–	–	STB[3]	BLI[3]	R/W	03H	
D2	DCCON1	VBG1	VBG0	VLO1	VLO0	–	–	–	–	R/W	00H	
D3	OS6CON	ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR	R/W	00H	
D4	OS6M0									R	00H	
D8	S1CON	–	ENS1	STA	STO	SI	AA	–	–	R/W	00H	bit addressable
D9	S1STA	SC4	SC3	SC2	SC1	SC0	0	0	0	R	78H	
DA	S1DAT									R/W	00H	
E0	ACC									R/W	00H	bit addressable
E8	IEN1	EMIN	EWD	EDC	EX6	ESC	EX4	EX3	EX2	R/W	00H	bit addressable
E9	IX1	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2	R/W	00H	

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
EC	DMD0	ENB	M	–	RES	LEV	BD2	BD1	BD0	R/W	00H	
ED	DMD1	ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0	R	00H	ENA is RW
EE	DMD2	ENC	–	BF	–	TEST	B2	B1	B0	R/W	00H	
EF	DMD3									R/W	00H	
F0	B									R/W	00H	bit addressable
F8	IP1	PMIN	PWD	PDC	PX6	PSC	PX4	PX3	PX2	R/W	00H	bit addressable
FC	CCON	ENB	PLUS	TEST	CIV17	CIV16	–	BYPAS	SET	R/W	00H	
FD	CC0	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0	R/W	00H	
FE	CC1	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8	R/W	00H	

Notes

1. An empty field in this map indicates a bit that can be read from or written to by software.
2. Value only reset with RESETIN and **not or only partly** with an off-restart sequence.
3. This bit cannot be changed by writing to it.

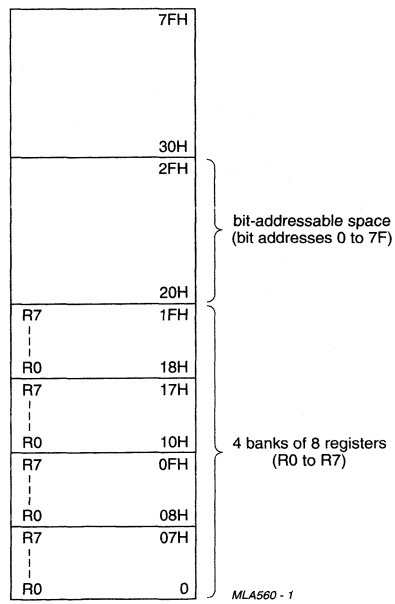


Fig.5 The lower 128 bytes of internal data memory.

6.6 I/O facilities

6.6.1 PORTS

The PCA5007 has 27 I/O lines treated as 27 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0 and 2 are complete, Port 1 has only 7 and Port 3 has only 4 pins externally available. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Is also used for external access, parallel OTP programming mode and emulation (see Table 2 for configuration details):

- Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals
- Provides access to the OTP data I/O lines in OTP parallel programming mode.

Port 1 Used for a number of alternative functions (see Table 3 for configuration details):

- Provides the inputs for the external interrupts INT2/P1.0 to INT4/P1.2 and INT6/P1.4
- SCL/P1.6 and SDA/P1.7 for the I^2C-bus interface are real open-drain outputs; no other port configurations are available
- RXD/P1.3 and TXD/P1.4 for the UART data input and output.

Port 2 Is also used for external access, parallel OTP programming mode and emulation (see Table 4 for configuration details):

- Provides the high-order address bus when expanding the device with external program memory
- Allows control of the on-chip OTP parallel programming mode.

Port 3 Pins are configured as strong push-pull outputs (see Table 5 for configuration details).
The following alternative Port 3 functions are available, but to avoid short-circuiting of the port pins, the input signals cannot be applied externally to the Port 3 pins. The alternative function can only be stimulated via the respective port output function:

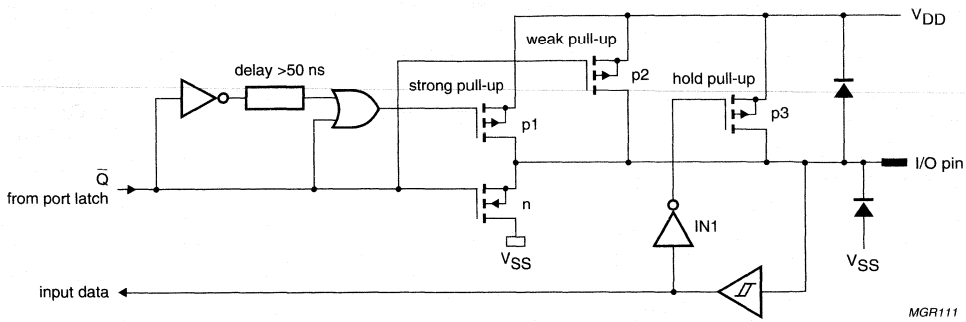
- External interrupt request inputs INT0/P3.2 and INT1/P3.3
- Counter inputs T0/P3.4 and T1/P3.5.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

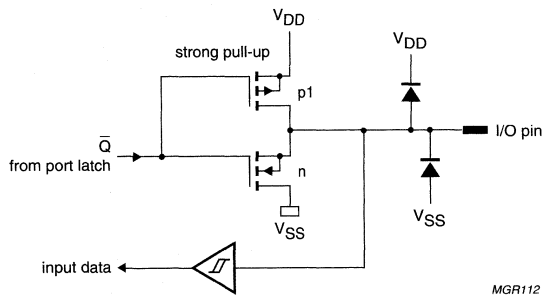
Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Standard ports have internal pull-ups. Figure 6a shows that the strong transistor p1 is turned on for only a short time after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter IN1. This inverter and p3 form a latch which holds the logic 1.

6.6.2 PORT I/O CONFIGURATION (OPTIONS)

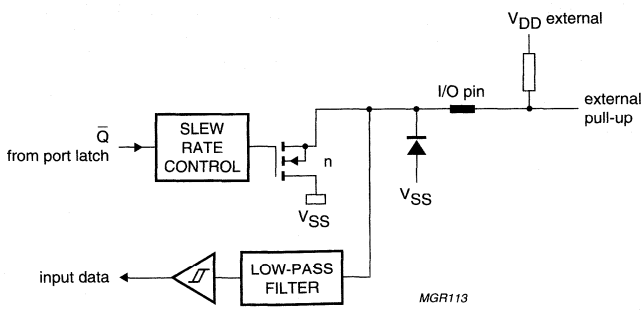
I/O port output configurations are determined on-chip according to one of the options illustrated in Fig.6. They cannot be changed by software.



a. Standard/quasi-bidirectional (option 1).



b. Push-pull (option 3).



c. Open-drain (only SDA/P1.7, SCL/P1.6; option 2).

Fig.6 Port configuration options.

6.6.3 PORT I/O CONFIGURATION

Tables 2 to 6 show the hardwired configuration for the different I/Os of the PCA5007.

Table 2 Port 0 configuration; notes 1 and 2

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P0.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_enable (O)
P0.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_enable (O)
P0.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_clock (O)
P0.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (O)
P0.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (I)
P0.5	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	RXE (O)
P0.6	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	ROE (O)
P0.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	bandwidth (O)/RSSI (I)

Notes

1. Option 1S means port configuration option 1 with post-reset set to HIGH; option 1R means post-reset state will be LOW.
2. 'hys' means input stage with hysteresis.

Table 3 Port 1 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P1.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	RXD
P1.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	TXD
P1.5	not available					
P1.6	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SCL
P1.7	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SDA

Table 4 Port 2 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.5	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.6	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

Table 5 Port 3 configuration

PORT PIN	CONFIGURATION	PULLUP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P3.0	not available					
P3.1	not available					
P3.2	push-pull output (option 3R)	no	hys	LOW	3 mA	call LED
P3.3	push-pull output (option 3R)	no	hys	LOW	3 mA	vibrator
P3.4	push-pull output (option 3R)	no	hys	LOW	3 mA	backlight
P3.5	push-pull output (option 3R)	no	hys	LOW	3 mA	LCD R/$\overline{W}$/RXD Enable
P3.6	not available					
P3.7	not available					

The port configuration is fixed and cannot be reconfigured by software or ROM code.

Table 6 Other pins

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
AT	push-pull output	no		LOW	3 mA	tone generator output
I(D1)	digital input	no	hys			
Q(D0)	digital input	no	hys			
TCLK	digital input	no	hys			
RESETIN	digital input	no	hys			reset input
$\overline{RESOUT}$	push-pull output	no		LOW	1.5 mA	reset output
XTL1	analog input/output (10 pF)	no	hys			to crystal quartz
XTL2	analog input/output (10 pF)	no				to crystal quartz
AFCOUT	analog output	no				
ALE	quasi bidirectional I/O	yes	hys	HIGH	1.5 mA	
$\overline{PSEN}$	quasi bidirectional I/O	yes	hys	HIGH	0.75 mA	
$\overline{EA}$	3-state I/O with bus keeper	hold	buffer	HIGH	0.75 mA	

6.7 Timer/event counters

The PCA5007 contains two 16-bit timer/event counters, Timer 0 and Timer 1, which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match
- Generate a Pulse Width Modulated (PWM) output signal.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0: 8-bit timer or 8-bit counter each with divide-by-32 prescaler

Mode 1: 16-bit time interval or event counter

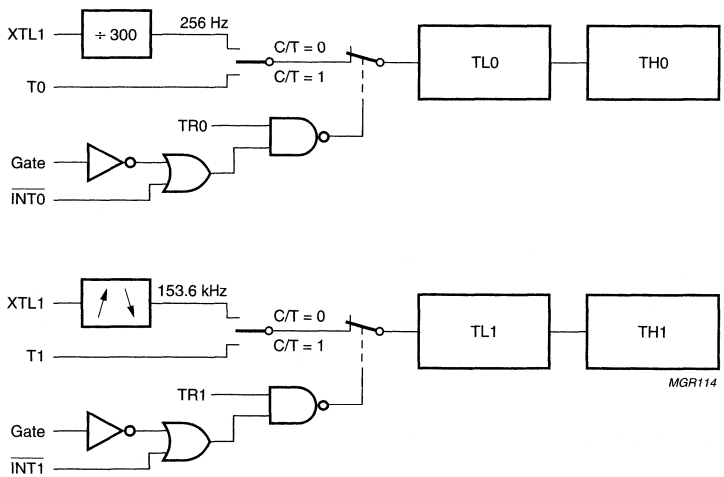
Mode 2: 8-bit time interval or event counter with automatic reload upon overflow

Mode 3: this mode of the standard 80C51 is not available.

In the timer mode the timers count events on the XTL1 input. Timer 0 counts through a prescaler at a rate of 256 Hz and Timer 1 counts directly on both edges of the XTL1 signal at a rate of 153.6 kHz. The nominal frequency of the XTL1 signal is 76.8 kHz.

In the counter mode, the register is incremented in response to a HIGH-to-LOW transition at P3.4 (T0) and P3.5 (T1).

Besides the different input frequencies and the non-availability of Mode 3, both Timer 0 and Timer 1 behave identically to the standard 80C51 Timer 0 and Timer 1.



Detailed configuration of the 4 available modes is found in the 80C51 family hardware description (*"Philips Semiconductors IC20 Data Handbook"*).

Fig.7 Timer/counter 0 and 1: clock sources and control logic.

6.8 I²C-bus serial I/O

The serial port supports the 2-line I²C-bus which consists of a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling. The implementation in the PCA5007 operates in single master mode as:

- Master transmitter
- Master receiver.

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register. The block diagram of the I²C-bus serial I/O is shown in Fig.8.

6.8.1 Differences to a standard I²C-bus interface

The I²C-bus interface of the PCA5007 implements the standard for master receiver and transmitter as defined in e.g. P83CL781/782 with the following restrictions:

- The baud rate is fixed to 100 kHz derived from the on-chip 6 MHz oscillator. Therefore bits CR0, CR1 and CR2 in the S1CON SFR are not available.
- Only single master functions are implemented.
  - Slave address (S1ADR) is not available
  - Status register (S1STA) reports only status defined for the MST/TRX and MST/REC modes
  - Multimaster operation is not supported.

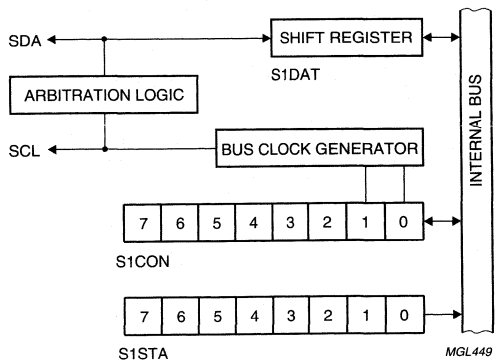


Fig.8 Block diagram of I²C-bus serial I/O.

6.8.2 Serial Control Register (S1CON)

Table 7 Serial Control Register (S1CON, SFR address D8H)

7	6	5	4	3	2	1	0
–	ENS1	STA	STO	SI	AA	–	–

Table 8 Description of the S1CON bits

BIT	SYMBOL	FUNCTION
S1CON.7	–	CR2 is not available.
S1CON.6	ENS1	**Enable Serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	**START flag**. If STA is set while the SIO is in master mode, SIO will generate a repeated START condition.
S1CON.4	STO	**STOP flag**. With this bit set while in master mode a STOP condition is generated. When a STOP condition is detected on the I²C-bus, the SIO hardware clears the STO flag.
S1CON.3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A START condition is generated in master mode • A data byte has been received or transmitted in master mode (even if arbitration is lost). If this flag is set, the I²C-bus is halted (by pulling down SCL). Received data is only valid until this flag is reset.
S1CON.2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • A data byte is received while the device is programmed to be a master receiver. When this bit is reset, no acknowledge is returned.
S1CON.1	–	CR1 and CR0 are not available.
S1CON.0	–	

6.8.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 9 Data Shift Register (S1DAT, SFR address DAH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.8.4 Address Register (S1ADR)

The slave address register is not available since slave mode is not supported.

6.8.5 Serial Status Register (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. S1STA is a read-only register. The status codes for all available modes of a single master I²C-bus interface are given in Tables 12 to 14.

Table 10 Serial Status Register (S1STA and SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 11 Description of the S1STA bits

BIT	SYMBOL	FUNCTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code
S1STA.0 to S1STA.2	–	these 3 bits are held LOW

Table 12 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received

Table 13 MST/REC mode

S1STA VALUE	DESCRIPTION
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned

Table 14 Miscellaneous

S1STA VALUE	DESCRIPTION
78H	no information available (reset value); the serial interrupt flag SI, is not yet set

Table 15 Symbols used in Tables 12 to 14

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	no acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

6.9 Serial interface SIO0: UART

The UART interface of the PCA5007 implements a subset of the complete standard as defined in e.g. the P80CL580.

6.9.1 Differences to the standard 80C51 UART

The following deviations from the standard exist:

- If [SM1 and SM0] = 10 then Mode 1 (8-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- If [SM1 and SM0] = 01 then Mode 2 (9-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- Modes 0 and 3 and the variable baud rate selection using Timer 1 overflow is not available
- The SM2 bit has no function
- The time reference for Modes 1 and 2 is taken from the 76.8 kHz oscillator, instead of the original $\frac{f_{osc}}{12}$

6.9.2 UART modes

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte has not been read by the time the reception of the second byte is complete, the second byte will be lost. The serial port receive and transmit registers are both accessed via the special function register S0BUF. Writing to S0BUF loads the transmit register and reading from S0BUF accesses a physically separate receive register.

The serial port can operate in 2 modes:

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a START bit (0), 8 data bits (LSB first) and a STOP bit (1). On receive, the stop bit goes into RB8 in special function register S0CON (see Figs 9 and 10).

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a START bit (0), 8 data bits (LSB first), a programmable 9th data bit and a STOP bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the STOP bit is ignored (see Figs 9 and 11).

In both modes the baud rate can be selected to either 4800 or 9600 depending on the SMOD bit in the PCON SFR. If SMOD = 0 the baud rate is 4800, if SMOD = 1 the baud rate is 9600 with a 76.8 kHz quartz crystal.

In both modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated by the incoming start bit if REN = 1.

6.9.3 Serial Port Control Register (S0CON)

The serial port control and status register is the special function register S0CON (see Table 16). The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 16 Serial Port Control Register (S0CON, SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	–	REN	TB8	RB8	TI	RI

Table 17 Description of the S0CON bits

BIT	SYMBOL	FUNCTION
S0CON.7	SM0	this bit together with the SM1 bit, is used to select the serial port mode; see Table 18
S0CON.6	SM1	this bit together with the SM0 bit, is used to select the serial port mode; see Table 18
S0CON.5	–	SM2 is not available
S0CON.4	REN	this bit enables serial reception and is set by software to enable reception, and cleared by software to disable reception
S0CON.3	TB8	this bit is the 9th data bit that will be transmitted in Mode 2; set or cleared by software as desired
S0CON.2	RB8	in Mode 2, this bit is the 9th data bit received; in Mode 1 it is the stop bit that was received
S0CON.1	TI	**The transmit interrupt flag**; Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission; must be cleared by software.
S0CON.0	RI	**The receive interrupt flag**; Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2); must be cleared by software.

Table 18 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	1	1	8-bit UART	$1/16 f_{osc}$ or $1/8 f_{osc}$
1	0	2	9-bit UART	$1/16 f_{osc}$ or $1/8 f_{osc}$

6.9.4 UART DATA REGISTER (S0BUF)

The UART data register (S0BUF) contains the serial data to be transmitted or data which has just been received. Bit 0 is transmitted or received first.

Table 19 Data Shift Register (S0BUF, SFR address 99H)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.9.5 BAUD RATES

The baud rate in Modes 1 and 2 depends on the value of the SMOD bit in SFR PCON and may be calculated as:

$$\text{Baud rate} = \frac{2^{SMOD}}{16} \times f_{osc}$$

- If SMOD = 0, (which is the value on reset), the baud rate is $1/16 f_{osc}$
- If SMOD = 1, the baud rate is $1/8 f_{osc}$.

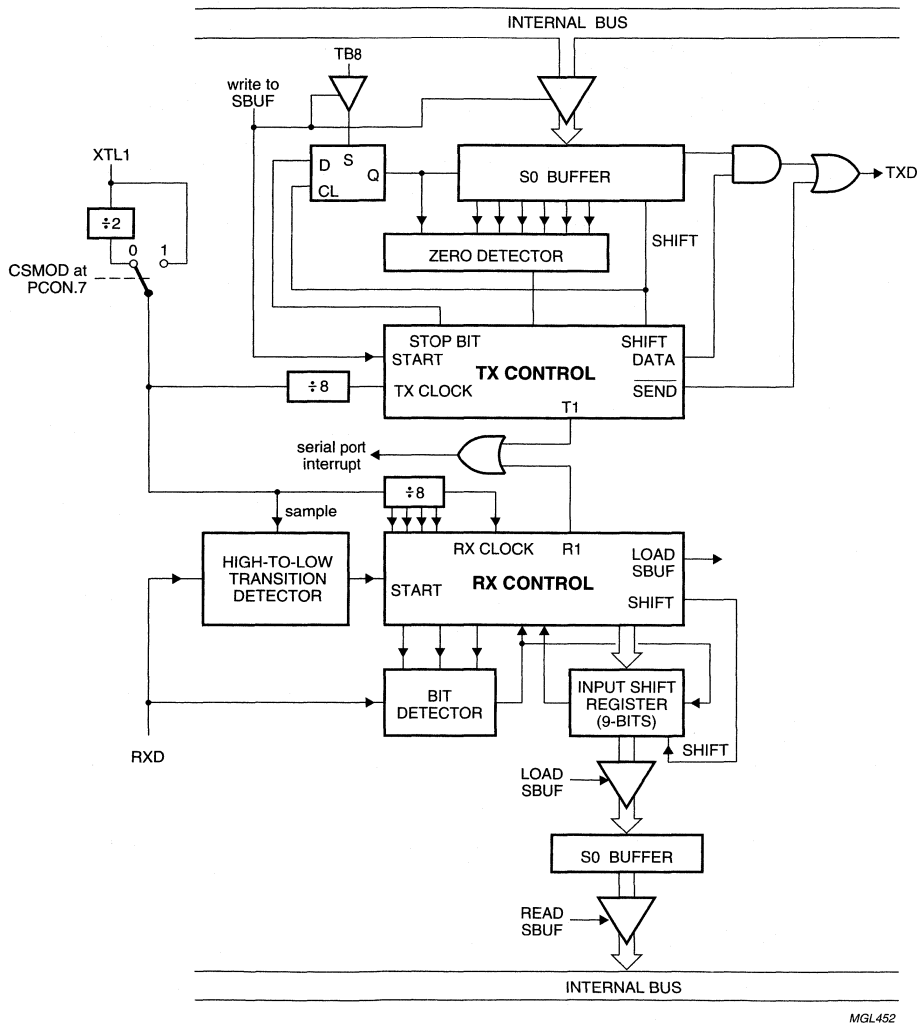


Fig.9 Serial port Mode 1and Mode 2.

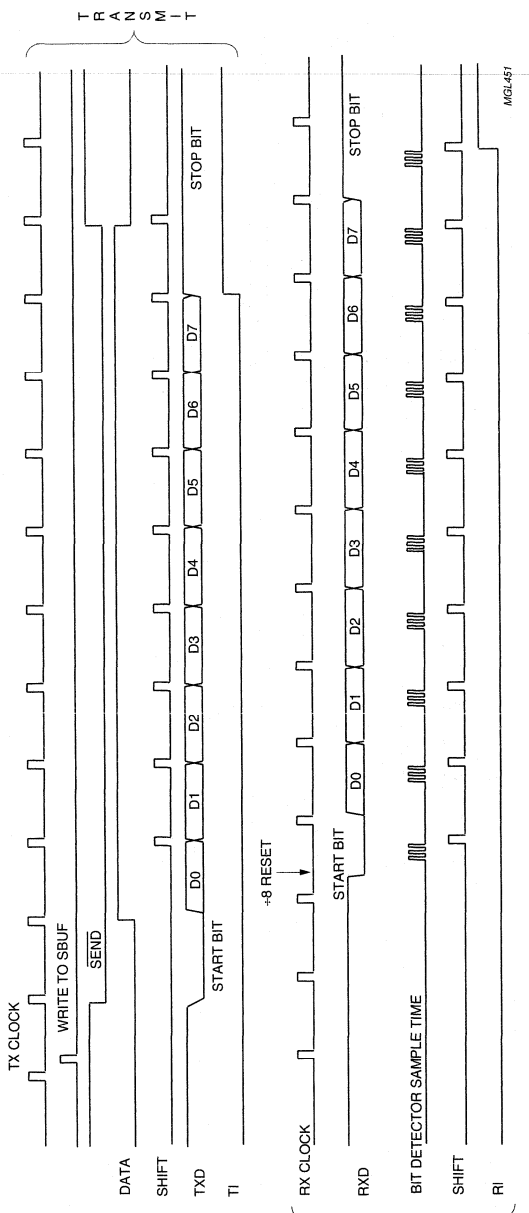


Fig.10 Serial port Mode 1 timing.

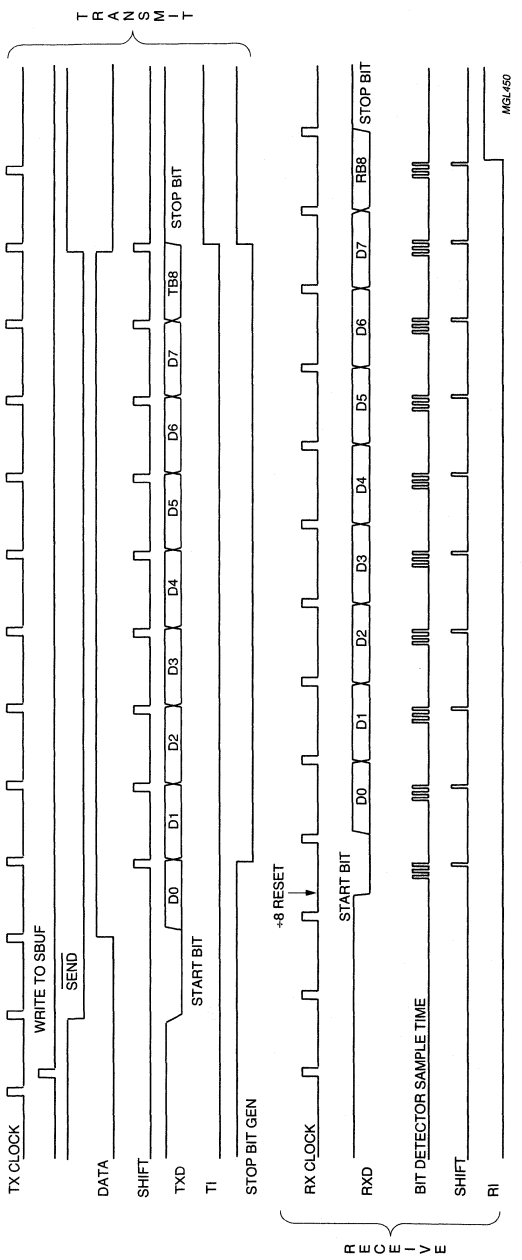


Fig.11 Serial port Mode 2 timing.

6.10 76.8 kHz oscillator

6.10.1 FUNCTION

The oscillator produces a reference frequency of 76.8 kHz. The frequency offset is compensated for by a separate digital clock correction block. The oscillator operates directly on V_{BAT} and is always enabled.

6.10.2 OSCILLATOR CIRCUITRY

The on-chip inverting oscillator amplifier is a single NMOS transistor supplied with a constant current. The amplitude visible at terminals XTL1 and XTL2 is therefore not a full rail swing with a very high impedance. To reduce the power consumption, the input Schmitt trigger buffer is limited to approximately 100 kHz maximum frequency.

The whole circuit operates directly at the battery supply. The 76.8 kHz oscillator cannot be disabled. It also continues its operation during DC/DC converter off or 8051 stop mode.

The simplest application configuration is shown in Fig.12a. C1 and C2 can be added to operate a crystal at its optimum load condition. The resulting capacitance of the series connection of C1 and C2 must be smaller than 5 pF for a guaranteed start-up of the oscillator.

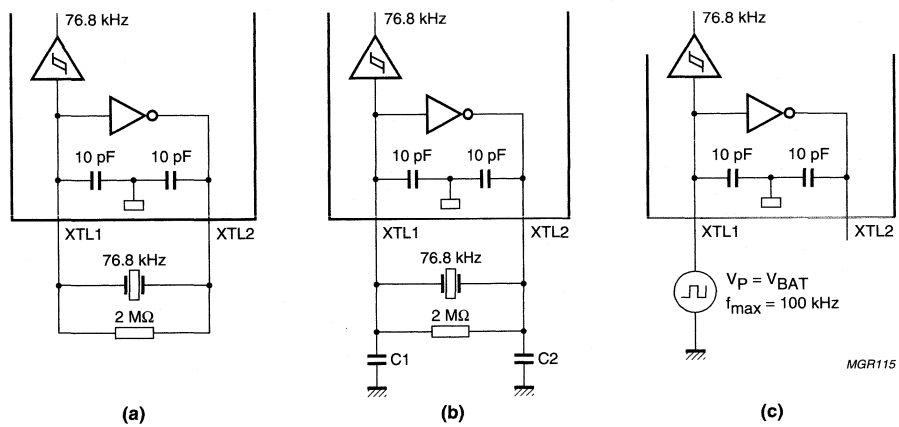


Fig.12 Oscillator circuit.

6.11 Clock correction

6.11.1 FUNCTION

The clock correction block is connected to the 76.8 kHz oscillator. It operates directly from V_{BAT}. By means of the clock correction circuit a digital adjustment of the 76.8 kHz oscillator signal is implemented.

An 18-bit interval counter inserts or deletes one pulse from the 76.8 kHz clock each time its count has expired. The interval is stored by the processor to the 18-bit interval register CIV. Addition or deletion is performed by hardware.

Crystal offset correction can be performed with a resolution of 5 ppm.

This block also generates the timing reference signals for other functional blocks such as the RTC (4 Hz), watchdog (16 Hz), Timer 0 (256 Hz), wake-up counter (9600 Hz) and the demodulator/clock recovery block. The generation of these timing references is always active and cannot be disabled.

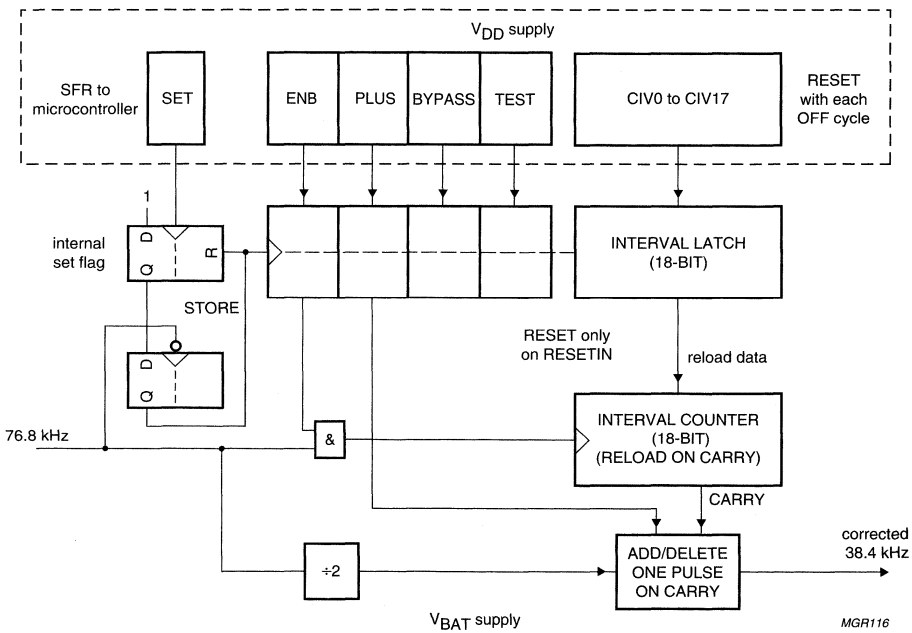


Fig.13 Block diagram for clock compensation.

6.11.2 Clock Correction Control Register (CCON)

The CCON special function register is used to control the clock correction by software.

Table 20 Clock Correction Control Register (CCON, SFR address FCH)

7	6	5	4	3	2	1	0
ENB	PLUS	TEST	CIV17	CIV16	–	BYPASS	SET

Table 21 Description of the CCON bits

BIT	SYMBOL	FUNCTION
CCON.7	ENB	**Enable clock correction**. If ENB = 1 has been set, then correction is enabled and will stay enabled even when the DC/DC converter is shut down and restarted.
CCON.6	PLUS	± **sign for value**. If PLUS = 1 then clock pulses are inserted, or else deleted.
CCON.5	TEST	**Test signal**, must always be logic 0 in normal mode. It is s used during test to bypass the first 9 FFs in the timing generator divider chain. If TEST = 1 the clock rate of the signals 9600 Hz and 256 Hz is doubled and the frequency on 16 Hz and 4 Hz is multiplied by 300.
CCON.4	CIV17	bit 17 of interval value, is used as extension of CC0 and CC1
CCON.3	CIV16	bit 16 of interval value, is used as extension of CC0 and CC1
CCON.2	–	unused.
CCON.1	BYPASS	**Test signal**, must always be logic 0 in normal mode. It is used during test to generate 76.8 kHz on all outputs of the timing generator (4 Hz, 16 Hz, 256 Hz and 9600 Hz).
CCON.0	SET	**A load signal to the interval register**. After a logic 0 to logic 1 transition of this bit the value of ENB, PLUS, TEST, BYPASS and CIV are copied into the local latches with the next 76.8 kHz clock pulse. The duration of one MOV instruction is long enough for the set operation to complete. The SFR values must remain stable for at least one oscillator period because the actual transfer happens synchronized with the local clock (see Figs 14 and 16).

6.11.3 Clock Correction Interval Registers (CC0 and CC1)

The CC0 and CC1 special function registers (together with CCON.3 and CCON.4) are used to define the interval between subsequent clock correction actions.

Table 22 Clock Correction Interval Register (CC0, SFR address FDH)

7	6	5	4	3	2	1	0
CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0

Table 23 Clock Correction Interval Register (CC1, SFR address FEH)

7	6	5	4	3	2	1	0
CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8

6.11.4 EXAMPLE SEQUENCE TO SET ANOTHER CLOCK CORRECTION INTERVAL

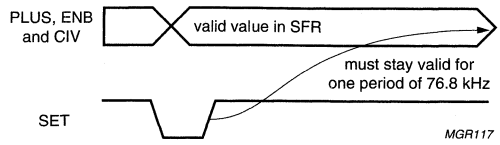


Fig.14 Sequence for setting the clock compensation.

MOV CC0, #(CIV7 to CIV0).

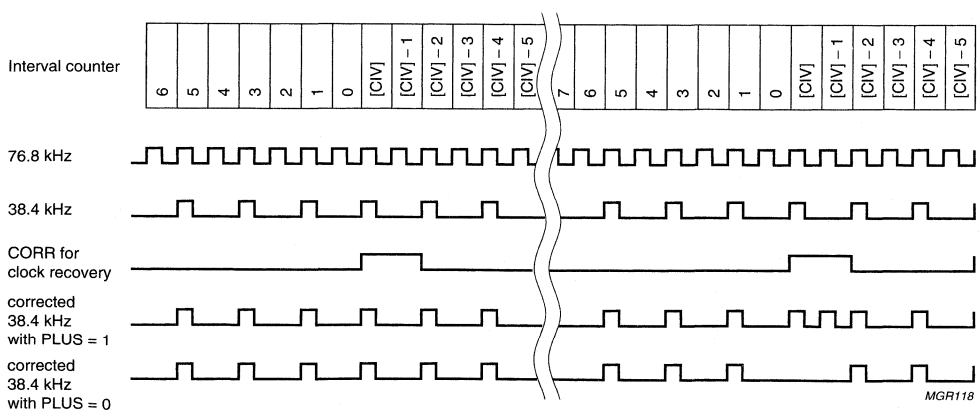
MOV CC1, #(CIV8 to CIV15).

MOV CCON, #D4H.

MOV CCON, #D5H.

6.11.5 TIMING

Figures 15 and 16 illustrate how the clock correction works and how the access of the microcontroller is synchronized to the local operation.



After (CIV) clock ticks of 76.8 kHz or 38.4 kHz one correction is made.

Fig.15 Operation of clock compensation.

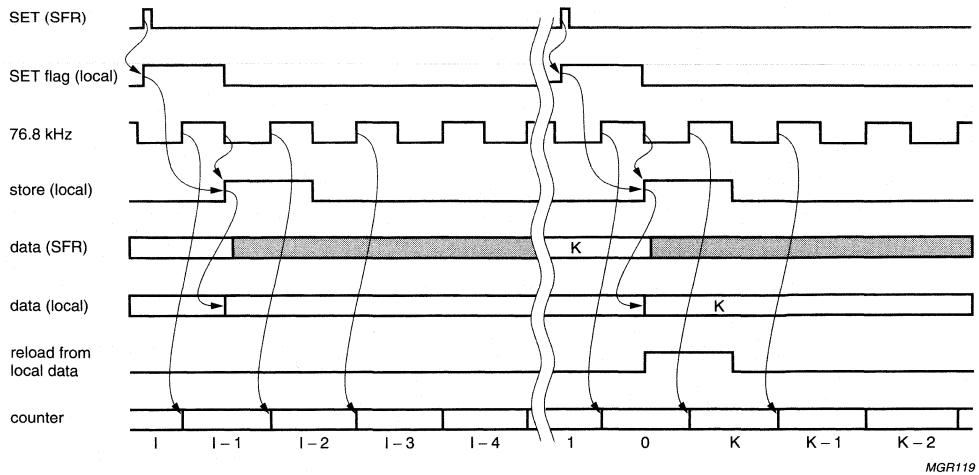


Fig.16 Synchronization of local counter operation and access from the microcontroller.

6.12 6 MHz oscillator

6.12.1 FUNCTION

The 6 MHz oscillator provides the clock for the DC/DC converter, the I²C-bus interface, the port I/Os and for the external memory access timing (ALE/$\overline{\text{PSEN}}$).

The 6 MHz oscillator is a 5 inverter stage current controlled ring oscillator. The oscillator is optimized for low operating current consumption.

The actual frequency of the oscillator can be measured by activating the MFR signal. An 8-bit counter will then be reset and will start counting at the first rising edge of the 76.8 kHz signal and will stop counting at the next rising edge of the 76.8 kHz signal. The processor then can read the contents of the MFR counter.

The processor can adjust the oscillator frequency using the F0 to F4 signals (control of source current for ring oscillator).

The 6 MHz oscillator is enabled by hardware only during the start-up phase and whenever the DC/DC converter needs the 6 MHz clock. In all other cases the 6 MHz oscillator is switched off by hardware.

The DC/DC converter does not need the 6 MHz clock when set in the standby mode.

If the 6 MHz output is required as a frequency source for other blocks (e.g. I²C-bus) the software needs to enable it explicitly by setting ENB = 1. Besides the DC/DC converter the following functions require the operation of the 6 MHz oscillator:

- I²C-bus block as basic time reference
- Port output logic. Software commands that write to the ports need this clock to complete the operation (if a program 'hangs', this could be the problem).
- Code fetching from external memories needs the clock for the ALE/$\overline{\text{PSEN}}$ timing (e.g. LJMP 5000H needs this clock for completion).

When the ENB bit has been set by software, the clock will be available internally after the start-up time of this oscillator. The start-up time is 2 to 3 periods of the 76.8 kHz reference frequency.

6.12.2 6 MHz Oscillator Control Register (OS6CON)

The OS6CON special function register is used to control the operation of the on-chip 6 MHz oscillator. The 6 MHz oscillator can be controlled as follows:

- It can be enabled or disabled. Disabling this oscillator when the DC/DC converter is in standby mode and no port I/O nor I^2C-bus activity is required saves current.
- The frequency of the oscillator can be adjusted by setting the SFx bits accordingly
- The actual frequency of the oscillator can be measured by writing the MFR bit to logic 1.

Table 24 6 MHz Oscillator Control Register (OS6CON, SFR address D3H)

7	6	5	4	3	2	1	0
ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR

Table 25 Description of the OS6CON bits

BIT	SYMBOL	FUNCTION
OS6CON.7	ENB	**Enable oscillator**. If ENB = 1 then the function is enabled. The enable bit is only cleared when the processor writes the bit to logic 0, or if the DC/DC converter is put into 'OFF' state and a reset is generated during the following power-up sequence.
OS6CON.6	–	unused
OS6CON.5	$\overline{SF4}$	**Set frequency**. This 5-bit value adjusts the current of the ring oscillator and thus the frequency. Writing a small value decreases the frequency. The nominal frequency of 6 MHz is assigned to code ($\overline{SF4}$, SF3, SF2, SF1 SF0) = 00000. The resolution of the frequency adjustment is 200 kHz per step, the range is approximately 3 to 9 MHz. In order to start with the nominal frequency the MSB bit is inverted in this SFR.
OS6CON.4	SF3	
OS6CON.3	SF2	
OS6CON.2	SF1	
OS6CON.1	SF0	
OS6CON.0	MFR	**Measure frequency**. If a positive pulse is issued on this SFR-bit a frequency measurement cycle is executed. The duration of this cycle is one period of 76.8 kHz. The count of 6 MHz periods during the measurement cycle is reported back in OS6M0. The bit must be reset by software.

6.12.3 6 MHz Oscillator Measured Frequency Register (OS6M0)

The actual frequency of the 6 MHz on-chip oscillator can be calculated from the value in the OS6M0 special function register, after a Measure Frequency operation (MFR).

Table 26 6 MHz Oscillator Measured Frequency Register (OS6M0, SFR address D4H)

7	6	5	4	3	2	1	0
MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0

The value stored in this SFR is the counted number of 6 MHz cycles during one 76.8 kHz period. The frequency of the 6 MHz oscillator is therefore f = MF × 76800 Hz with a resolution of 76800 Hz.

6.12.4 Enabling of the 6 MHz oscillator

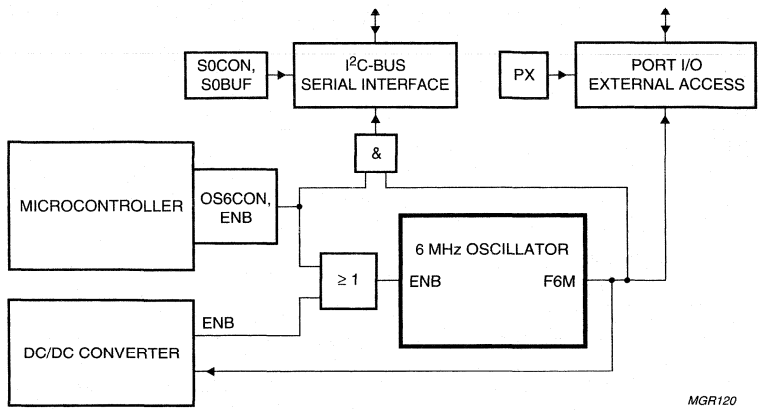


Fig.17 Relationship between 6 MHz oscillator, DC/DC converter and microcontroller.

6.13 Real-time clock

6.13.1 Function

The Real-Time Clock (RTC) consists of an 8-bit counter that is active at all times. To save power it is operated directly on V_{BAT}. It counts up on every 4 Hz clock pulse (corrected clock).

The RTC can be read from and written to by the processor. When it reaches 239, the signal MINUTE is activated. This signal resets the counter to 0 (at the next clock pulse), and generates a MIN-interrupt for the processor.
The microcontroller 'sees' the minute interrupt as if it was an X9 interrupt. It can be enabled and disabled and must be cleared as an X9 interrupt (CLR IQ9).

If the DC/DC converter is not active when this happens, the DC/DC converter is started first, and a power-up/restart sequence of the microcontroller follows. The MIN bit remains set during this procedure.

6.13.2 Real-Time Clock Control Register (RTCON)

The RTCCON special function register is used to control the operation of the on-chip real-time clock function.

Table 27 RTC Control Register (RTCCON, SFR address CDH)

7	6	5	4	3	2	1	0
MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET

Table 28 Description of the RTCON bits

BIT	SYMBOL	FUNCTION
RTCON.7	MIN	**MIN is activated when the counter reaches 239**. MIN is used to generate the interrupt request signal MINUTE. In order to complete the interrupt cycle and reset the interrupt source, the processor has to clear MIN. This must be done in a 2 step operation writing MIN and then applying a positive edge to SET.
RTCON.6	–	unused
RTCON.5	–	unused
RTCON.4	–	unused
RTCON.3	–	unused
RTCON.2	W/$\overline{R}$	Before the RTC time can be set by software, the updating of the SFR by the RTC must be disabled. This is done by writing the W/$\overline{R}$ bit to logic 1. The W/$\overline{R}$ bit is cleared by hardware after the next 4 Hz clock, when the RTC has been loaded with its next value.
RTCON.1	LOAD	**Load RTC with contents of RTC0**. LOAD is sampled with the positive edge of the set flag SET. If LOAD is not HIGH during a SET operation, only the MIN flag is (re)set by the command.
RTCON.0	SET	**Latch signal for the real-time clock**. With the pulse on SET the content of MIN is copied into the 'real' MIN latch. This is necessary because the RTC has to be active at all times independant of the microcontroller.

6.13.3 Real-Time Clock Data Register (RTC0)

Table 29 RTC Data Register (RTC0, SFR address CEH)

7	6	5	4	3	2	1	0
QSECS7	QSECS6	QSECS5	QSECS4	QSECS3	QSECS2	QSECS1	QSECS0

The value stored in this SFR is the actual 4 Hz count since the last MINUTE interrupt. The contents of this counter can be read from and written to by software. The contents of this counter are only initialized when RESETIN is activated. During an OFF sequence, the RTC continues its operation.

The value of the RTC data register is only updated while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is at logic 0 the real-time clock continues its operation, the MINUTE interrupt occurs regularly, but the SFR is not updated.

6.13.4 Example sequence for programming the RTC:

Sequence to set another value into the RTC:

MOV RTCON, #06H; set LOAD, W/$\overline{R}$ bits

MOV RTC0, #(new value); load new RTC value into SFR

MOV RTCON, #07H; now set the data valid flag (SET) in the SFR.

Sequence to clear an interrupt of the RTC:

CLR IQ9; Interrupt request flag is IQ9

MOV RTCON, #00H; clear also MIN flag in the SFR

MOV RTCON, #01H; now set the data valid flag (SET) in the SFR.

6.13.5 Timing

The interface between 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.13).

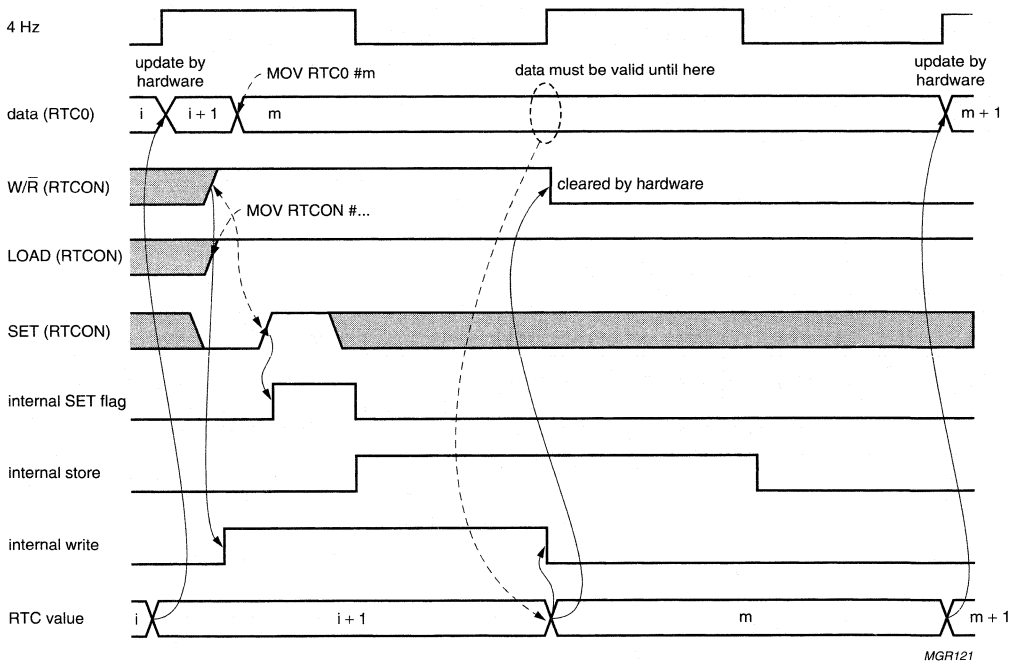


Fig.18 Operation of RTC to microcontroller interface.

6.14 Wake-up counter

6.14.1 FUNCTION

The wake-up counter is intended to be used as a protocol timer. It can be programmed to wake-up the processor when the protocol needs an action. Amongst others this may be:

- Switching on the DC/DC converter at time 0
- Enabling the receiver at time 1
- Enabling the demodulator and clock recovery function at time 2 before relevant data is expected.

The time to wake-up is defined as a 16-bit value containing the number of 9600 Hz ticks. The maximum time interval that can be spawn with one cycle then equals 6.8 s.

The wake-up counter and its reload latch are supplied by V_{BAT} and operate independent of the 2 V supply.

A reset to the microcontroller does not clear the wake-up counter control flags or the reload latch, but clears the reload register (see Fig.19).

The counter is implemented as a 16-bit ripple-down counter. It can be loaded from the wake-up reload latch by a signal from the processor. When the counter is loaded it automatically starts if the RUN signal is active. When the counter reaches zero the wake-up signal becomes active and may generate an interrupt. The wake-up signal automatically reloads the counter (modulo N counter). The counter is stopped when the RUN signal is written to logic 0. Auto reloading of the counter is also possible, when the DC/DC converter is not operating (i.e. V_{DD} is below 1.8 V).

The contents of the wake-up counter cannot be read by the processor. Reading WUC0 and WUC1 reflects the contents of the 16-bit wake-up register (set by the microcontroller).

The interface between the 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.14).

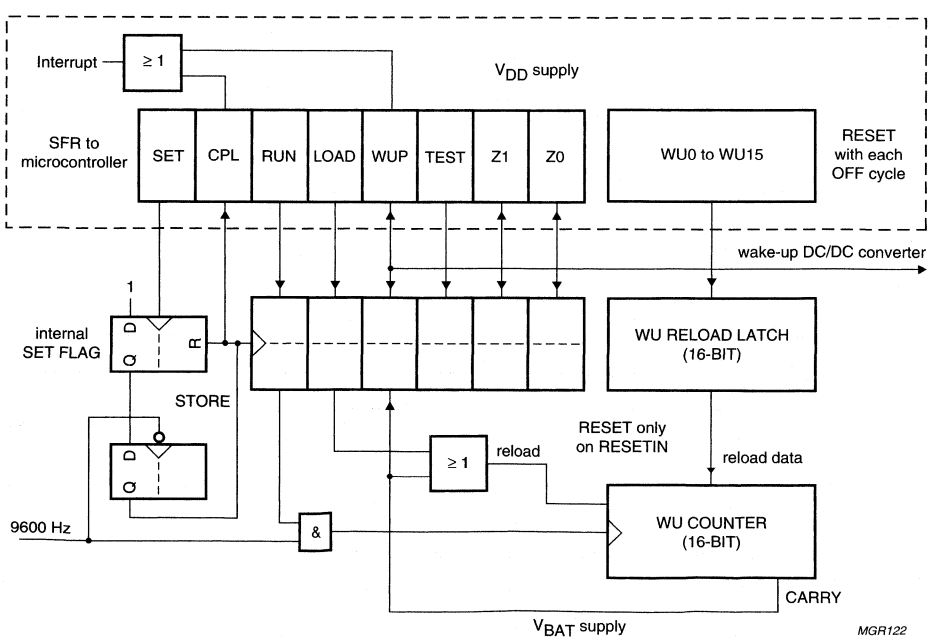


Fig.19 Block diagram of the wake-up counter.

6.14.2 Wake-Up Counter Control Register (WUCON)

The WUCON special function register is used to control the operation of the wake-up counter by software.

Table 30 Wake-up Counter Control Register (WUCON, SFR address 94H)

7	6	5	4	3	2	1	0
RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET

Table 31 Description of the WUCON bits

BIT	SYMBOL	FUNCTION
WUCON.7	RUN	Control signal from the processor.
WUCON.6	WUP	**Latched Wake-Up signal**. The bit is set by hardware (or software) and generates a wake-up interrupt if enabled and the DC/DC STB bit is set. The bit needs to be cleared by software (SFR and 1 V bits). A SET sequence is required to clear the flag on the 1 V side. Attention: reading the bit reads the contents of the 'real' wake-up flag on the 1 V side, (read/modify/write commands will fail on this bit).
WUCON.5	TEST	**Test control signal** (uses 76.8 kHz as clock input for high and low counter).
WUCON.4	CPL	**Set operation completed.** Bit set by hardware when the last operation is completed and the SFRs are again ready to accept new settings. The bit generates a wake-up interrupt if enabled. The bit needs to be cleared by software.
WUCON.3	Z1	2 bits that are only reset by a primary RESETIN. The bits can be written to and read from by the software. The bits are not cleared when the DC/DC converter is switched off. Same procedure for setting the bits as WU0 to WU15 (reading these bits returns the 'real' flags on the 1 V side; read/modify/write commands will fail on this bit).
WUCON.2	Z0	
WUCON.1	LOAD	**Load wake-up counter with contents of reload latch** (see Fig.19). Is sampled on the positive edge of SET.
WUCON.0	SET	Clock signal for writing to RUN or wake-up SFR (on 1 V level).

6.14.3 Wake-Up Data Registers (WUC0, WUC1)

The WUC0 and WUC1 special function registers are used to define the interval to the next wake-up interrupt.

Table 32 Low Wake-UP Register (WUC0, SFR address 95H)

7	6	5	4	3	2	1	0
WU7	WU6	WU5	WU4	WU3	WU2	WU1	WU0

Table 33 High Wake-UP Register (WUC1, SFR address 96H)

7	6	5	4	3	2	1	0
WU15	WU14	WU13	WU12	WU11	WU10	WU9	WU8

WU0 to WU15 is a 16-bit register that is loaded by the processor. The contents of this register will be loaded into a 16-bit reload latch with a positive pulse on SET and into the 16-bit ripple-down counter with a positive pulse on LOAD.

The value stored in the wake-up counter cannot be read by software. The contents of this counter are only initialized when RESETIN is activated. During an off sequence, the wake-up counter continues its operation.

The wake-up interrupt can only occur while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is at logic 0 the wake-up counter continues its operation, the WUP flag is set when expired (but can still be checked by software) but an interrupt is not generated.

6.14.4 Example sequence for controlling the wake-up counter

Sequence to set another reload value:

```
MOV WUC1, #(high VALUE)
MOV WUC0, #(low VALUE)
MOV WUCON, #82H; set RUN and LOAD bit
MOV WUCON, #83H; activate SET flag
MOV PCON, #01H; >>> IDLE, WAIT FOR CPL INTERRUPT.
```

6.14.5 Timing

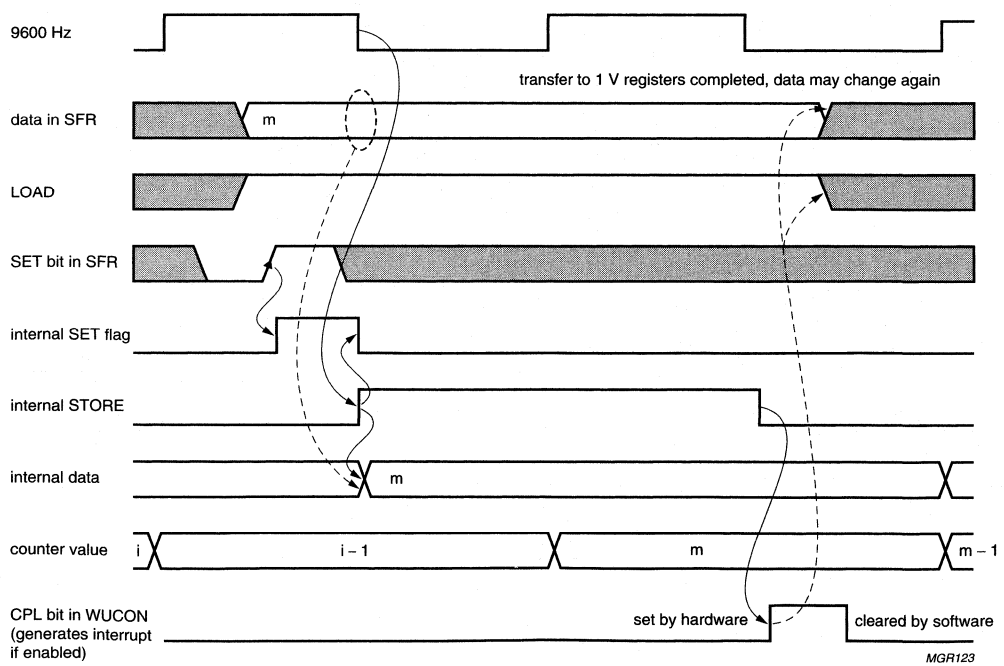


Fig.20 Operation of wake-up counter to microcontroller interface.

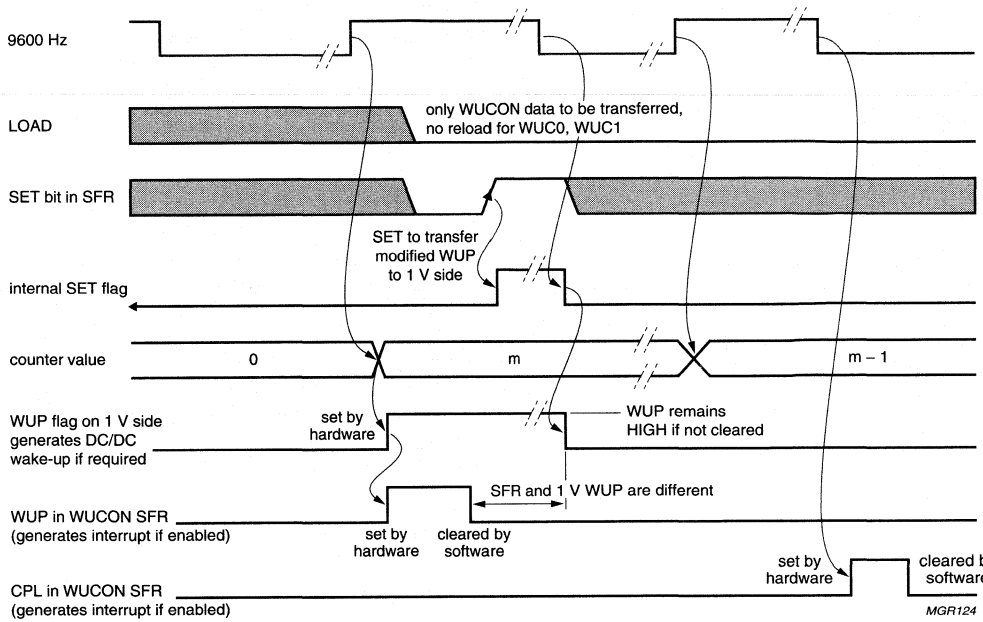


Fig.21 Wake-up interrupt sequence.

6.15 Tone generator

6.15.1 FUNCTION

The tone generator is implemented by a programmable divider from 76.8 kHz. An 8-bit value is used to define the cycle of a modulo N counter. The output of the modulo N counter is divided-by-2 to produce a symmetrical output signal. The counter is running when enabled.

The output frequency at the pin AT is defined as: $f_{AT} = \frac{76.8\ kHz}{TFREQ}$ if TFREQ ≥ 1. If TFREQ = 0 then f_{AT} = 76.8 kHz.

A secondary clock signal can be used as clock input to the modulo N counter. This input is required to generate the accurate resonance frequency of certain acoustic alerters (e.g. 512, 687, 1024, 1365, 2048, 2730, 4096).

The tone volume can be controlled by setting the frequency on or off alerter resonance.

6.15.2 INTERFACES

SFR ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TGCON (92H)	ENB	CLK2	–	–	–	–	–	–
TG0 (93H)	TFREQ7	TFREQ6	TFREQ5	TFREQ4	TFREQ3	TFREQ2	TFREQ1	TFREQ0

SFR:

- TFREQ0 to TFREQ7: 8-bit register containing the divisor of the tone. Loaded by the processor.
- ENB: Enable frequency generator. Control signal from processor.
- CLK2: Use secondary clock input for tone generation. If set a 32768 Hz clock signal is generated from the primary 76800 Hz clock signal and used as a timing reference for the tone generator.

Inputs:

- 76.8 kHz: Input to the tone counter.

Outputs:

- AT: Output for alerter. Is logic 0 when disabled:

$$f_{AT} = \frac{76.8\ kHz}{TFREQ}$$

6.15.3 Generation of the 32768 Hz reference

The 32768 Hz reference is generated from 76800 Hz according to the following algorithm:

```
forever do
  begin
    for 10 times do {
      from 7 clocks on 76.8 kHz generate
      3 pulses on 32 kHz
    }
    from 5 clocks on 76.8 kHz generate
    2 pulses on 32 kHz
  end
```

6.16 Watchdog timer

6.16.1 Function

The watchdog timer consists of an 8-bit down counter. The binary number defined with WD3 to WD0 defines the expiry time of the watchdog timer between 1 to 16 s. Once enabled this counter is running continuously. Once expired the timer produces firstly an interrupt and finally a reset. The software must reload the watchdog in regular intervals to avoid expiry.

A positive edge on the LD SFR bit (re)loads the counter with the value of WD3 to WD0, sets the LOW bits to logic 1 and activates this counter if it is not yet running. However, to prepare the (re)loading a positive edge must be applied to the COND bit in WDCON. In this way at least two locations in software must be passed before the counter can be reloaded. After reset the counter is not running. Only after the first LD it is clocked continuously by a clock pulse of 16 Hz until the DC/DC converter is switched off or an external reset is applied.

If the next LD signal is not given within the defined expiry interval an overflow occurs and the processor will be reset (signal WDR). A WDI interrupt is issued one clock cycle before the reset is applied. This gives the opportunity to avoid the reset if required. The maximum watchdog expiry time is thus 254 × 16 Hz ticks to the WD interrupt and 255 × 16 Hz ticks to the reset.

If the DC/DC converter is in the off mode, the watchdog timer is suspended.

6.16.2 WatchDog Timer Control Register (WDCON)

The WDCON special function register is used to control the operation of the on-chip watchdog timer.

Table 34 Watchdog Control Register (WDCON, SFR address A5H)

7	6	5	4	3	2	1	0
COND	WD3	WD2	WD1	WD0	–	–	LD

Table 35 Description of the WDCON bits

BIT	SYMBOL	FUNCTION
WDCON.7	COND	**Load condition**. Control signal from processor.
WDCON.6	WD3	WD0 to WD3 is the preset value for the high nibble of the watchdog timer. The value is the number of seconds to expiry of the watchdog.
WDCON.5	WD2	
WDCON.4	WD1	
WDCON.3	WD0	
WDCON.2	–	unused
WDCON.1	–	unused
WDCON.0	LD	**Load watchdog timer with WD0 to WD3**. Control signal from processor.

6.16.3 SAMPLE SEQUENCE TO RELOAD THE WATCHDOG

The sequence to reload the watchdog with 1 s is:

```
MOV WDCON, #80H; prepare condition.
MOV WDCON, #01H; reload the timer.
```

6.17 2 or 4-FSK demodulator, filter and clock recovery circuit

6.17.1 FUNCTION

The aim of the demodulator and clock recovery circuitry is to take the signal from the receiver, to format it into symbols and to transfer it to the processor. The two blocks use the 76.8 kHz clock.

The demodulator decodes the incoming signal and generates a sequence of NRZ data. This data is fed to the clock recovery block which regenerates the synchronization clock. This clock is used to sample and to shift the symbols into register DMD3.

6.17.1.1 Demodulator and filter

The demodulator can operate both with 2-FSK and 4-FSK (selected by the LEV bit). For both types of input signals the so called demodulator, filter and direct modes are allowed. The operational mode is selected on the basis of the M bit and BF bit.

In the demodulator mode (M = 0 and BF = X) the I and Q signals are decoded according to Table 36.

Operating in this mode, an offset compensation can be performed and the calculated offset value is stored into register DMD1, in the field AVG. The offset value can be used by the processor to adjust the analog AFC output voltage.

The offset coding is given in Table 37.

Both the filter and direct modes are intended for applications with an external demodulator. In this case, at the I and Q pins, there are fed NRZ data. In the 4-FSK situation the MSB is at pin I and the LSB is at pin Q. In the 2-FSK situation, only pin I is used; pin Q must be connected to V_{SS}. In these two modes, the offset calculation and compensation cannot be performed.

In the filter mode (M = 1 and BF = 0), the data is filtered and then sent to the clock recovery. In the direct mode (M = 1 and BF = 1), no function of the demodulator is performed. Consequently there is no filtering on the data which is sent directly to the clock recovery.

Table 36 Modulation coding

FREQUENCY (Hz)	2-FSK		4-FSK	
	D1	D0	D1	D0
+4800	1	X	1	0
+1600	1	X	1	1
−1600	0	X	0	1
−4800	0	X	0	0

Table 37 Offset coding (two's compliment)

OFFSET (Hz)	MAGNITUDE (AVG6 TO AVG0)
−9450	0111111
−9300	0111110
...	...
−300	0000010
−150	0000001
0	0000000
150	1111111
300	1111110
...	...
9300	1000001
9450	1000000

6.17.1.2 Clock recovery

The clock recovery regenerates the synchronization clock using the edges of the incoming NRZ data. When the NRZ data have no edges for a long time, the synchronization is maintained by means of the correction information from the clock correction block.

The recovered clock is used to sample and shift to left into an internal register one bit each symbol period in 2-FSK and two bits in 4-FSK. The symbol period is determined by bits BD2 to BD0. On the basis of BD bits the demodulator filter length is also set.

In the clock recovery, a pulse (SYMCLK) is generated each N-bit, where 'N' is defined by means of bits B2 to B0. This pulse is used to update the DMD3 register. Moreover, it can be used as an interrupt to the processor through the IRQ1.3 (symbol interrupt).

The interrupt informs the controller that 'N' bits are available in the DMD3 register.

6.17.2 Demodulator Control Register (DMD0)

The demodulator control register DMD0 contains the control bits for enabling the demodulator function and setting its mode and data rate.

Table 38 Demodulator Control Register (DMD0, SFR address ECH)

7	6	5	4	3	2	1	0
ENB	M	–	RES	LEV	BD2	BD1	BD0

Table 39 Description of the DMD0 bits

BIT	SYMBOL	FUNCTION
DMD0.7	ENB	enable demodulator function
DMD0.6	M	mode selection: logic 0 = I/Q from zero-IF receiver, logic 1 = NRZ data
DMD0.5	–	not used
DMD0.4	RES	reserved for future implementation
DMD0.3	LEV	if set to logic 0 2-FSK demodulation, if set to logic 1 4-FSK demodulation
DMD0.2	BD2	baud rate setting; see Table 40
DMD0.1	BD1	
DMD0.0	BD0	

Table 40 Baud rate for bits BD2, BD1 and BD0

BITS			BAUD RATE
BD2	BD1	BD0	
0	0	0	1200 symbols/s
0	0	1	2400 symbols/s
0	1	0	1600 symbols/s
0	1	1	3200 symbols/s
1	0	0	undefined
1	0	1	undefined
1	1	0	undefined
1	1	1	undefined

6.17.3 Demodulator Averaging Register (DMD1)

The demodulator averaging register DMD1 contains the control bit for enabling the averaging function, used for the offset compensation during demodulation and the coded average (offset) value.

Table 41 Demodulator Averaging Register (DMD1, SFR address EDH)

7	6	5	4	3	2	1	0
ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0

Table 42 Description of the DMD1 bits

BIT	SYMBOL	FUNCTION
DMD1.7	ENA	enable averaging function/offset calculation
DMD1.6	AVG6	7-bit value indicating the offset value of the demodulator. This is an indication of the LO offset frequency and will be used to determine the AFC output voltage. For coding see Table 37.
DMD1.5	AVG5	
DMD1.4	AVG4	
DMD1.3	AVG3	
DMD1.2	AVG2	
DMD1.1	AVG1	
DMD1.0	AVG0	

6.17.4 Clock Recovery Control Register (DMD2)

The clock recovery control register DMD2 contains the control bits for enabling the clock recovery function and setting its mode.

Whenever the clock recovery function is enabled (DMD2.7 = 1) the positive edge of the synchronized SYMCLK signal will force a SymClk interrupt through the IRQ1.3 request flag after [B2, B1 and B0] received bits (see Section 6.19 Table 50).

Table 43 Clock Recovery Control Register (DMD2, SFR address EEH)

7	6	5	4	3	2	1	0
ENC	–	BF	–	TEST	B2	B1	B0

Table 44 Description of the DMD2 bits

BIT	SYMBOL	FUNCTION
DMD2.7	ENC	enable clock recovery function
DMD2.6	–	not used
DMD2.5	BF	bypass demodulator filter
DMD2.4	–	not used
DMD2.3	TEST	reserved, should always beat logic 0
DMD2.2	B2	Select number of bits per interrupt:
DMD2.1	B1	If LEV = 0 then 000 = 1-bit, 001 = 2-bit to 111 = 8-bit
DMD2.0	B0	If LEV = 1 then 00X = 2-bit, 01X = 4-bit, 10X = 6-bit and 11X = 8-bit.

6.17.5 Demodulator Data Register (DMD3)

The demodulator data register DMD3 contains the (demodulated) recovered received symbols.

Table 45 Demodulator Data Register (DMD3, SFR address EFH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 46 Description of the DMD3 bits

BIT	SYMBOL	FUNCTION
DMD3.7	D7	Recovered symbols. The number of relevant bits are set with DMD2[2 to 0].
DMD3.6	D6	
DMD3.5	D5	
DMD3.4	D4	
DMD3.3	D3	
DMD3.2	D2	
DMD3.1	D1	
DMD3.0	D0	

6.18 AFC-DAC

6.18.1 FUNCTION

The AFC digital-to-analog converter provides an analog signal to the receiver to reduce its frequency offset. The analog signal is available at pin 18 (AFCOUT).

For low noise sensitivity the DAC output is buffered and can drive a load impedance of 10 kΩ (max.). The output swing is from rail-to-rail V_{DD}. When the enable signal ENB is at logic 1 a linear binary conversion is performed according to Table 47.

Below 0.2 V the linearity at the output voltage is not ideal.

When ENB is at logic 0 the AFCOUT pin is tied to V_{SS} and all currents are switched off.

Table 47 Coding of the AFC-DAC

CODE	OUTPUT VOLTAGE
000000	0
000001	$1 \times {}^{1}/_{64}V_{DD}$
...	...
N	$N \times {}^{1}/_{64}V_{DD}$
...	...
111111	$63 \times {}^{1}/_{64}V_{DD}$

6.18.2 AFC-DAC CONTROL/DATA REGISTER (AFCON)

The AFC-DAC Control/Data register AFCON contains the control bit for enabling the AFC-DAC and the data bits for setting the output voltage.

Table 48 AFC-DAC Control/Data Register (AFCON, SFR address 9EH)

7	6	5	4	3	2	1	0
ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0

Table 49 Description of the AFCON bits

BIT	SYMBOL	FUNCTION
AFCON.7	ENB	enable DAC output
AFCON.6	–	not used.
AFCON.5	AFC5	6-bit value for DAC output according to Table 47
AFCON.4	AFC4	
AFCON.3	AFC3	
AFCON.2	AFC2	
AFCON.1	AFC1	
AFCON.0	AFC0	

6.19 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Fig.27. The PCA5007 acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT4 and INT6
- Timer 0 and Timer 1
- Wake-up counter
- I^2C-bus serial I/O
- UART transmitter and receiver
- Demodulator
- DC/DC converter
- Watchdog timer
- Real-time clock (MINUTE).

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (IEN0 and IEN1).
The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

6.19.1 Overview

The interrupt controller implemented in the PCA5007 has 15 interrupt sources, of which some are level sensitive and some are edge sensitive. The interrupt controller samples all active sources during one instruction cycle; evaluation of the interrupts is then performed. A priority decoder decides which interrupt is serviced. Each interrupt has its own vector pointing to an 8 bytes long program segment. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt i.e. only two interrupt levels are possible. Between the RETI instruction (Return from Interrupt) and the LCALL to a next interrupt, there is at least one instruction of the lower program level executed (see Fig.22).

An interrupt is performed with a long subroutine call (LCALL) to vector address, which is determined by the respective interrupt. During LCALL the PC is pushed onto the stack. Returning from interrupt with RETI, the PC is popped from the stack.

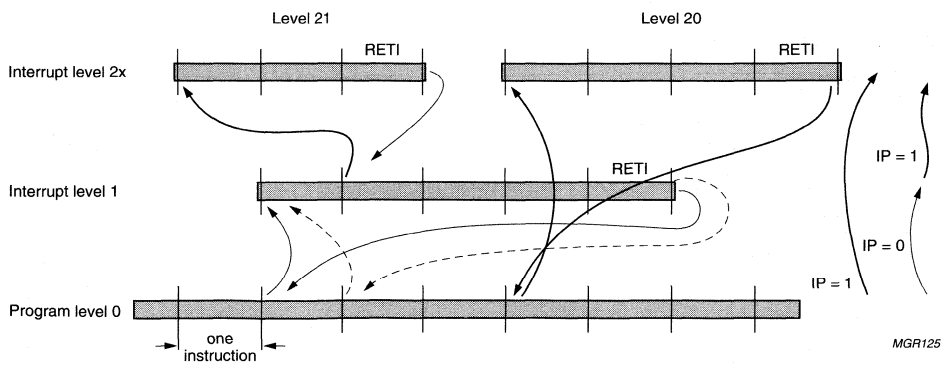


Fig.22 Interrupt hierarchy.

6.19.2 INTERRUPT PROCESS

Sample the interrupt lines: The interrupt lines are latched at the beginning of each instruction cycle.

Analyse the requests: The sampled interrupt lines will be analysed with respect to the relevant Interrupt Enable register (IEx) and Interrupt Priority register (IPx).
The process will deliver the vector of the highest interrupt request and the priority information. Depending on the interrupt level and the priority of the interrupt in progress, an interrupt request to the core is performed. The vector address will be passed to the core process.

Interrupt request to core:

Level 0: The interrupt request to the core is performed, when at least one instruction is performed since the RETI from Level 1.

Level 1: The interrupt request is performed, when at least one instruction is performed since the RETI from Level 21 and the request has high priority.

Level 20: No request is performed.

Level 21: No request is performed.

Emulation: In break mode no interrupt request is performed.

Update the interrupt level:

Level 0: In the event of a high priority interrupt the new level will be Level 20. If it is a low priority interrupt, the new level will be Level 1.

Level 1: In the event of a high priority interrupt, the new level will be Level 21. A low priority interrupt is not performed, the level is unchanged. On RETI the new level will be Level 0.

Level 20: On RETI, the new level is Level 0.

Level 21: On RETI, the new level is Level 1.

Level 1: On RETI, the new level is Level 0.

Level 0: The new level is Level 0.

Clearing the flags: During the forced LCALL the interrupt flag of the relevant interrupt is cleared by hardware, if applicable, otherwise by software.

Emulation: During emulation the interrupts may be disabled. This is performed during break mode. With $\overline{\text{INTD}}$ asserted, all the interrupts are disabled.

Idle or power-down: When Idle (PCON.0) or power-down (PCON.1) is set, the interrupt controller waits for the according WUI signal. Because the interrupt controller is waiting for WUI, all activity in the circuit will be stopped, thus no handshake can be completed. The WUI signal for Idle is the OR of all the interrupt request bits and the reset. For power-down the WUI signal is built only with the Port 1 interrupt request flags and the reset.

6.19.3 INTERRUPT CONTROLLER RELATED SFRS

The implementation of the interrupt controller related SFRs for enabling and disabling interrupts is identical to a standard 80C51, but the interrupt sources have been changed according to Table 50.

Table 50 Interrupt controller related SFRs: IEN0 (A8H), IEN1 (E8H), IP0 (B8H), IP1 (F8H), IRQ1 (C0H), TCON (88H), WUCON (94H) and RTCON (CDH)

BITS	CONV. NAME	SOURCE	NOTES
IEN0 address A8H: interrupt enable for X0, X1, T0, T1, T2, S0, S1 and global interrupt enable (note 1)			
0	EX0	P3.2	Enables or disables EXTERNAL0 interrupt. If EX0 = 0, the external interrupt 0 is disabled.
1	ET0	TIMER 0	Enables or disables the TIMER 0 overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
2	EX1	P3.3	Enables or disables the EXTERNAL1 interrupt. If EX1 = 0, external interrupt 1 is disabled.
3	ET1	TIMER 1	Enables or disables TIMER 1 overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
4	ES0	UART	Enables or disables the UART interrupt. If ES0 = 0, the UART interrupt is disabled.
5	ES1	I^2C	Enables or disables the I^2C-bus interrupt. If ES1 = 0, the I^2C-bus interrupt is disabled.
6	ET2	WAKE-UP	Enables or disables the WAKE-UP interrupt. If ET2 = 0, the wake-up interrupt is disabled.
7	EA	/	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
IEN1 address E8H: interrupt enable for X2 to X9 (note 1)			
0	EX2	P1.0	Enables or disables interrupts on P1.0. If EX2 = 0, the corresponding interrupt is disabled.
1	EX3	P1.1	Enables or disables interrupts on P1.1. If EX3 = 0, the corresponding interrupt is disabled.
2	EX4	P1.2	Enables or disables interrupts on P1.2. If EX4 = 0, the corresponding interrupt is disabled.
3	EX5	SYMBOL	Enables or disables the SYMBOL interrupt. If EX5 = 0, the SYMBOL interrupt is disabled.
4	EX6	P1.4	Enables or disables interrupts on P1.4. If EX6 = 0, the corresponding interrupt is disabled.
5	EX7	DC/DC	Enables or disables the DC/DC CONVERTER interrupt. If EX7 = 0, the DC/DC converter interrupt is disabled.
6	EX8	WDI	Enables or disables interrupts on the WATCHDOG. If EX8 = 0, the WDINT interrupt is disabled.
7	EX9	MIN	Enables or disables REAL-TIME CLOCK interrupt. If EX9 = 0, the MINUTE interrupt is disabled.
IP0 address B8H: interrupt priority for X0, X1, T0, T1, T2, S0 and S1 (note 2)			
0	PX0	P3.2	Defines the EXTERNAL0 interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.
1	PT0	TIMER 0	Enables or disables the TIMER 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
2	PX1	P3.3	Defines the EXTERNAL1 interrupt priority level. PX1 = 1 programs it to the higher priority level.
3	PT1	TIMER 1	Defines the TIMER 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.

BITS	CONV. NAME	SOURCE	NOTES
4	PS0	UART	Defines the UART interrupt priority level. PS0 = 1 programs it to the higher priority level.
5	PS1	I^2C	Defines the I^2C-bus interrupt priority level. PS1 = 1 programs it to the higher priority level.
6	PT2	WAKE-UP	Defines the WAKE-UP interrupt priority level. PT2 = 1 programs it to the higher priority level.
7	–	/	unused
IP1 address F8H: interrupt priority for X2 to X9 (note 2)			
0	PX2	P1.0	Defines the EXTERNAL2 interrupt priority level 1. PX2 = 1 programs it to the higher priority level.
1	PX3	P1.1	Defines the EXTERNAL3 interrupt priority level 1. PX3 = 1 programs it to the higher priority level.
2	PX4	P1.2	Defines the EXTERNAL4 interrupt priority level 1. PX4 = 1 programs it to the higher priority level.
3	PX5	SYMBOL	Defines the SYMBOL interrupt priority level 1. PX5 = 1 programs it to the higher priority level.
4	PX6	P1.4	Defines the EXTERNAL6 interrupt priority level 1. PX6 = 1 programs it to the higher priority level.
5	PX7	DC/DC	Defines the DC/DC CONVERTER interrupt priority level 1. PX7 = 1 programs it to the higher priority level.
6	PX8	WDI	Defines the WATCHDOG interrupt priority level 1. PX8 = 1 programs it to the higher priority level.
7	PX9	MIN	Defines the REAL-TIME CLOCK interrupt priority level 1. PX9 = 1 programs it to the higher priority level.
TCON address 88H: timer/counter mode control register			
0	IT0	P3.2	**EXTERNAL0 interrupt type control bit**. Set/cleared by software to specify falling edge/low level triggered external interrupt.
1	IE0	P3.2	**EXTERNAL0 interrupt flag**. Set by hardware when external Interrupt detected. Cleared by hardware.
2	IT1	P3.3	**EXTERNAL1 interrupt type control bit**. Set/cleared by software to specify falling edge/low level triggered external interrupt.
3	IE1	P3.3	**EXTERNAL1 interrupt flag**. Set by hardware when external Interrupt detected. Cleared by hardware.
4	TR0	TIMER 0	**Timer 0 run control bit**. Set/cleared by software to turn timer on/off.
5	TF0	TIMER 0	**Timer 0 overflow flag**. Set by hardware on timer/counter overflow. Cleared by hardware or software.
6	TR1	TIMER 1	**Timer 1 run control bit**. Set/cleared by software to turn timer on/off.
7	TF1	TIMER 1	**Timer 1 overflow flag**. Set by hardware on timer/counter overflow. Cleared by hardware or software.
IRQ1 address C0H: interrupt request register for X2 to X9			
0	IQ2	P1.0	Interrupt request flag from P1.0.
1	IQ3	P1.1	Interrupt request flag from P1.1.

BITS	CONV. NAME	SOURCE	NOTES
2	IQ4	P1.2	Interrupt request flag from P1.2.
3	IQ5	SYMBOL	Interrupt request flag from clock recovery circuit. Set by hardware or software. Cleared by software.
4	IQ6	P1.4	Interrupt request flag from P1.4.
5	IQ7	DC/DC	Interrupt request flag from DC/DC CONVERTER. Set by hardware or software. Cleared by software.
6	IQ8	WDI	Interrupt request flag from watchdog timer. Set by hardware or software. Cleared by software.
7	IQ9	MIN	Interrupt request flag from real-time clock interrupt. Set by hardware or software. Cleared by software.
WUCON address 94H: wake-up counter control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Parallel load signal for wake-up counter.
2	Z0	–	
3	Z1	–	
4	CPL	–	Complete interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
5	unused	–	
6	WUP	–	WUP interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
7	RUN	–	RUN bit for wake-up counter.
RTCON address CDH: real-time clock control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Load RTC0 value from SFR to RTC.
2	W/$\overline{R}$	–	Disable write back to SFR.
3 to 6	unused	–	
7	MIN	–	Interrupt request flag from RTC. Set by hardware or software. Cleared by software.

Notes

1. IEN0 and IEN1: These are two 8-bit registers that control the enabling of the 15 interrupt sources individually as well as a global enable/disable for all of the sources.
2. IP0 and IP1: These are two 8-bit registers that set priority for each interrupt source. IP0 actually contains only 7 bits as IP.7 is not implemented. This bit will always read as logic 0.

6.19.4 Port 3 interrupts: P3.2 and P3.3

INT0 and INT1 are level or edge sensitive.
The programming is performed with TCON. Since P3.2 and P3.3 are configured as push-pull outputs, these interrupts can only be triggered by output commands to these ports and not by external events.

TCON.0 (IT0): Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt (see Fig.23).

TCON.1 (IE0): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

TCON.2 (IT1): Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

TCON.3 (IE1): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

6.19.5 Wake-up interrupt

The wake-up interrupt (T2) is the level sensitive OR function of the WUP bit or CPL bit in the WUCON SFR. The wake-up interrupt is mapped to the T2 vector (see Fig.24). These flags are set by hardware and need to be cleared by software. For more information see Section 6.14.

WUCON.6 (WUP): WUP interrupt flag. Attention: writing and reading this SFR bit does not access the same flag. The flag is set by hardware and needs to be cleared by software.

WUCON.4 (CPL): Complete flag. The previous set instruction is completed. The settings of the SFR have been copied to the peripheral block. The flag is set by hardware and needs to be cleared by software.

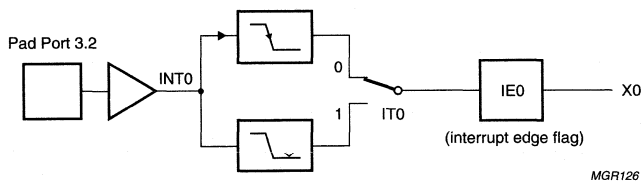


Fig.23 External interrupt Port 3.2 and Port 3.3 (INT0 and INT1).

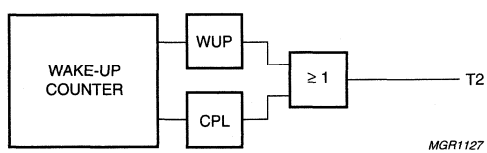


Fig.24 Wake-up interrupt.

6.19.6 PORT 1 INTERRUPTS: PORT 1.0 TO PORT 1.4 (INT2 TO INT6)

Four Port 1 lines can be used as external interrupt inputs (see Fig.25). When enabled (IEN1 SFR), each of these lines can wake-up the device from power-down. Using the IX1 register, each of these port lines may be set active to either HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will send an interrupt request, but must be cleared by software, i.e. via the interrupt software. The Port 1 interrupt request flags can only be set if the corresponding interrupt enable bit is set.

6.19.7 MORE INTERRUPTS: SYMCLK, DC/DC CONVERTER, WATCHDOG AND MINUTE

The decoder blocks generate events that can force an interrupt when enabled (IEN0 and IEN1 SFR). These interrupts are mapped to the corresponding P1 interrupt request flag register bits (see Fig.26). Each flag, if the interrupt is enabled, will send an interrupt request and must be cleared by software, i.e. via the interrupt service routine.

The IRQ bits are not set if the corresponding enable is not set.

IRQ1.3: (symbol interrupt); this interrupt request flag, if enabled, is set if the demodulator (clock recovery) has data ready, that should be read by the microcontroller. The event is called symbol clock or SymClk, because in one mode of operation one symbol is delivered per interrupt. The flag is set by hardware and needs to be cleared by software.

IRQ1.5: (DC/DC converter interrupt); this interrupt request flag, if enabled, is set if the DC/DC converter is not able to deliver the required current (STB flag cleared). The flag is set by hardware and needs to be cleared by software.

IRQ1.6: (watchdog interrupt); this interrupt request flag, if enabled, is set if the watchdog timer will expire within $^1/_{16}$ s. The flag is set by hardware and needs to be cleared by software.

IRQ1.7: (minute interrupt); this interrupt request flag, if enabled, is set once each minute by the real-time clock. The flag is set by hardware and needs to be cleared by software.

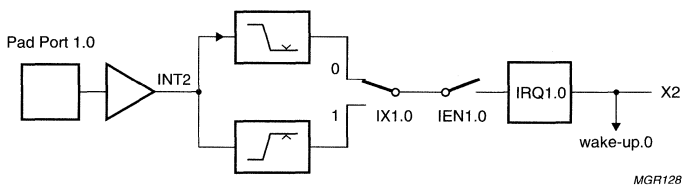


Fig.25 Interrupt Port 1.0.

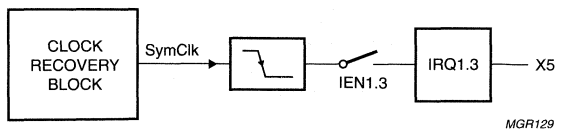


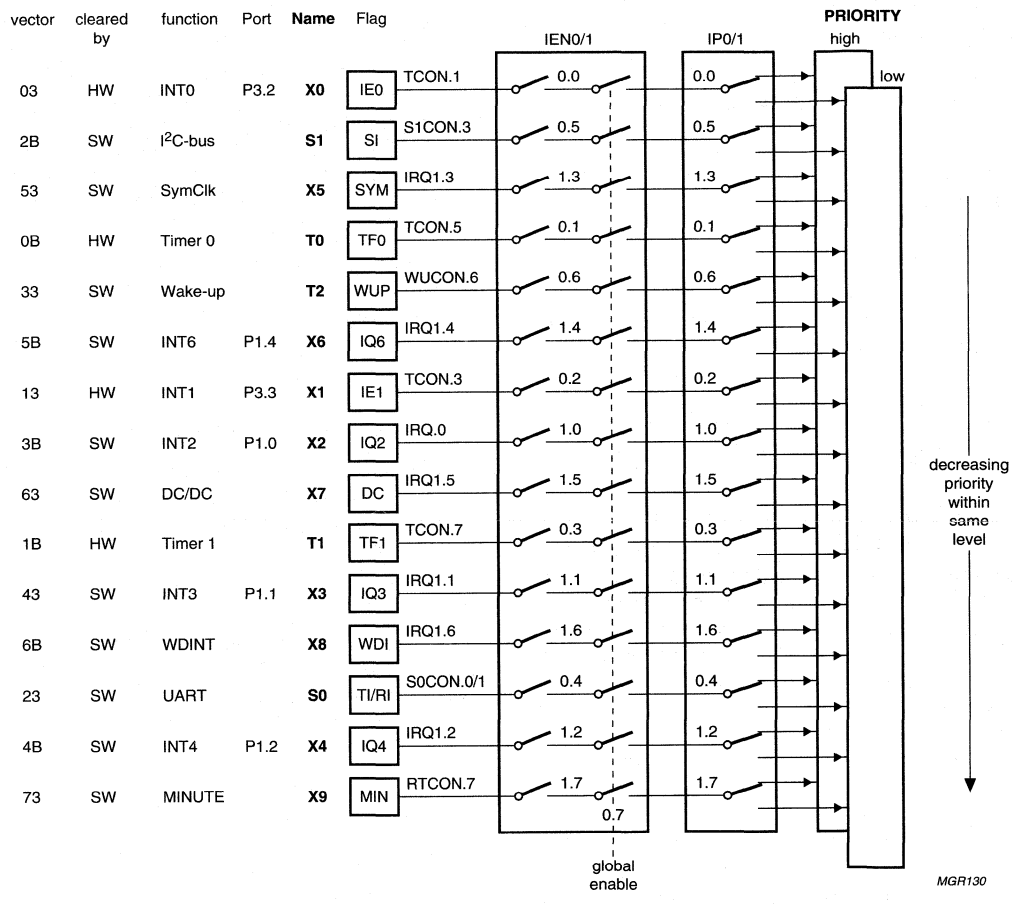
Fig.26 SymClk (as an example for any of the 4 mentioned interrupts).

6.19.8 INTERRUPT HANDLING

Figure 27 shows the conventions for interrupt assignments and priorities.

Arbitration of several simultaneous interrupts can be seen from Fig.27. The sampled interrupt with the highest priority will be handled first (assuming that the interrupt priority is default).

Setting of interrupt request flags for X2 to X9 is masked by the corresponding interrupt enable bit (IEN1).



The signal level applied to the $\overline{EAN}$ pin defines whether the interrupt vector code is fetched from external or internal ROM.

Fig.27 Interrupt assignment and priorities.

6.20 Idle and power-down operation

Idle and power-down are power saving modes of the microcontroller that can be activated when no CPU activity is required. Both modes do not stop the 76.8 kHz oscillator nor disable any peripheral function.

The following functions remain active during the Idle mode.

- Timer 0 and Timer 1
- Wake-up counter
- Watchdog counter
- Real-time clock
- Demodulator and clock recovery
- UART
- I²C-bus
- External interrupt.

6.20.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 51.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device into the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are:
   a) Watchdog reset if the watchdog had expired
   b) Off/on reset if the DC/DC converter is restarted from the off mode (wake-up counter, RTC or P1 pins).

6.20.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last instruction executed in the normal operating mode before the power-down mode is activated. Once in the power-down mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during power-down mode. The status of the external pins during power-down mode is shown in Table 51.

There are two ways to terminate the power-down mode:

1. Activation of an enabled external interrupt (INT2 to INT9) will cause PCON.1 to be cleared by hardware thus terminating the power-down mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the power-down mode.
2. The second way of terminating the power-down mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are
   a) Watchdog reset if the watchdog had expired
   b) OFF-ON reset if the DC/DC converter is restarted from the off mode (wake-up counter or P1 pins).

The power-down mode is not especially useful. It has been implemented for compatibility only. The Idle mode has the same power saving capability and allows much more flexible wake-up.

6.20.3 OFF MODE

The off mode has been designed as the power saving mode of the PCA5007. Shortly after entering this mode the DC/DC converter is switched off and V_{DD} is reduced to V_{BAT}. Directly after activating the off mode, the CPU must be set in Idle mode.

The off mode is entered by:

1. ORL DCCON0, #80H
2. ORL PCON, #01H.

The off mode can be exited by one of the following events:

- RTC minute event
- Wake-up counter event
- Event on any P1 pin
- RESETIN active HIGH.

Each of these events first starts the DC/DC converter to ramp up V_{DD} to 2.2 V. After an initial reset, generated by the DC/DC converter when V_{DD} is again at normal level, all 2 V blocks will restart their operation. The first instruction will be fetched from address 0.

The edge sensitive interrupts (minute and wake-up) from the internal sources will have been lost during restart and must be polled from their SFRs. Events from P1 pins can be served after enabling the interrupts, since they are level sensitive.

6.20.4 Status of external pins

The status of the external pins during Idle and power-down mode is shown in Table 51.

Table 51 Status of external pins during normal, Idle and power-down modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Normal	internal	0	1	port data	port data	port data	port data
Idle	internal	1	1	port data	port data	port data	port data
	external	1	1	pull-up HIGH	port data	address	port data
Power-down	internal	0	0	pull-up HIGH	port data	port data	port data
	external	0	0	pull-up HIGH	port data	address	port data

6.20.5 Power Control Register (PCON)

The reduced power modes are activated by software using this special function register. PCON is not bit addressable.

Table 52 Power Control Register (PCON and SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL

Table 53 Power Control Register (PCON, SFR address 87H)

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Control bit to double data rate of UART, when set to logic 1.
PCON.6	XRE	If set to logic 1 enables external XRAM from address 0 on, if set to logic 0 the first 768 XRAM bytes are in internal XRAM, the higher addresses come from external XRAM; see note 2.
PCON.5	ENIS	**Enable ISYNC**. If bit is set, ISYNC can be monitored at pin $\overline{EA}$ in internal access mode. The binary value of ISYNC changes each time a new instruction is fetched from memory. This bit must not be set to logic 1 by user program!
PCON.4	–	reserved
PCON.3	GF1	**General purpose flag bit.**
PCON.2	GF0	**General purpose flag bit**.
PCON.1	PD	**Power-down bit**. Setting this bit activates the power-down mode; see note 1.
PCON.0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode; see note 1.

Notes

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (00000000).
2. This device does not support external XRAM access. Therefore the XRE bit is meaningless and should never be written to logic 1.

6.21 Reset

To initialize the PCA5007 a reset is performed by using either of the 2 following methods:

- Applying an external reset signal to the RESETIN pin
- Via the on-chip watchdog timer.

The reset state of the output pins is given in separate tables (Tables 2 to 6). The reset state of the SFRs is given in a separate overview (see Table 1).

While a reset is applied to the device the output $\overline{\text{RESOUT}}$ is driven LOW.

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

6.21.1 External reset using the RESETIN pin

The external reset input for the PCA5007 is the RESETIN pin. A Schmitt trigger is used at the input for noise rejection. Immediately after pin RESETIN goes HIGH, an internal reset is executed. As a consequence the SFRs and port pins adopt their reset state, ALE and $\overline{\text{PSEN}}$ are held HIGH. As long as the RESETIN pin stays HIGH, the reset state is maintained. When RESETIN goes LOW, the device start-up sequence is executed (see Section 6.22).

6.21.2 External power-on reset using the RESETIN pin

An automatic reset can be obtained by connecting the RESETIN pin to V_{BAT} via a capacitor and to V_{SS} via a resistor. At power-on, the voltage on the RESETIN pin is equal to V_{BAT} and decreases from V_{BAT} as the capacitor charges through the resistor to V_{SS}. $V_{RESETIN}$ must remain higher than the threshold of the Schmitt trigger for a duration of $t_{RESETIN}$ (see Chapter "AC characteristics"). The reset configuration is shown in Fig.28.

6.21.3 Internal reset

The watchdog which is available in the PCA5007 (see Section 6.16) will force a reset if it is enabled and expires.

A reset is also forced, when the DC/DC converter restarts operation from the off mode (see Section 6.22.3).

All resets to the microcontroller can be observed as negative pulses at the output $\overline{\text{RESOUT}}$.

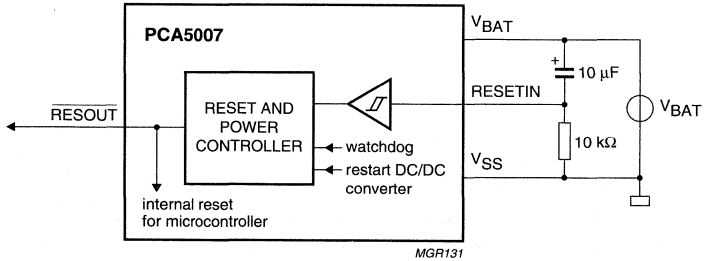


Fig.28 Application diagram for external power-on reset configuration.

6.22 DC/DC converter

6.22.1 FUNCTION

The DC/DC converter converts the voltage from a single primary cell (0.9 to 1.6 V) to a nominal 2.2 V supply voltage for on-chip and off-chip use. For EMC reasons a special technique is used to minimize coil current ripples under all load conditions.

The voltage generated by the DC/DC converter is available at pin $V_{DD(DC)}$. The supply for all functions of the chip is taken from the V_{DD} and V_{DDA} pins. The user has to connect $V_{DD(DC)}$ to the other V_{DD} pins. The supply used for the reference and comparators is taken from V_{DDA}.
A typical circuit configuration is shown in Fig.29.

For a certain current load (I_L) the controller settles to a stable voltage V_{DD} (I_L) between 2.15 to 2.25 V. Increasing the load decreases V_{DD} (I_L) by a small amount. When V_{DD} (I_L) drops below 2.15 V the DC/DC converter calculates a new set of coefficients and V_{DD} (I_L) settles again between 2.15 and 2.25 V (see Fig.38).

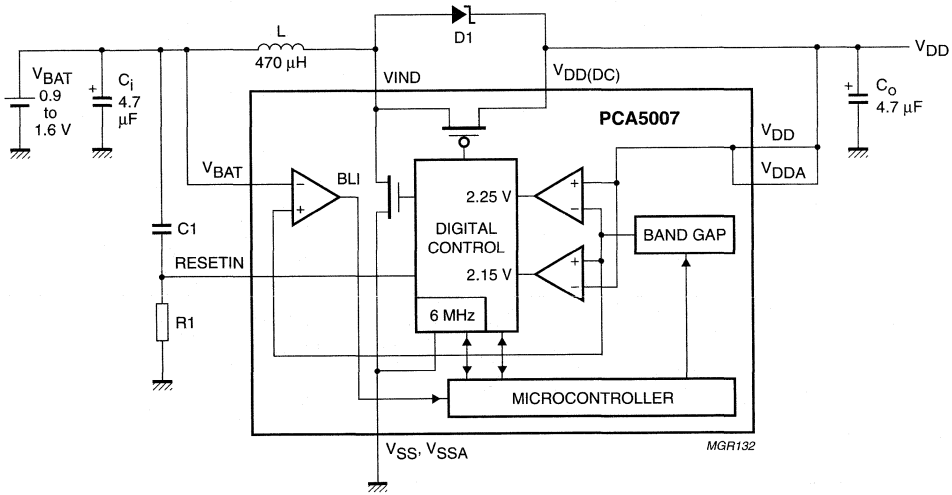


Fig.29 Typical operating circuit.

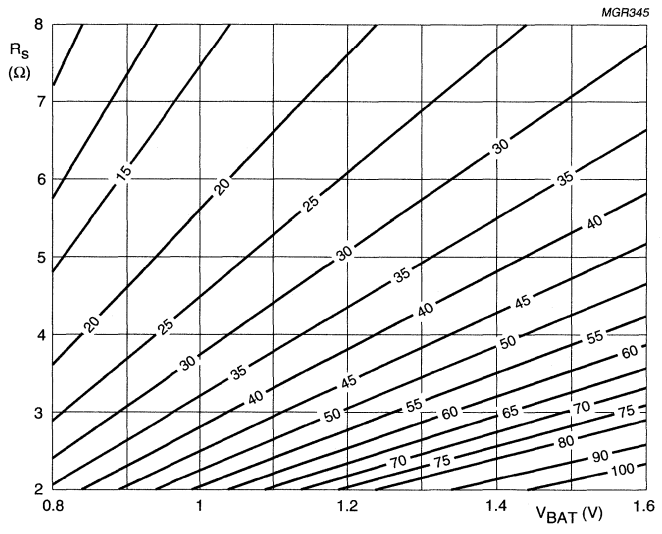
6.22.2 TYPICAL OPERATING CHARACTERISTICS

The maximum power delivered by the DC/DC converter is given by equation (1).

$$P_{o(max)} \leq \frac{(V_{Bat})^2}{4 \times R_s} \quad (1)$$

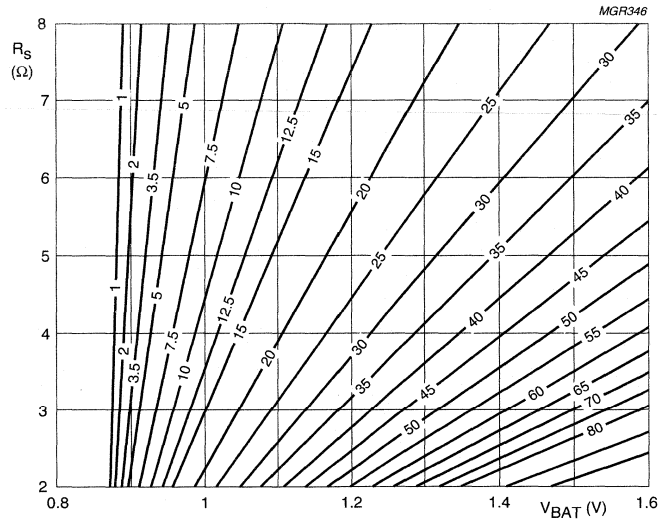
R_S is the total series resistance which is the sum of $R_{BAT} + R_{ind} + R_{sw} + ESR(C_o)$. In Figs 30 and 31 the maximum available output current (I_L) is shown as a function of V_{BAT} and R_S.

The efficiency is determined by the series resistance R_S and the current consumption of the converter itself. R_S is the sum of the battery resistance R_{BAT}, the DC resistance SRL of the coil, the on resistance of the MOSFET $R_{DS,on}$ and the ESR of the output capacitor C_o. Figure 32a shows the efficiency when using a 470 µH coil with a SRL of 5 Ω and a load capacitor of 4.7 µF with an ESR of 0.5 Ω. In Fig.32b the efficiency for the same configuration is shown but with a SRL of only 0.1 Ω. To increase efficiency for extremely low output currents, the converter should be set into standby mode (see Fig.33).



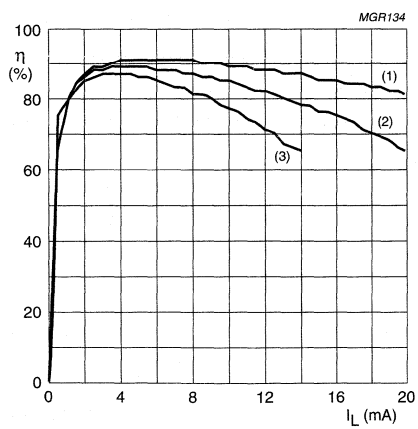
V_{DD} = 2.2 V; $R_S = R_{BAT} + R_{ind} + R_{sw}$

Fig.30 Maximum available output current (mA) in normal mode.

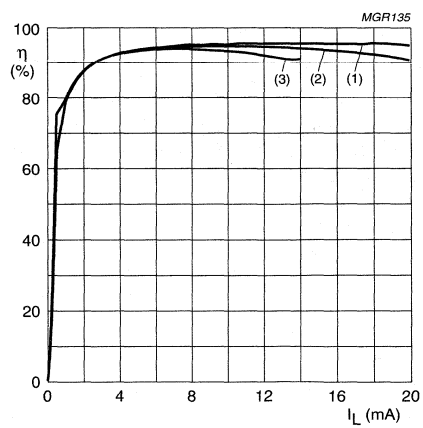


V_{DD} = 2.2 V; $R_s = R_{BAT} + R_{ind} + R_{sw}$

Fig.31 Maximum available output current (mA) in standby mode.



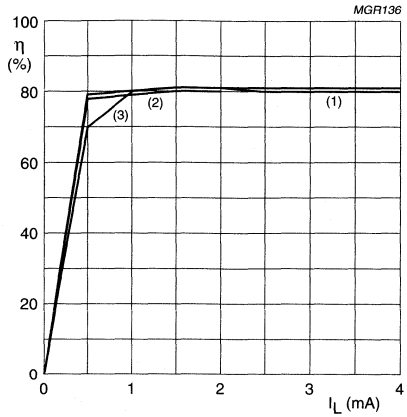
a. R_S = 6 Ω.



b. R_S = 1 Ω.

(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.32 Efficiency in normal mode as a function of load current.



(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.33 Efficiency in standby mode as a function of load current.

6.22.3 START-UP DESCRIPTION

6.22.3.1 Start-up from reset

An external RC network together with an on-chip Schmitt trigger is used to generate a reset pulse after the insertion of a new battery (see Section 6.21). A reset pulse at the RESETIN pin resets the SFRs and the internal registers of the DC/DC converter to the factory programmed values and the start-up sequence shown in Fig.34 is started. The reset pulse must be essentially longer then the rise time of V_{BAT}.

The start-up sequence is divided into several steps:

1. Start-up 76.8 kHz crystal oscillator (256 clocks).
2. Boost up of V_{DD} to approximately 1.7 V using the 76.8 kHz clock. During this phase, the p-channel MOSFET is switched off and the charge is transferred via the external Schottky diode.
3. Start of the 6 MHz clock $\left(2 \times \frac{1}{76.8\ \text{kHz}}\right)$; (see Section 6.12).
4. Boost up V_{DD} to 2.2 V using the internal 6 MHz clock and the p-channel MOSFET. As soon as $V_{DD} \geq 2.15$ V, the stable flag is set to indicate that the system is powered-up successfully and the microcontroller starts operating. The DC/DC converter now stays in the normal mode of the normal operating mode.

If a reset pulse is generated during normal operation, the DC/DC converter immediately resets the whole system and enters the start-up sequence.

6.22.3.2 Start-up from off mode

Start-up from off mode behaves exactly as start-up from external reset (see Fig.34) except that:

- The internal registers of the DC/DC converter are not reset; however the DC/DC converter SFRs are reset.

off mode is exited when one of the following events occur:

- Key pressed
- Minute interrupt
- Wake-up interrupt.

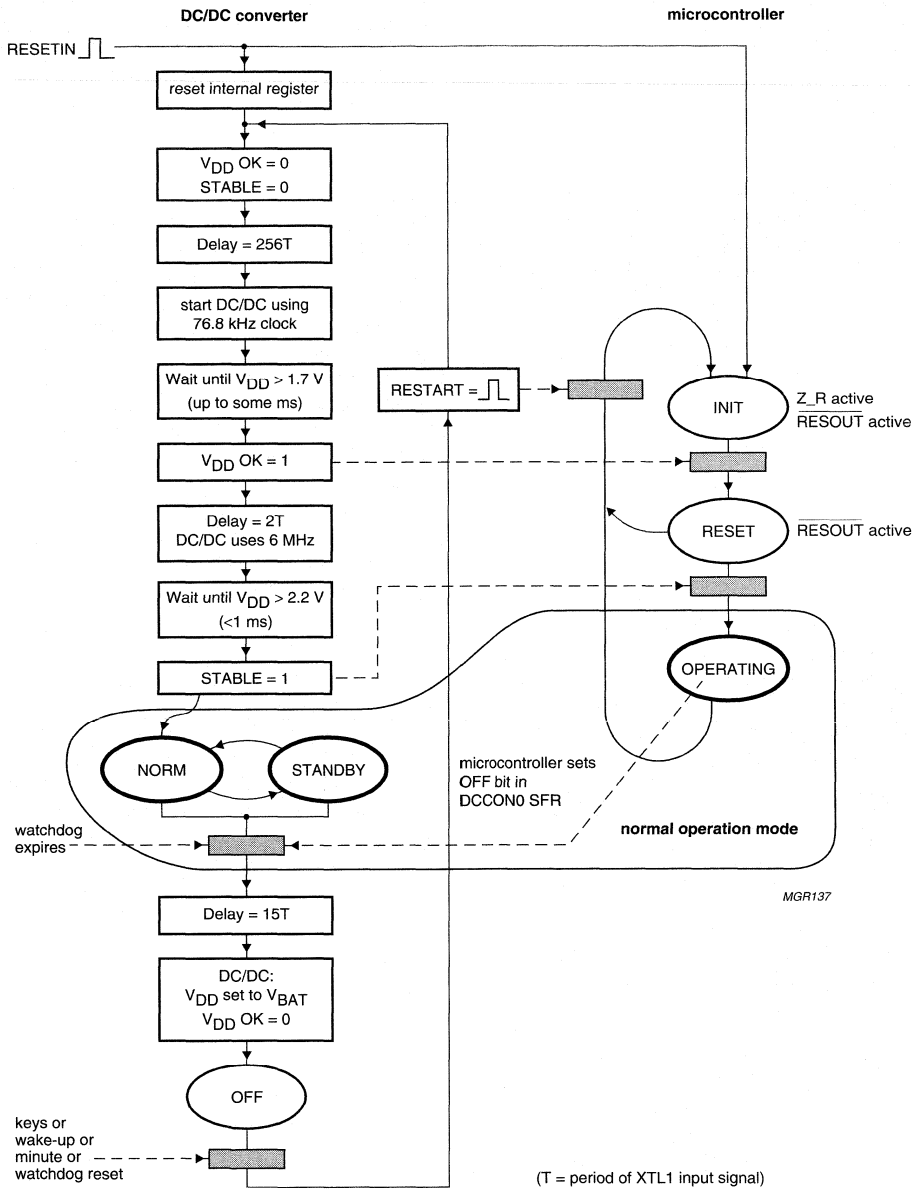


Fig.34 System power-up/off sequencing.

6.22.4 DESCRIPTION OF OPERATING MODES

6.22.4.1 Normal operating mode

Once the system is powered-up successfully (STB = 1), the DC/DC converter is in normal operating mode. This mode has two sub modes:

- Normal mode
- Standby mode.

By setting/resetting the standby bit in DCCON0 (D1H), the DC/DC converter switches between the normal mode and the standby mode. Switching between these two modes is possible at any time by software if the controller is in the normal operating mode. Normal operating mode can be exited by any of the following events:

- HIGH level at the RESETIN pin
- A watchdog reset, which will force the same sequence as an off command
- Writing the off bit in DCCON0.

Setting the off bit in DCCON0 forces the converter into DC/DC converter off mode.

6.22.4.2 Normal mode

Normal mode is the high efficiency mode of the DC/DC converter. In this mode the controller can keep V_{DD} stable at 2.2 V up to the maximum available current (see Fig.30). The output voltage is regulated in a small window and the current peaks in the coil are kept as small as possible (see Fig.36). After a reset and the following start-up sequence, the controller is in normal mode.

To shorten the settling time when the receiver is switched on or off, the DC/DC converter uses 2 sets of coefficients. One for low output current and one for high output current. When the RXE bit in DCCON0 is set, the DC/DC converter stores the actual coefficients for low output current and switches to the coefficients for high load current. At the same time, the receiver should be enabled. If the battery voltage did not change very much since the last time the receiver was on, the settling time is only a few microseconds instead of a few hundreds of microseconds when not using the RXE bit. When switching off the receiver, the RXE bit in DCCON0 should be reset. In this case, the DC/DC converter stores the new values for high output current and restores the values for low output current. It should be noted that the RXE bit does not change the algorithm of the DC/DC converter but shortens the settling time dramatically.

When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. STB = 0 flags the inability to deliver enough current in normal mode or in standby mode. When the STB flag is set to logic 0, V_{DD} can drop very quickly, depending on the battery voltage and the load.

6.22.4.3 Standby mode

Standby mode is a low current mode which can be used when only the microcontroller is running and the quality of V_{DD} is not important. In standby mode the DC/DC converter uses the 76.8 kHz clock instead of the 6 MHz clock. This reduces the current consumption of the DC/DC converter. The maximum output current in this mode is limited to a few milliamperes (see Fig.31). In standby mode V_{DD} can be set to 1.9, 2.0, 2.1 or 2.2 V by setting the VLO1 and VLO0 bits in DCCON1 to the corresponding values. When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. In this case, the microcontroller should switch-off the different loads and switch to normal mode.

6.22.4.4 Off mode

The off mode can only be entered by setting the off bit in DCCON0 by software. The DC/DC converter waits for 15 periods of the 76.8 kHz clock before it sets V_{DD} to V_{BAT} and switches off completely (see Fig.34). In the off mode the PMOS is conducting and therefore it is guaranteed that V_{DD} never drops below V_{BAT} – 100 mV. When the DC/DC converter is in the off mode, one of the following events can restart the converter:

- P1X (independent from interrupt enabling or polarity)
- Minute
- Wake-up
- RESETIN pulse.

6.22.5 VOLTAGE/CURRENT RIPPLE

The ripples are determined by V_{BAT}, inductance L, C_o, ESR (Equivalent Series Resistance of C_o, switching frequency and the load current I_L. The ripples are illustrated in Fig.36. If ESR = 0 Ω, then $V_{ripple} = \Delta V$.

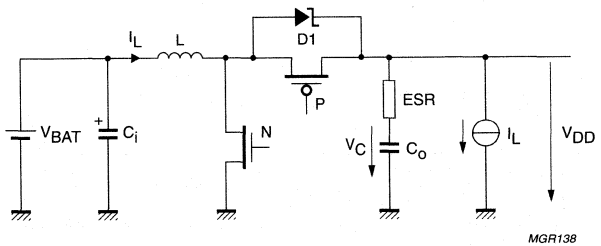
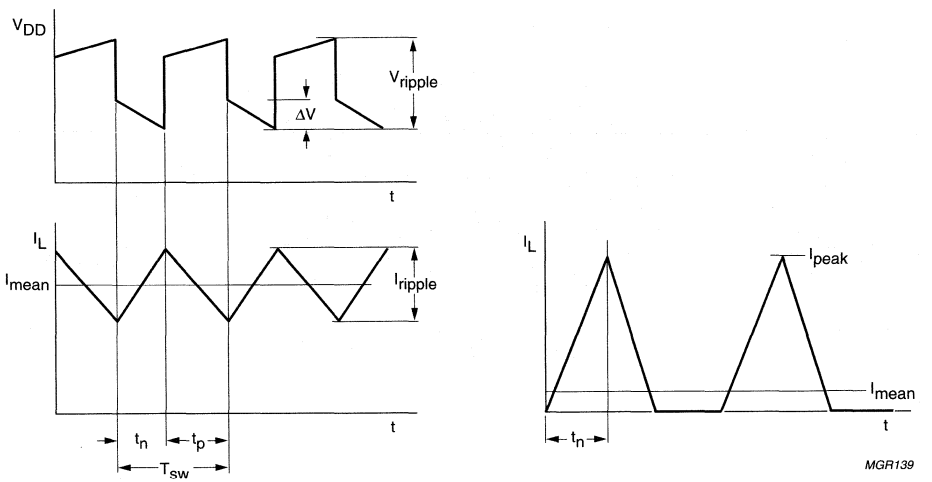


Fig.35 Circuit to analyse ripples.



a. Normal mode.

b. Standby mode.

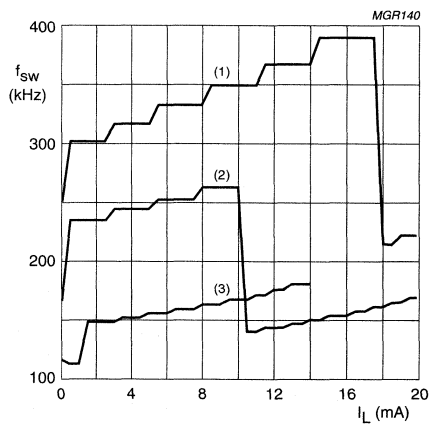
Fig.36 Zoom-in on the voltage and current ripples.

Table 54 Ripples in normal operating mode

MODE			
STANDBY		**NORM**	
$I_{peak} = V_{BAT} \times \frac{t_n}{L}$	t_n = 6.51 µs	$I_{ripple} = V_{BAT} \times \frac{t_n}{L}$	t_n = 1 µs, 2 µs, 4 µs
		$I_{L(mean)} = \frac{I_L}{D_p}$	$0.2 \leq D_p \leq 0.73$
$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 6.51 µs	$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 1 µs, 2 µs, 4 µs
$V_{ripple} = \frac{V_{BAT} \times t_n}{L} \times ESR$	t_n = 6.51 µs	$V_{ripple} = \left(I_{mean} + \frac{1}{2} \times \frac{V_{BAT} \times t_n}{L}\right) \times ESR$	t_n = 1 µs, 2 µs, 4 µs

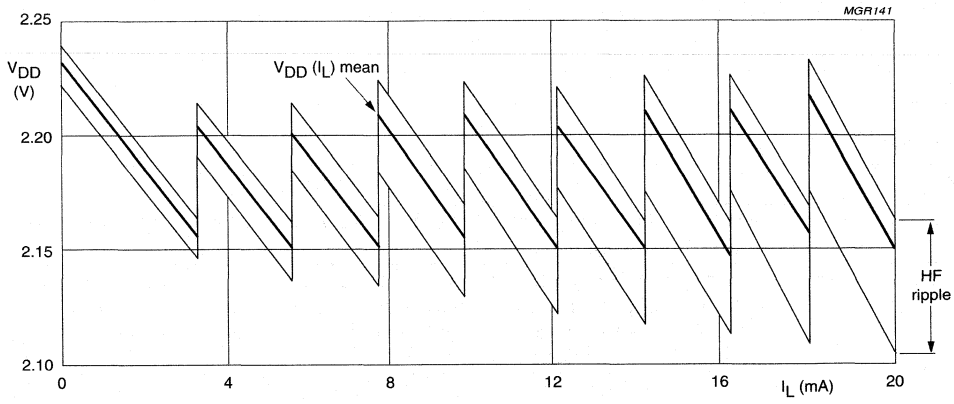
6.22.6 SWITCHING FREQUENCIES

Depending on the load and more importantly on the battery voltage the controller uses different on and off times for the NMOS and PMOS transistors. This results in different switching frequencies. If the 6 MHz ring oscillator is trimmed to 6 MHz (see Section 6.12) the switching frequency is 120 kHz ≤ f_{sw} ≤ 400 kHz. A typical frequency behaviour is shown in Fig.37.



L = 470 µH; SRL = 5 Ω; C_o = 4.7 µF; ESR = 0.5 Ω.
(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 1.0 V.

Fig.37 Switching frequencies.



V_{BAT} = 1.2 V; L = 470 µH; SRL = 5 Ω; C_o = 4.7 µF; ESR = 0.5 Ω.

Fig.38 V_{DD} as a function of load current.

6.22.7 V_{DD} ADJUSTMENT

V_{DD} can be shifted in four steps by adjusting the band gap voltage. The band gap voltage is set with the two bits VBG1 and VBG0 in DCCON1, see Table 55.

Table 55 V_{DD} adjustment

VBG1	VBG0	OUTPUT VOLTAGE
0	0	V_{DD}
0	1	V_{DD} – 50 mV
1	0	V_{DD} + 50 mV
1	1	V_{DD} + 100 mV

6.22.8 BATTERY LOW MEASUREMENT

Battery low measurement is enabled by setting the SBLI bit in DCCON0. 0.5 ms after setting SBLI to logic 1 the BLI bit in DCCON0 will contain the measurement result. When BLI = 0 the battery voltage is below 1.1 V. When BLI = 1 V_{BAT} is above 1.1 V. When SBLI = 1 V_{BAT} is measured continuously. Setting SBLI to logic 0 disables the V_{BAT} comparator and BLI is set to logic 1. After a reset pulse at RESETIN, SBLI is reset to logic 0.

6.22.9 DC/DC Control Register (DCCON0)

The DCCON0 special function register is used to control the operation of the on-chip DC/DC converter.

Table 56 DC/DC Control Register (DCCON0, SFR address D1H)

7	6	5	4	3	2	1	0
OFF	SBY	RXE	SBLI	–	–	STB	BLI

Table 57 Description of the DCCON0 bits

BIT	SYMBOL	FUNCTION
DCCON0.7	OFF	Writing this SFR bit to logic 1 puts the DC/DC converter in the off mode (independent of other control bits).
DCCON0.6	SBY	Writing this SFR bit to logic 1 puts the DC/DC converter in standby mode, where the DC/DC converter is clocked from the 76.8 kHz oscillator and the ripple voltage will be higher. If the DC/DC converter is unable to deliver enough current in SBY mode, the software has to reset the SBY mode.
DCCON0.5	RXE	Writing this SFR bit to logic 1 uses the stored set of coefficients from a local register to force the DC/DC converter into the state which is appropriate for the required current. The contents of this local register are maintained when the DC/DC converter is set into off state. For the first time after connecting V_{BAT} a set of default coefficients is used. Writing this bit to logic 0 copies the actual coefficients used momentary by the DC/DC converter back to the local register.
DCCON0.4	SBLI	Writing this SFR bit to logic 1 enables the circuitry for measurement of the battery voltage. The new BLI value is valid 0.5 ms later. In order to make a new measurement, the receiver should draw current (continuous mode of DC/DC converter). If SBLI is logic 0 (BLI measurement disabled) BLI will go to HIGH.
DCCON0.3	–	unused
DCCON0.2	–	unused
DCCON0.1	STB	**Set by the DC/DC converter after power-up**. Reset by the DC/DC converter if the converter is not able to deliver the required power. The signal is set in SBY and non SBY mode. This bit is read only.
DCCON0.0	BLI	**Battery low indicator**. Set by the DC/DC converter if V_{BAT} < 1100 mV ±50 mV. This bit is read only.

6.22.10 DC/DC Adjust Control Register (DCCON1)

The DCCON1 special function register is used to adjust the exact voltage levels of the on-chip DC/DC converter.

Table 58 DC/DC Adjust Control Register (DCCON1, SFR address D2H)

7	6	5	4	3	2	1	0
VBG1	VBG0	VLO1	VLO0	–	–	–	–

Table 59 Description of the DCCON1 bits

BIT	SYMBOL	FUNCTION
DCCON1.7	VBG1	**Adjustment for band gap voltage**; used to trim the band gap voltage [00] = 1.260 V, [01] = 1.233 V, [10] = 1.286 V, [11] = 1.312 V.
DCCON1.6	VBG0	
DCCON1.5	VLO1	**Adjustment for DC/DC converter output voltage in standby mode;** [00] = 1.9 V, [01] = 2.0 V, [10] = 2.1 V, [11] = 2.2 V.
DCCON1.4	VLO0	
DCCON1.3	–	unused
DCCON1.2	–	unused
DCCON1.1	–	unused
DCCON1.0	–	unused

7 INSTRUCTION SET

The PBB family uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes power consumption in Idle and active modes as well as byte efficiency and execution speed. Typical execution times and energy consumption at a V_{DD} of 2.2 V are given in Table 60. **Attention**: for most opcodes the numbers for execution speed and energy are also strongly dependant on the data (ADD, SUBB, DEC, INC, MUL, DIV, DA, conditional jumps etc.) and the operand address (CPU internal SFRs or SFRs in a peripheral block).

Table 60 Instruction set

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME (μs)	ENERGY [NJ]	OPCODE (HEX)
Arithmetic operations						
ADD	A,Rn	add register to A	1	0.498	1.831	2*
ADD	A,direct	add direct byte to A	2	0.631	2.501	25
ADD	A,@Ri	add indirect RAM to A	1	0.529	1.990	26, 27
ADD	A,#data	add immediate data to A	2	0.583	2.262	24
ADDC	A,Rn	add register to A with carry flag	1	0.508	1.864	3*
ADDC	A,direct	add direct byte to A with carry flag	2	0.637	2.525	35
ADDC	A,@Ri	add indirect RAM to A with carry flag	1	0.539	2.030	36, 37
ADDC	A,#data	add immediate data to A with carry flag	2	0.597	2.304	34
SUBB	A,Rn	subtract register from A with borrow	1	0.497	1.861	9*
SUBB	A,direct	subtract direct byte from A with borrow	2	0.630	2.527	95
SUBB	A,@Ri	subtract indirect RAM from A with borrow	1	0.528	2.021	96, 97

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME (μs)	ENERGY [NJ]	OPCODE (HEX)
SUBB	A,#data	subtract immediate data from A with borrow	2	0.582	2.287	94
INC	A	increment A	1	0.459	2.475	04
INC	Rn	increment register	1	0.457	1.737	0*
INC	direct	increment direct byte	2	0.586	1.982	05
INC	@Ri	increment indirect RAM	1	0.493	1.982	06, 07
DEC	A	decrement A	1	0.459	1.489	14
DEC	Rn	decrement register	1	0.457	1.74	1*
DEC	direct	decrement direct byte	2	0.590	2.488	15
DEC	@Ri	decrement indirect RAM	1	0.489	1.972	16, 17
INC	DPTR	increment data pointer	1	0.384	1.345	A3
MUL	AB	multiply A & B	1	0.378	1.242	A4
DIV	AB	divide A by B	1	0.733	2.532	84
DA	A	decimal adjust A	1	0.426	1.363	D4
Logic operations						
ANL	A,Rn	AND register to A	1	0.495	1.857	5*
ANL[1]	A,direct	AND direct byte to A	2	0.623	2.494	55
ANL	A,@Ri	AND indirect RAM to A	1	0.525	2.021	56, 57
ANL	A,#data	AND immediate data to A	2	0.583	2.272	54
ANL	direct,A	AND A to direct byte	2	0.650	2.639	52
ANL	direct,#data	AND immediate data to direct byte	3	0.719	3.138	53
ORL	A,Rn	OR register to A	1	0.459	1.605	4*
ORL[1]	A,direct	OR direct byte to A	2	0.584	2.248	45
ORL	A,@Ri	OR indirect RAM to A	1	0.486	1.767	46, 47
ORL	A,#data	OR immediate data to A	2	0.539	2.015	44
ORL	direct,A	OR A to direct byte	2	0.614	2.405	42
ORL	direct,#data	OR immediate data to direct byte	3	0.679	2.886	43
XRL	A,Rn	exclusive-OR register to A	1	0.459	1.715	6*
XRL[1]	A,direct	exclusive-OR direct byte to A	2	0.584	2.361	65
XRL	A,@Ri	exclusive-OR indirect RAM to A	1	0.486	1.873	66, 67
XRL	A,#data	exclusive-OR immediate data to A	2	0.540	2.128	64
XRL	direct,A	exclusive-OR A to direct byte	2	0.614	2.550	62
XRL	direct,#data	exclusive-OR immediate data to direct byte	3	0.679	3.017	63
CLR	A	clear A	1	0.374	1.265	E4
CPL	A	complement A	1	0.398	1.511	F4
RL	A	rotate A left	1	0.383	1.388	23
RLC	A	rotate A left through the carry flag	1	0.383	1.390	33
RR	A	rotate A right	1	0.382	1.381	03

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME (μs)	ENERGY [NJ]	OPCODE (HEX)
RRC	A	rotate A right through the carry flag	1	0.383	1.382	13
SWAP	A	swap nibbles within A	1	0.371	1.394	C4
Data transfer						
MOV	A,Rn	move register to A	1	0.377	1.406	E*
MOV	A,direct	move direct byte to A	2	0.509	2.080	E5
MOV	A,@Ri	move indirect RAM to A	1	0.408	1.568	E6, E7
MOV	A,#data	move immediate data to A	2	0.426	1.752	74
MOV	Rn A	move A to register	1	0.344	1.347	F*
MOV	Rn,direct	move direct byte to register	2	0.602	2.654	A*
MOV	Rn,#data	move immediate data to register	2	0.415	1.839	7*
MOV	direct,A	move A to direct byte	2	0.477	2.024	F5
MOV	direct,Rn	move register to direct byte	2	0.536	2.294	8*
MOV	direct,direct	move direct byte to direct byte	3	0.661	2.950	85
MOV	direct,@Ri	move indirect RAM to direct byte	2	0.564	2.438	86, 87
MOV	direct,#data	move immediate data to direct byte	3	0.679	3.017	75
MOV	@RI,A	move A to indirect RAM	1	0.378	1.517	F6, F7
MOV	@Ri,direct	move direct byte to indirect RAM	2	0.633	2.629	A6, A7
MOV	@Ri,#data	move immediate data to indirect RAM	3	0.448	2.019	76, 77
MOV	DPTR,#data 16	load data pointer with a 16-bit constant	3	0.519	2.267	90
MOVC	A,@A+DPTR	move code byte relative to DPTR to A	1	0.775	3.570	93
MOVC	A,@A+PC	move code byte relative to PC to A	1	0.770	3.374	83
MOVX	A,@Ri	move external RAM (8-bit address) to A	1	0.707	2.732	E2, E3
MOVX	A,@DPTR	move external RAM (16-bit address) to A	1	0.710	2.605	E0
MOVX	@Ri,A	move A to external RAM (8-bit address)	1	0.629	2.595	F2, F3
MOVX	@DPTR,A	move A to external RAM (16-bit address)	1	0.631	2.439	F0
PUSH	direct	push direct byte onto stack	2	0.600	2.543	C0
POP	direct	pop direct byte from stack	2	0.606	2.548	D0
XCH	A,Rn	exchange register with A	1	0.513	1.847	C*
XCH	A,direct	exchange direct byte with A	2	0.645	2.526	C5
XCH	A,@Ri	exchange indirect RAM with A	1	0.544	2.024	C6, C7
XCHD	A,@Ri	exchange LOW-order nibble indirect RAM with A	1	0.486	1.904	D6, D7
Boolean variable manipulation						
CLR	C	clear carry flag	1	0.293	1.075	C3
CLR	bit	clear direct bit	2	0.597	2.509	C2
SETB	C	set carry flag	1	0.293	1.084	D3
SETB	bit	set direct bit	2	0.611	2.603	D2
CPL	C	complement carry flag	1	0.320	1.134	B3
CPL	bit	complement direct bit	2	0.583	2.471	B2

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME (µs)	ENERGY [NJ]	OPCODE (HEX)
ANL	C,bit	AND direct bit to carry flag	2	0.540	2.187	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	0.563	2.388	B0
ORL[2]	C,bit	OR direct bit to carry flag	2	0.561	2.341	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	0.561	2.341	A0
MOV	C,bit	move direct bit to carry flag	2	0.610	2.542	A2
MOV	bit,C	move carry flag to direct bit	2	0.610	2.542	92
Program and machine control						
ACALL	addr11	absolute subroutine call	2	0.840	3.384	•1 addr
LCALL	addr16	long subroutine call	3	1.082	4.562	12
RET		return from subroutine	1	1.082	4.562	22
RETI		return from interrupt	1	1.082	4.562	32
AJMP	addr11	absolute jump	2	0.670	2.524	♦1 addr
LJMP	addr16	long jump	3	0.840	3.384	02
SJMP	rel	short jump (relative address)	2	0.670	2.524	80
JMP	@A+DPTR	jump indirect relative to the DPTR	1	1.049	4.015	73
JZ	rel	jump if A is zero	2	0.639	2.224	60
JNZ	rel	jump if A is not zero	2	0.754	2.896	70
JC	rel	jump if carry flag is set	2	0.620	2.128	40
JNC	rel	jump if carry flag is not set	2	0.733	2.705	50
JB	bit,rel	jump if direct bit is set	3	0.788	3.095	20
JNB	bit,rel	jump if direct bit is not set	3	0.902	3.708	30
JBC	bit,rel	jump if direct bit is set and clear bit	3	0.894	3.520	10
CJNE	A,direct,rel	compare direct to A and jump if not equal	3	0.855	3.307	B5
CJNE	A,#data,rel	compare immediate to A and jump if not equal	3	0.794	3.024	B4
CJNE	Rn,#data,rel	compare immediate to register and jump if not equal	3	0.787	3.139	B*
CJNE	@Ri,#data,rel	compare immediate to indirect and jump if not equal	3	0.822	3.333	B6, B7
DJNZ	Rn,rel	decrement register and jump if not zero	2	0.857	3.474	D*
DJNZ	direct,rel	decrement direct and jump if not zero	3	0.991	4.178	D5
NOP		no operation	1	0.284	1.027	00

Notes

1. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct field addresses one of the I/O ports (P0 to P3) then the standard 80C51 uses the port pin input state for the operation while the PCA5007 uses the SFR contents.
2. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct bit field addresses one of the port bits, then the state of the corresponding port pin is written to the port SFR after execution of the instruction.

Table 61 Notation for data addressing modes

SYMBOL	DESCRIPTION
Rn	working registers R0 to R7
direct	128 internal RAM locations and any special function register (SFR)
@Ri	indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64-kbyte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2-kbyte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

Table 62 Hexadecimal opcode cross reference

SYMBOL	DESCRIPTION
*	8, 9, A, B, C, D, E and F.
•	11, 31, 51, 71, 91, B1, D1 and F1.
♦	01, 21, 41, 61, 81, A1, C1 and E1.

7.1 Instruction map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC@Ri					INC Rn				
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC@Ri					DEC Rn				
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri					ADD A,Rn				
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri					ADDC A,Rn				
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri					ORL A,Rn				
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri					ANL A,Rn				
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri					XRL A,Rn				
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data					MOV Rn,#data				
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri					MOV direct,Rn				
9	MOV DPTR,#data 16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri					SUBB A, Rn				
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,direct					MOV Rn,direct				
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel					CJNE Rn,#data,rel				
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri					XCH A,Rn				
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri					DJNZ Rn,rel				
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri		CLR A	MOV * A,direct	MOV A,@Ri					MOV A,Rn				
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A		CPL A	MOV direct,A	MOV @Ri,A					MOV Rn,A				

* MOV A, ACC is not a valid instruction.

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8 LIMITING VALUES

According to the Absolute Maximum Ratings System (IEC 134); note 1

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{BAT}	battery supply voltage	−0.5	+2.0	V
V_{DD}	supply voltage	−0.5	+5.0	V
V_I	input voltage (all inputs)	−0.3	V_{DD} + 0.3	V
$I_{I/O}$	maximum sink/source current for all input/output pins	−10	+10	mA
I_{BAT}, I_{IND}	maximum supply current for pins V_{BAT} and VIND	–	100	mA
I_{DD}	maximum supply current for any supply pin	–	50	mA
P_{tot}	total power dissipation	–	100	mW
$V_{ESD(HBM)}$	maximum ESD stress level applied to V_{PP} pin using human body model	–	2000	V
$V_{ESD(MM)}$	maximum ESD stress level applied to V_{PP} pin using machine model	–	200	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature (for all devices)	−10	+55	°C

Note

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise specified.

9 EXTERNAL COMPONENTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Discrete components					
L	inductor	330	470	1000	µH
C_o	output capacitor	–	4.7	10.0	µF
R_{FB}	feedback oscillator resistance	2.0	2.2	–	MΩ
R_{X1}	parasitic serial resistance of quartz	–	–	20	kΩ

10 DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.2 V; V_{BAT} = 1.2 V; T_{amb} = −10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified.; DC/DC converter configured as indicated in note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Battery supply						
V_{BAT}	battery operating voltage	note 2	0.9	1.2	1.6	V
$I_{BAT(reset)}$	static reset supply current	V_{BAT} = 1.2 V; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7; I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	5	µA
$I_{DD(reset)}$	static reset supply current	V_{DD} = V_{BAT}; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7, I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	10	µA
R_{NFET}	NFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V	–	1.1	5	Ω
R_{PFET}	PFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V	–	1.2	5	Ω
$I_{L(NFET)}$	NFET leakage current		–	–	1	µA
$I_{L(PFET)}$	PFET leakage current		−1	–	–	µA
$I_{NFET(max)}$	maximum allowed NFET current		–	–	50	mA
$I_{PFET(max)}$	maximum allowed PFET current		–	–	50	mA
DC/DC converter in off mode						
V_{DD}	DC supply voltage output		V_{BAT} − 0.1	–	V_{BAT}	V
$I_{BAT(off)}$	current consumed from V_{BAT} by the DC/DC converter itself	V_{DD} = V_{BAT}; all inputs at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	6	–	µA
DC/DC converter in standby mode						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5007 and external chips	note 3; programmable in 4 steps	1.8	1.9	2.3	V
		1.9: [VLO, VLO] = 00	–	1.9	–	V
		2.0: [VLO, VLO] = 01	–	2.0	–	V
		2.1: [VLO, VLO] = 10	–	2.1	–	V
		2.2: [VLO, VLO] = 11	–	2.2	–	V
V_{DROP}	DC voltage drop due to load	I_L = 500 µA; notes 3 and 4	–	–	100	mV
$V_{ripple(p-p)}$	ripple voltage (peak-to-peak value)	notes 4 and 5	–	50	–	mV
$I_{BAT(stb)}$	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 6 and 7	–	25	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(max)(stb)}$	maximum delivered continuous supply current	V_{BAT} = 0.9 V; R_S = 8 Ω; notes 7 and 9; see Fig.31	1	–	–	mA
$\eta_{(stb)}$	efficiency of DC/DC converter in standby mode	V_{BAT} = 1.2 V; I_{DD} = 100 μA; note 7	–	80	–	%
DC/DC converter in high current mode (non standby)						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5007 and external chips	note 3	2.2 – 6%	2.2	2.2 + 6%	V
$V_{DD(av)}$	mean DC voltage	notes 3 and 4	2.1	2.2	2.3	V
$V_{HFripple(p-p)}$	ripple voltage for frequencies above 20 kHz (peak-to-peak value)	notes 4 and 7	–	–	100	mV
$V_{LFripple(p-p)}$	low frequency ripple voltage caused by load variations (peak-to-peak value)	notes 4, 7 and 13	–	–	100	mV
I_{BAT}	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 7 and 8; see Fig.44	–	110	–	μA
$I_{DD(max)}$	maximum delivered continuous supply current	V_{BAT} = 0.9 V; R_S = 8 Ω; notes 7 and 9; see Fig.30	10	–	–	mA
$\eta_{(norm)}$	efficiency of DC/DC converter	note 7				
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 3 mA	–	90	–	%
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 10 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 3 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 10 mA	–	75	–	%
External supply current from V_{DD} = 2.2 V, V_{BAT} = 1.2 V						
V_{DD}	DC supply voltage (V_{DD} and V_{DDA} pins)	see Fig.57; note 10	2.2	2.2	2.5	V
I_{BAT}	operating current	T_{amb} = 25 °C; 76.8 kHz quartz	–	2	–	μA
$I_{DD(stb)}$	operating standby mode supply current from V_{DD}	T_{amb} = 25 °C; note 6	–	12	–	μA
$I_{DD(RX)}$	operating receive mode supply current from V_{DD}	T_{amb} = 25 °C; note 8	–	85	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply current from internal or external V_{DD} = 2.2 V						
$I_{DD(micro)}$	supply current due to operation of microcontroller	T_{amb} = 25 °C; note 11	–	0.7	–	mA/MIPS
$I_{DD(UART)}$	increase in I_{DD} due to operation of the UART	T_{amb} = 25 °C	–	5	–	µA
$I_{DD(IIC)}$	increase in I_{DD} due to operation of the I^2C-bus master	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(T0)}$	increase in I_{DD} due to operation of timer/counter 0	T_{amb} = 25 °C	–	0	–	µA
$I_{DD(T1)}$	increase in I_{DD} due to operation of timer/counter 1	T_{amb} = 25 °C	–	2	–	µA
$I_{DD(AFC)}$	supply current due to operation of AFC-DAC	T_{amb} = 25 °C	–	60	–	µA
$I_{DD(SBL)}$	supply current due to battery measurement active (SBLI = 1)	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(6MHz)}$	increase in I_{DD} due to activation of 6 MHz oscillator in standby mode	T_{amb} = 25 °C; frequency adjusted to 6 MHz	–	50	–	µA
OTP programming (OTP data retention can only be guaranteed if the devices are preprogrammed by Philips Semiconductors; data retention cannot be guaranteed for customer programmed samples)						
$V_{DD(prog)}$	supply voltage during programming	note 10	2.2	–	3.6	V
V_{PP}	program supply voltage		12.5	–	13	V
I_{PP}	program supply current	note 12	–	24	–	mA
$T_{amb(prog)}$	operating ambient temperature during programming		21	–	27	°C
Band gap (reference voltage for all comparators)						
V_{BG}	band gap voltage	[VBG1, VBG0] = 00	1.23	1.26	1.29	V
		[VBG1, VBG0] = 01	–	1.233	–	V
		[VBG1, VBG0] = 10	–	1.286	–	V
		[VBG1, VBG0] = 11	–	1.312	–	V
Initial V_{DD} OK detection						
$V_{DD(OK)}$	V_{DD} OK indication	T_{amb} = 25 °C	1.5	1.85	2.0	V
Battery low indicator						
V_{BLI}	battery low indication	[VBG1, VBG0] = 00	1.05	1.1	1.15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input; pins I(D1), Q(D0) and TCLK						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	+0.1	µA
Digital input; pin RESETIN						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{BAT}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{BAT}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	+0.1	µA
Digital input/output pin $\overline{EA}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
$I_{NMOS(h)}$	NMOS hold current	V_{DD} = 2.2 V; V_I = 0.6 V	–	–	200	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–200	–	–	µA
Digital output; pin $\overline{RESOUT}$						
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
Digital input/output; pin $\overline{PSEN}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
Digital input/output; pin ALE						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microcontroller input/output; ports P0, P1 and P2 pins (except P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = 0.5V_{DD}$	–200	–70	–20	µA
Microcontroller output port P3						
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.6 V	4	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–	–	–6	mA
Open-drain pins SDA and SCL (P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$	–1	–	+1	µA
$I_{sink(stat)}$	static output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	2.25	–	–	mA
$I_{sink(stat)(sc)}$	static output sink short-circuit current	V_{DD} = 2.2 V; $V_I = V_{DD}$	2.2	6	14	mA
AT output pin						
$I_{o(sink)}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	3	–	–	mA
$I_{o(source)}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–3	mA
76.8 kHz oscillator						
$V_{IL(XTAL1)}$	LOW-level input voltage at pin XTL1		–	–	0.3	V
$V_{IH(XTAL1)}$	HIGH-level input voltage at pin XTL1		1	–	–	V
$I_{LI(XTL1)}$	leakage current at pin XTL1	$V_I = V_{BAT}$ or V_{SS}	–1	–	+1	µA
I_{bias}	bias current from XTL2 to V_{SS}	V_{BAT} = 1.6 V; XTL1 at V_{SS}	0.5	0.8	1.1	µA
I_{op}	operating current consumption	V_{BAT} = 1.6 V; R_{fb} = 2.2 MΩ	–	2	–	µA
g_m	transconductance	I_o = ±0.3 µA	5	20	60	µA/V
V_{WP}	DC working point		–	550	–	mV
AFC-DAC						
V_{AFC}	resolution		–	$1/64V_{DD}$	–	V
ΔAFC	deviation for codes between 010000 and 100000 from straight line		–0.25LSB	–	+0.25LSB	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{L(DAC)}$	allowed resistive load at DAC output		10	–	–	kΩ
$C_{L(DAC)}$	allowed capacitive load at DAC output		–	–	50	pF
I_{source}	AFCOUT source current	V_{DD} = 2.2 V; $V_{AFCOUT} = V_{DD} - 0.4$ V; code = 111111	–	−895	−100	μA
I_{sink}	AFCOUT sink current	V_{DD} = 2.2 V; V_{AFCOUT} = 0.4 V; code = 000000	10	25	–	μA

Notes

1. DC/DC converter configured with inductor of L = 470 μH, SRL = 5 Ω, input capacitance of C_i = 4.7 μF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 μF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. The required V_{BAT} for starting the circuit after connecting it to the battery is 1.1 V. But once in place, the battery can be used until it is discharged to 0.9 V.
3. This parameter is not tested during production; it is covered by other measurements.
4. The accuracy of the voltage is defined by maximum offset and ripple voltage. DC offset is defined by the accuracy of the internal band gap reference and the offset of comparators, whereas the ripple voltage is defined by the limits of the allowed voltage window of the regulated V_{DD}.
5. The ripple in standby mode is defined by V_{BAT}, L, t_n and ESR (see Table 54).
6. PCA5007 set to standby mode by software: 76.8 kHz oscillator running, DC/DC converter running in standby mode, all timers/counters disabled except RTC, microcontroller Idle, all outputs open-circuit, no supply current delivered to external circuits.
7. This parameter depends on external components and is not tested during production; hence no guarantee.
8. PCA5007 set to receive mode by software: 76.8 kHz and 6 MHz oscillator running, DC/DC converter running in normal mode, wake-up counter, clock compensation, watchdog timer, T0 and T1 enabled, demodulator set to direct input data, AFC disabled, microcontroller Idle, all outputs open-circuit, no supply current delivered to external circuits.
9. R_s = total series resistance = R_{BAT} + SRL + $R_{DS(on)}$ + ESR.
10. The minimum supply voltage is determined by the start-up sequence of the device. When the start-up sequence is completed, the supply voltage can be lowered to 1.8 V.
11. The microcontroller operates with approximately1.9 million instructions per second at V_{DD} = 2.2 V. The current consumption at this supply voltage is 0.7 mA/MIPS (peripheral blocks as e.g. timers, DC/DC converter, I²C-bus, UART, demodulator etc., are excluded). The current required from V_{DD} is then 1.35 mA (typ.). This scales to

$$I_{BAT} = \frac{V_{DD}}{V_{BAT}} \times I_{DD} = 2.5 \text{ mA sunk from } V_{BAT}.$$

12. In mass program mode the current can increase to 100 mA.
13. This parameter is not tested during production; it is guaranteed by design.

11 AC CHARACTERISTICS

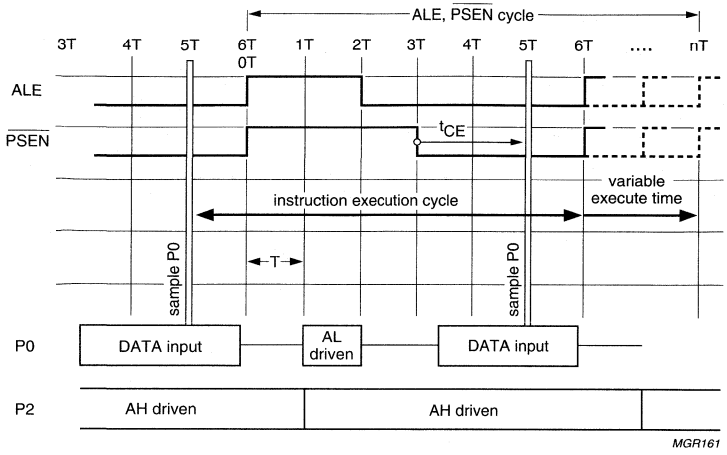
V_{BAT} = 0.9 to 1.6 V; V_{SS} = 0 V; T_{amb} = −10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
DC/DC converter; note 1						
t_{on}	turn on time	off to normal operation; I_L < 500 µA; note 2	–	–	5	ms
$t_{ch(mode)}$	mode change time	enable to standby and reverse; note 2	–	–	1	ms
t_{step}	load step accommodation delay until stable	load step from 10 µA to 6 mA; note 3	–	–	1	ms
f_{sw}	switching frequency	in normal mode; note 2	120	250	400	kHz
		in standby mode	–	f_{XTL1}	–	kHz
$t_{ch(L)}$	inductor charge time	in standby mode; note 4	–	$\frac{1}{2}t_{XTL1}$	t_{XTL1}	µs
RESET signal						
$t_{RESETIN(min)}$	minimum duration of RESETIN pulse		20	–	–	µs
Microcontroller						
$t_{instr(int)}$	internal instruction execution time	internal access; V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	550	–	ns
$t_{instr(ext)}$	external instruction execution time	external access; V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	650	–	ns
76.8 kHz oscillator						
f_{xtal}	crystal frequency	note 3	76784	76800	76816	Hz
$f_{i(max)}$	max input frequency through input buffer		–	–	100	kHz
C_1	input capacitance		–	10 ±15%	–	pF
C_2	output capacitance		–	10 ±15%	–	pF
6 MHz oscillator						
$f_{i(osc)}$	oscillator input frequency	($\overline{SF4}$, SF3, SF2, SF1, SF0) = 00000 (reset condition)	3	5.4	8	MHz
		($\overline{SF4}$, SF3, SF2, SF1, SF0) = 10000	1	2.7	5	MHz
		($\overline{SF4}$, SF3, SF2, SF1, SF0) = 01111	6	7.6	11	MHz
$f_{i(osc)} \pm \Delta f$	adjusted frequency		5.85	6	6.15	MHz
$t_{d(en)}$	enable oscillator delay	note 2	–	20	30	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
ZIF (I and Q) demodulator						
f_{offset}	offset from 0 frequency	note 2	6	–	–	kHz
S/N	minimum signal strength	3% bit error rate; note 2	–	–	–95	dB(m)
$t_{(ENA-AVG)}$	ENA to valid AVG value	3 kHz offset; note 2	–	–	100	ms
t_{ENB}	ENB to valid demodulator output	24 samples per symbol; note 2	–	–	1	symbol duration
t_{ENC}	ENB to correct recovered clock	note 2	12/12 positive/negative transitions of data			
t_{BR}	changing baud rate to correct recovered clock	note 2	2/2 positive/negative transitions of data			
All outputs						
$t_{r,f}$	rise and fall times for outputs	C_L = 20 pF	–	15	–	ns
Open-drain pins SDA and SCL (P1.7 and P1.6)						
t_{noise}	noise suppression filter time		–	60	–	ns
$\Delta V/\Delta t$	slope for the falling edge	R_L = 20 kΩ; C_L = 50 pF; V_{DD} = 2.2 V	–	50	–	ns/V
$\delta I/\delta t$	slope for both edges	R_L = 20 kΩ; C_L = 50 pF	–	250	–	μA/ns
$I_{o(sink)(swL)}$	dynamic output sink current during switching low (Miller compensated)	V_{DD} = 2.2 V; R_L = 20 kΩ; C_L = 50 pF	–	2	–	mA
OTP programming characteristics						
$t_{SU;VPP}$	V_{PP} set-up time		10	–	–	μs
$t_{W(prog)}$	program pulse width		100	–	–	μs
$t_{W(prog)(sec)}$	program pulse security bits		200	–	–	μs
$t_{W(prog)(rec)}$	program pulse recover time		1	–	–	μs
AFC-DAC						
$t_{start(DAC)}$	start-up time disabled DAC to stable output for code 111111	note 2	–	50	100	μs
PSRR	power supply ripple rejection (V_{DD} -> DAC)		–	0	–	dB
t_{slew}	slew time for analog output from 10 to 90% for a voltage step of 1 V	code 010000 <-> 110000	–	2.5	–	μs

Notes

1. DC/DC converter configured with inductor of L = 470 μH, SRL = 5 Ω, input capacitance of C_i = 4.7 μF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 μF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. This parameter is not tested during production; it is guaranteed by design.
3. This parameter depends on external components.
4. At high load or low battery voltage the inductor charge time can be extended to a full XTL1 period, while the minimum inductor discharge time remains an $\frac{1}{2}t_{XTL1}$ period.
5. The execution time is strongly dependant on command type and addressing mode (see Table 60).



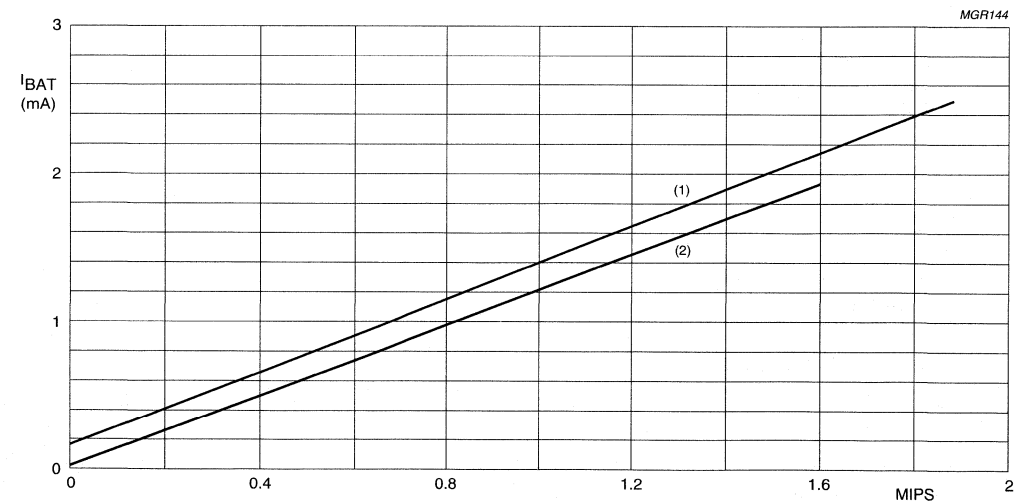
T being the half period of the internal 6 MHz oscillator for normal external access and of TCLK for emulation, programming and test modes.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, temperature and opcode).

Execution of an opcode goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.39 External access timing.

12 CHARACTERISTIC CURVES

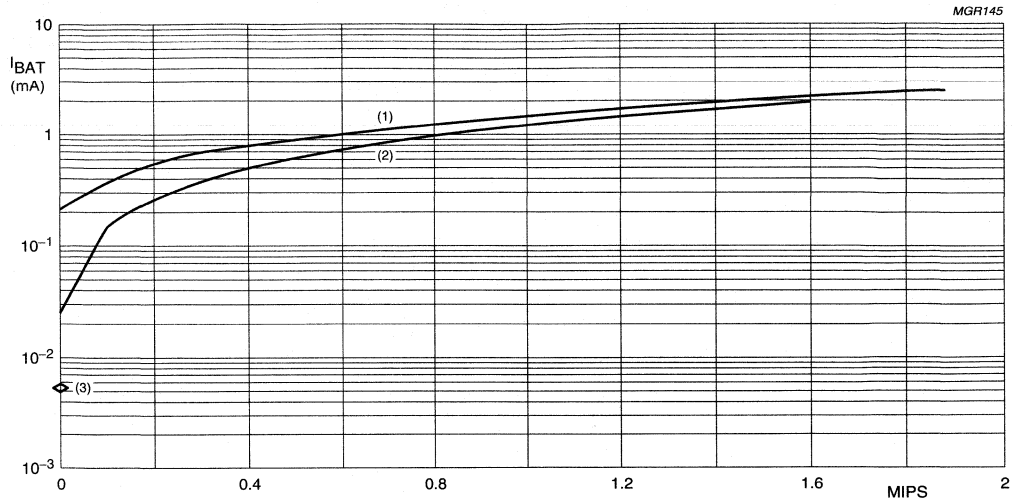


V_{BAT} = 1.2 V.

(1) DC/DC converter in normal mode.

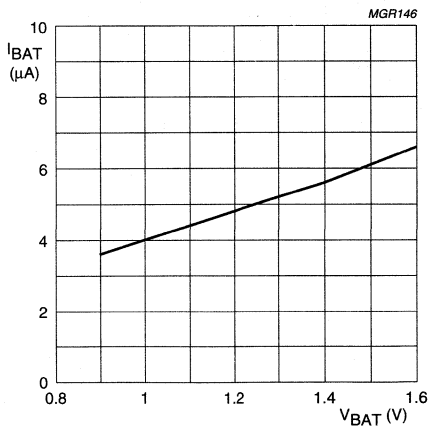
(2) DC/DC converter in standby mode.

Fig.40 Measured battery current consumption as function of mean microcontroller instruction rate.



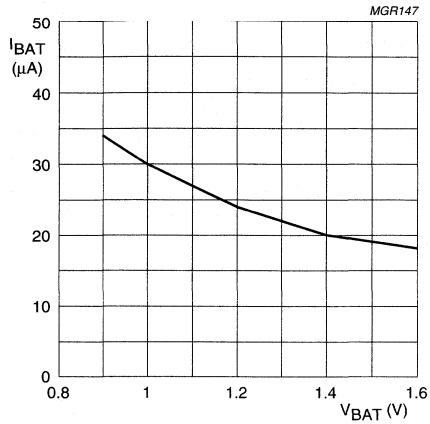
V_{BAT} = 1.2 V.
(1) DC/DC converter in normal mode.
(2) DC/DC converter in standby mode.
(3) DC/DC converter in off mode.

Fig.41 Measured battery current consumption as function of mean microcontroller instruction rate.



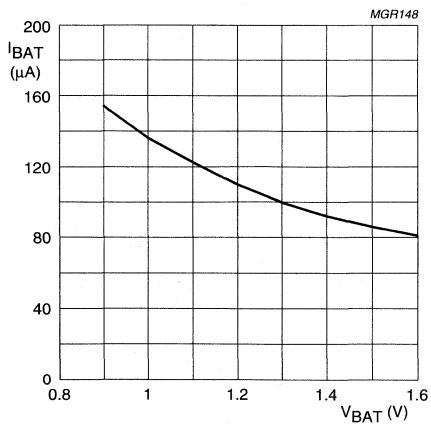
$V_{DD} = V_{BAT}$, microcontroller idle, all functions disabled.

Fig.42 Supply current in off mode.



V_{DD} = 1.9 V, microcontroller idle, all functions disabled.

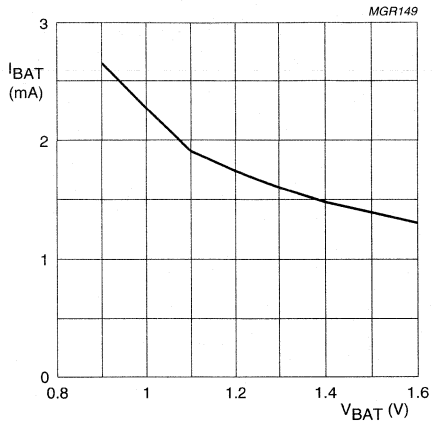
Fig.43 Supply current in standby mode.



V_{DD} = 2.2 V, microcontroller idle, all functions disabled.

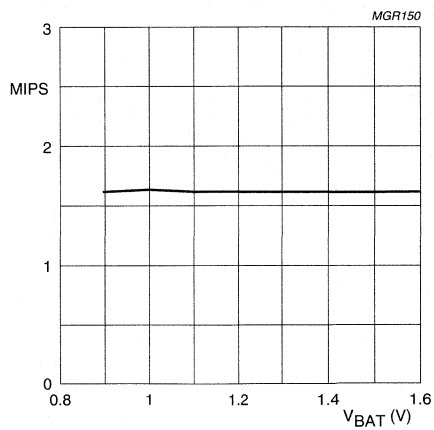
This curve cannot be directly measured by varying V_{BAT} because the shown current is the battery current in discontinuous mode. Changing the battery voltage can force the DC/DC converter to enter the continuous mode. At a given battery voltage a mode change from continuous to discontinuous mode happens only after a load reduction.

Fig.44 Supply current in normal mode.



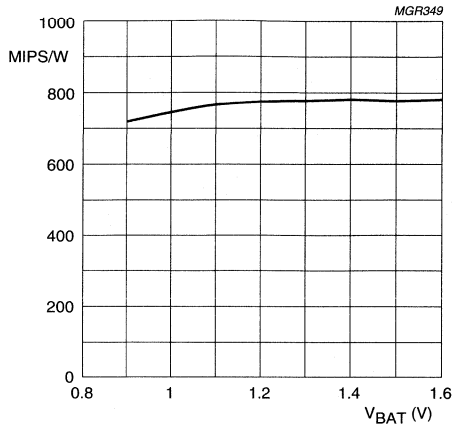
V_{DD} = 1.9 V, microcontroller running at approximately 1.6 MIPS, all other functions disabled.

Fig.45 Supply current in standby mode.



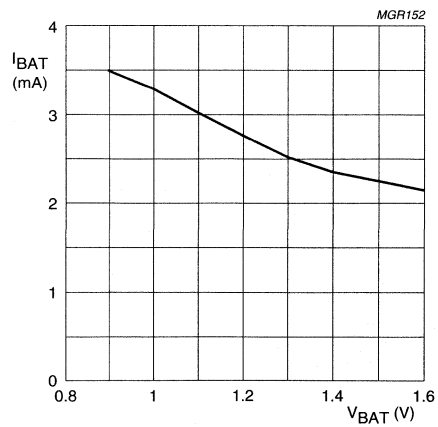
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.46 CPU speed performance with DC/DC converter in standby mode.



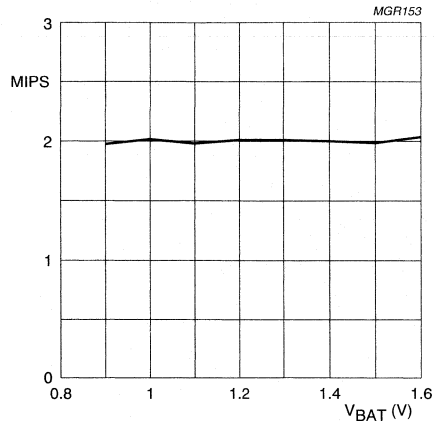
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.47 Overall power/speed performance with DC/DC converter in standby mode.



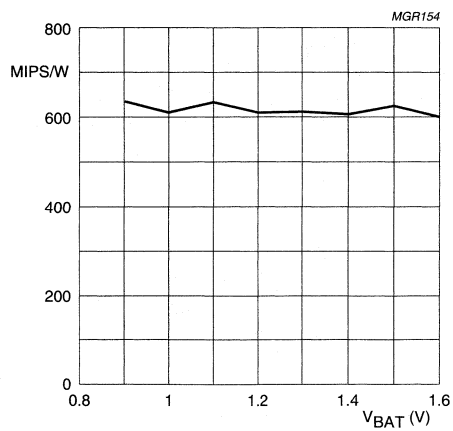
V_{DD} = 2.2 V, microcontroller running at approximately 2 MIPS, all other functions disabled.

Fig.48 Supply current in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.49 CPU speed performance with DC/DC converter in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.50 Overall power/speed performance with DC/DC converter in normal mode.

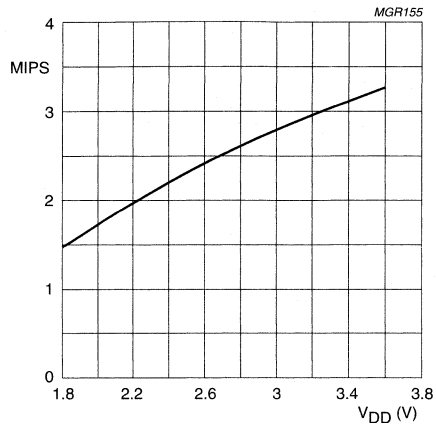


Fig.51 Speed performance PCA5007 when V_{DD} is externally supplied (DC/DC converter not used).

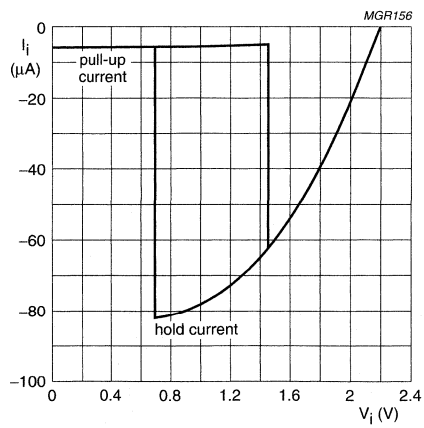


Fig.52 Typical impedance characteristic of standard port in input mode.

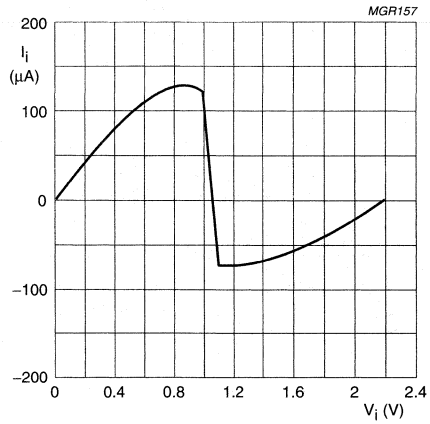
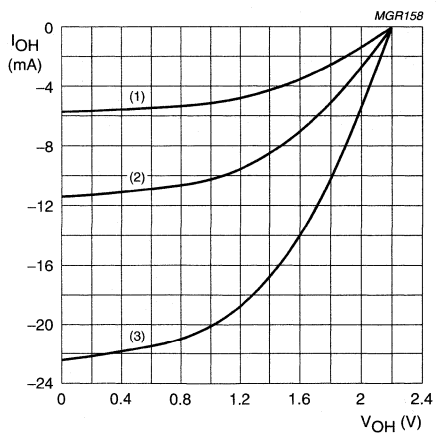
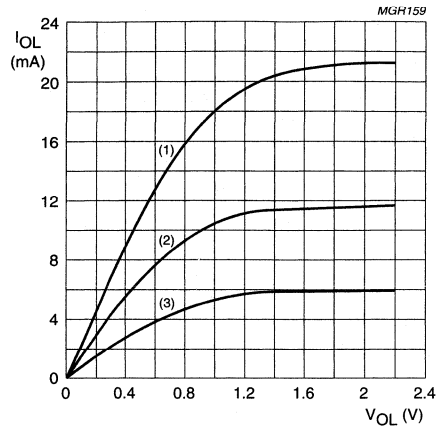


Fig.53 Typical impedance characteristic of $\overline{EAN}$ pin in input mode.



(1) Pins P0.X, P1.X, P2.X, $\overline{PSEN}$ and $\overline{EAN}$.
(2) Pins $\overline{RESOUTN}$ and ALE.
(3) Pins P3.X and AT.

Fig.54 Typical output characteristics driven HIGH (digital output/port pins except P1.6 and P1.7).



(1) Pins P3.X and AT.
(2) Pins $\overline{\text{RESOUTN}}$ and ALE.
(3) Pins P0.X, P1.X, P2.X, $\overline{\text{PSEN}}$ and $\overline{\text{EAN}}$.

Fig.55 Typical output characteristics LOW (digital output/port pins except P1.6 and P1.7).

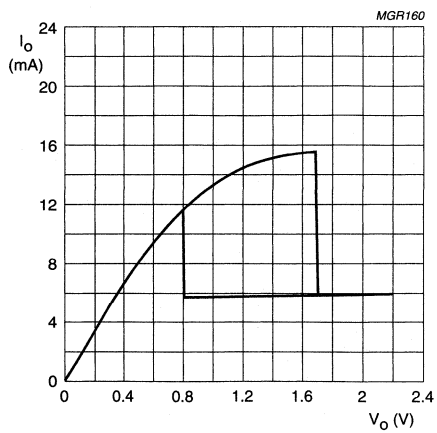


Fig.56 Typical output characteristics LOW for P1.6 and P1.7.

13 TEST AND APPLICATION INFORMATION

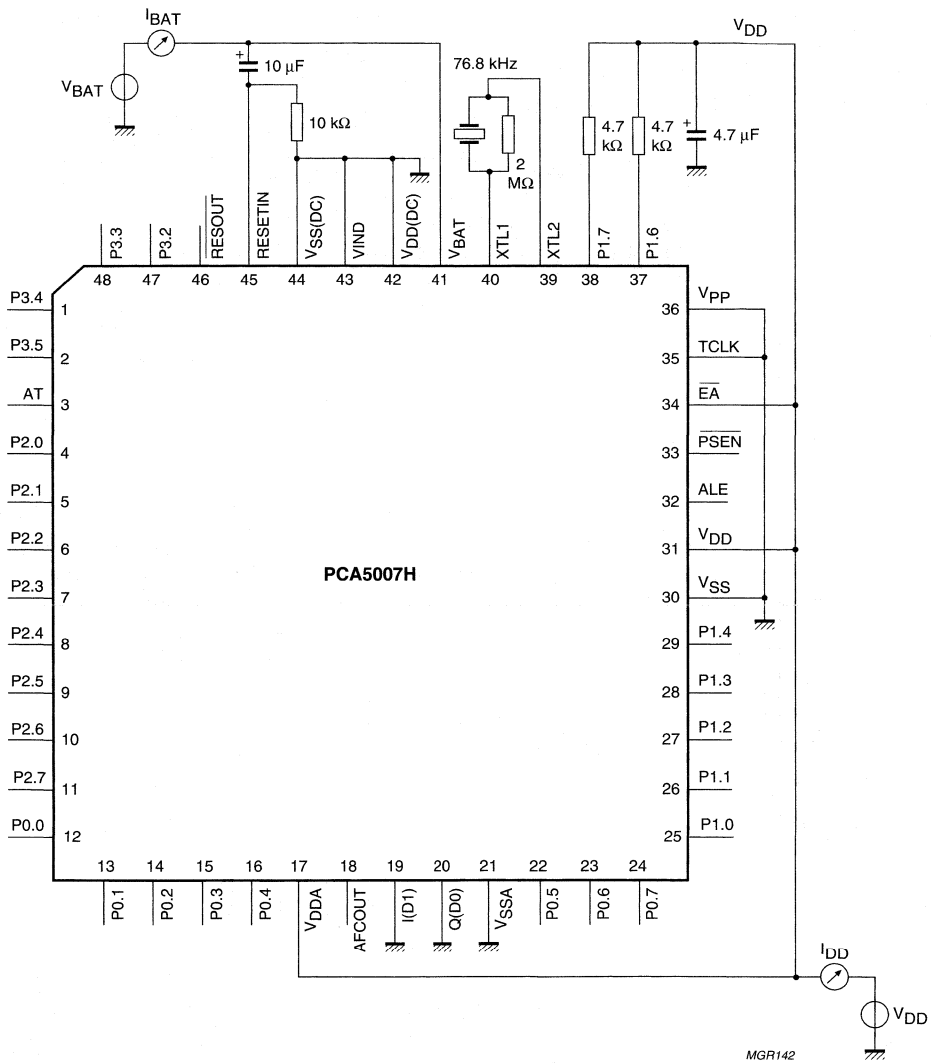


Fig.57 Test circuit for current measurements with external V_{DD} supply.

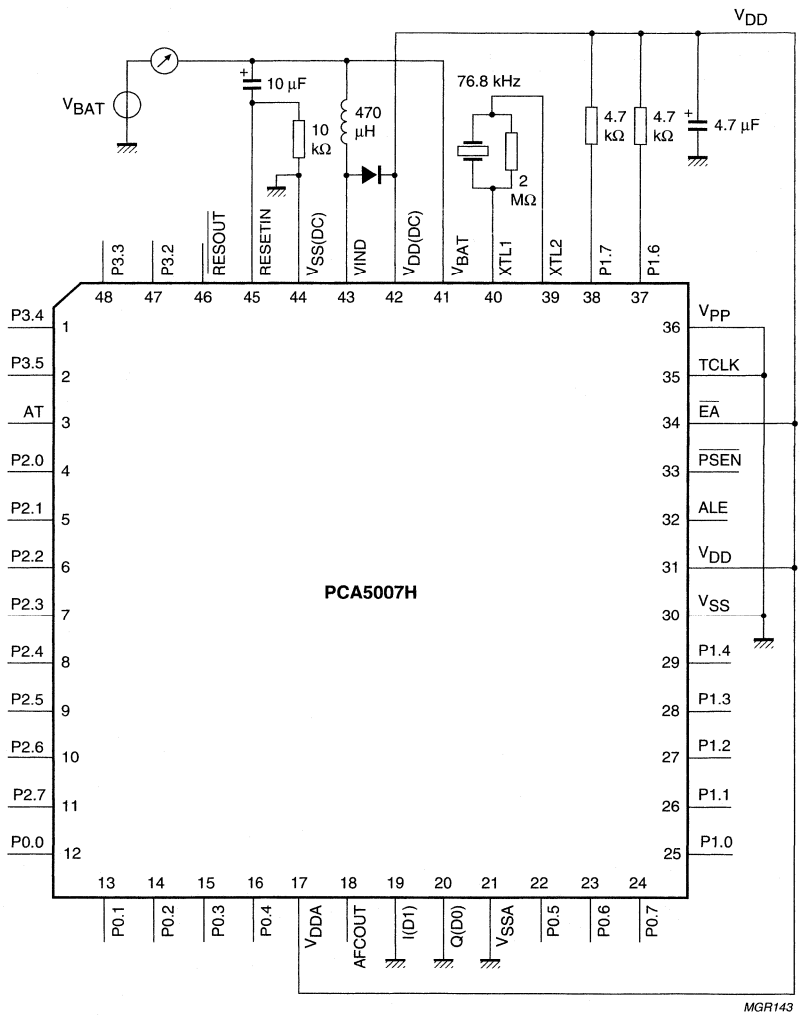


Fig.58 Test circuit for current measurements with on-chip DC/DC converter.

14 APPENDIX 1: SPECIAL MODES OF THE PCA5007

14.1 Overview

During the rising edge of the external $\overline{\text{RESOUT}}$ signal, the state of pins ALE, $\overline{\text{PSEN}}$ and $\overline{\text{EA}}$ and P2.X is sampled and stored. The following decoding (ALE, $\overline{\text{PSEN}}$ and P2) is used to force the PCA5007 into different operating modes:

[1, 1, X] → RUN mode

[0, 1, X] → EMUlation modes (for P2 decoding refer to Metalink documents)

[1, 0, Y] → test mode, submode Y

[0, 0, X] ≥ OTP parallel programming mode.

The customer will usually only see the normal RUN mode.

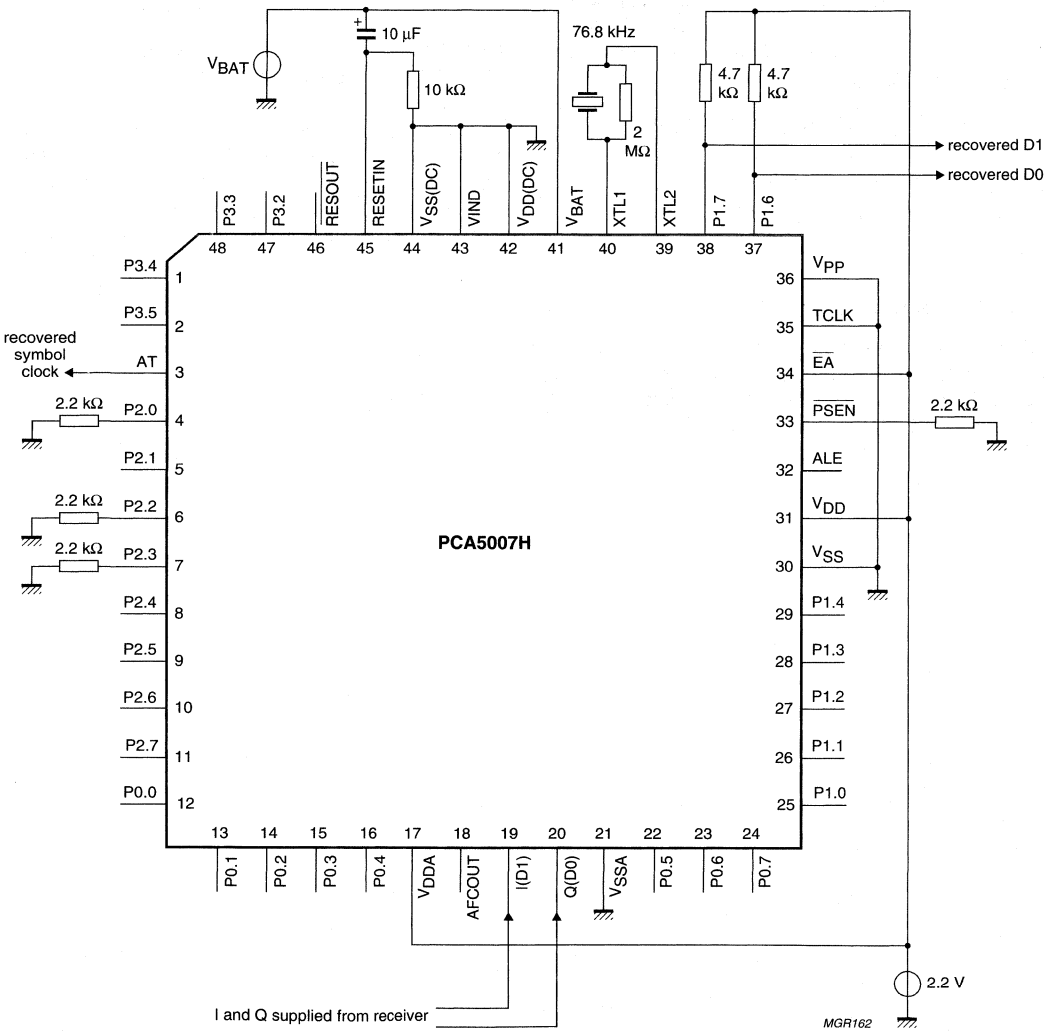
14.2 OTP parallel programming mode

The OTP parallel programming mode is used to access the on-chip OTP directly from the device pins for programming and verification. The OTP parallel programming mode and its initialization are explained in detail in Chapter 15.

14.3 Test modes

The test modes of the PCA5007 are used during the production test of the circuit. Test modes are not intended to be used by customers except test mode 2, the demodulator and clock recovery test mode.

Test mode 2 may be used by customers for Bit Error Rate (BER) measurements in closed-loop systems.
The following application diagram (see Fig.59) shows an application, which enters this mode during start-up. After the test mode is entered the PCA5007 starts execution of code from the internal program memory. This code must enable the demodulator and clock recovery in the required modes. If the microcontroller is requested to make port I/O, then a frequency of approximately 6 MHz with V_{DD} level needs to be supplied at the TCLK pin.



The OTP must contain code that enables the demodulator and clock recovery in the desired operating modes.

Fig.59 Application diagram for entering the demodulator test mode after reset.

15 APPENDIX 2: THE PARALLEL PROGRAMMING MODE

15.1 Introduction

This section describes the parallel programming mode of the PCA5007. Parallel programming mode is the mode where the OTP is programmed by an EPROM programmer or by a tester.

15.2 General description

The PCA5007 is packaged in a LQFP48 package. Port 0 and Port 2 are available for programming. To program the OTP of the PCA5007, multiplexing of addresses and data is necessary. Port 0 is a bidirectional data port, used for the memory addresses and the program and verify data. Port 2 is an input port which controls the parallel programming mode. A coarse block diagram of the OTP interface in parallel programming mode is given in Fig.60.

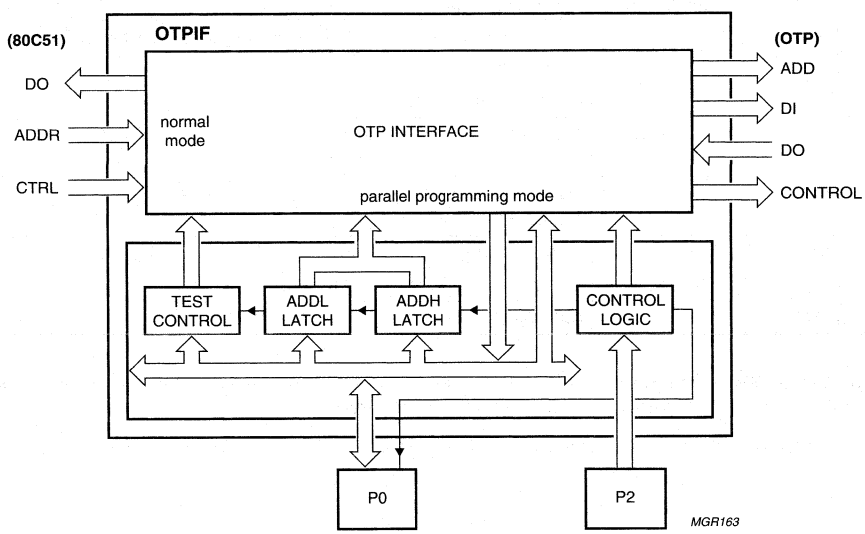


Fig.60 The OTP interface in parallel programming mode.

15.2.1 SIGNALS FOR THE PARALLEL PROGRAMMING MODE

In this configuration, the following signals are necessary to program the OTP:

Table 63 Pins for programming mode

OTP PIN	TYPE	EPROM PIN	DESCRIPTION	COMMENTS
V_{PP}	supply	V_{PP}	programming voltage	special pin/logic signal not time critical
V_{DD}	supply	V_{DD}	positive supply	
GND	supply	GND	negative supply	
P0.7 to P0.0	I/O	A<14:0>	address	20 kbyte addresses available
		Q<7:0>	data output	
		I<7:0>	data input	
		PS<2:0>	security bits input	connected to P0.2 to P0.0 pins
		QS<2:0>	security bits output	
P2.0/LS0	input	–	latch select 0	latch select signals, see Table 64
P2.1/LS1	input	–	latch select 1	
P2.2/PGM	input	–	programming mode	
P2.3/RdStrb	input	CEP/MBPC	read/strobe	read enable Clock (CEP) when PGM = 0; strobe for the latches when PGM = 1
P2.4/GBMbpB	input	GB	output enable not/ Mult.BProg Not	read EPROM and set P0 as output; multiple byte programming when PGM = 1
P2.5/WEB	input	WEB	Write Enable not	programs data if V_{PP} is present
P2.6/SEC	input	SEC	select security bits	see Section 15.10
P2.7/SIG	input	SIG	read signature bytes	see Section 15.9

The control signals GBMbpB, PGM, LS1 and LS0 can be used to select the latches of the interface block and the internal data latches of the OTP. Table 64 shows how the latches are selected.

RdStrb is used to open the selected latch. If PGM is not active the RdSTrb signal is used to start the OTP read cycle.

Table 64 Latch selection

P2.4/GBMbpB	P2.2/PGM	P2.1/LS1	P2.1/LS0	DESCRIPTION
X	0	X	X	no latches selected
1	1	0	0	select test control latch
X	1	0	1	select lower address latch
X	1	1	0	select upper address latch
0	1	1	1	select internal data latch in multi byte programming mode

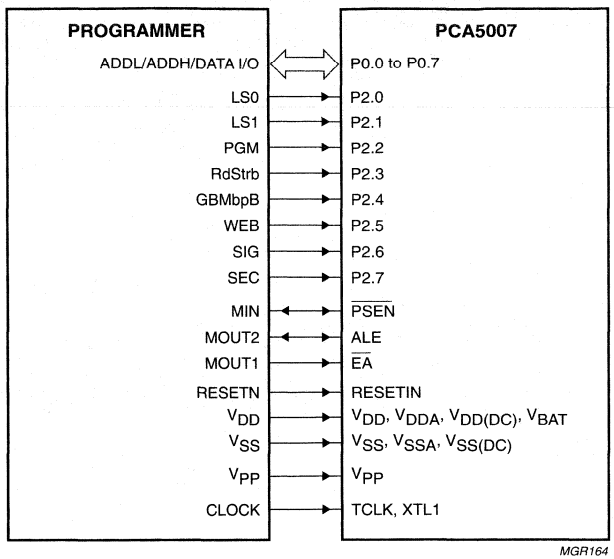


Fig.61 Parallel programming mode.

15.3 Entering the parallel programming mode

The parallel programming mode has been implemented as a general test mode of the PCA5007. This mode can be entered by applying 000 to pins $\overline{PSEN}$, ALE and $\overline{EA}$ during reset. For the initializing sequence a clock of 76.8 kHz at XTL1 is expected and the supply voltage V_{DD} must be higher then 2.2 V. At the rising edge of $\overline{RESOUT}$ these signals are latched and the code 000 leads to parallel programming mode. The high voltage pin V_{PP} can be either HIGH or V_{DD}.

Since $\overline{PSEN}$ and ALE are output signals of the PCA5007 after reset, a pull-down (strong enough to overdrive the internal 100 µA pull-up of the PCA5007) should be used to drive the outputs LOW. Alternatively the LOW can be driven with a 3-state buffer which is enabled with $\overline{RESOUT}$ = LOW.

The microcontroller fetches instructions from Port 0 in external mode. Data fetching is controlled by $\overline{PSEN}$ and ALE. This is the standard data fetch in external mode. A clock has to be supplied to TCLK while entering the parallel programming mode. Before entering the parallel programming mode, Port 2 should be set to 30H and the microcontroller should be put in Idle mode by setting the bit PCON.0 (address 87H).

The test mode is activated by making $\overline{EA}$ equal to logic 1. The mode entering sequence is given in Table 65.

Before entering the parallel program mode Port 2 can be an output port (dependent on the reset configuration of this port). As soon as the parallel programmed mode is entered Port 2 is an input.

After entering the parallel programming mode this mode has to be initialized. The OTP test latch has to be loaded with code 01H to set the sense amplifiers in verify mode. Before a byte can be programmed a verify has to be performed to ensure that the programming is not blocked by the security (see Section 15.10). The address of this verify cycle is not important and the address latches do not have to be loaded. After this initialization the PCA5007 is ready for programming. Parallel program mode initialization is shown in Fig.64.

The security check can be replaced by another read action e.g. reading the security or signature bytes (see Section 15.9).

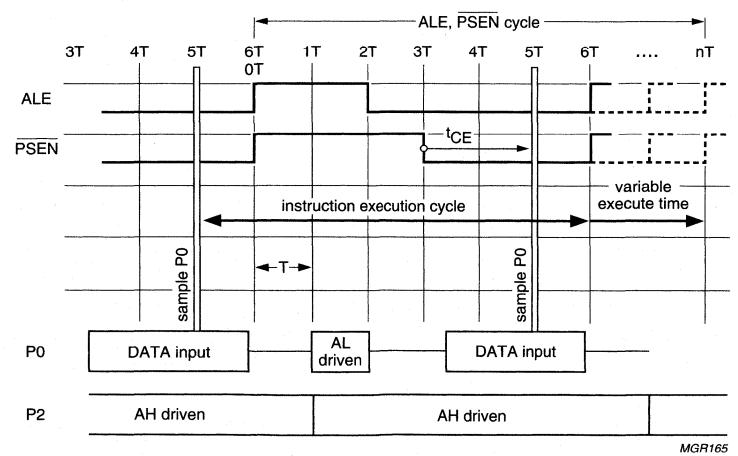
It should be noted that this paragraph is only applicable for the first series. It can be neglected in the future. To prevent problems with the self timed loop it is advised to set the circuit in DC read mode during verify. This is achieved by writing 09H instead of 01H into the OTP test latch.

Table 65 Entering the parallel programming mode; note 1

PINS $\overline{PSEN}$, ALE AND $\overline{EA}$	RESETIN	$\overline{RESOUT}$	PORT 0	DESCRIPTION
000	1	0	XX	reset
000	0	0	XX	259 or more slow clocks at XTL1
000	0	0 → 1	XX	prepare parallel programming mode, enter external access mode, now clocks must be provided on TCLK
ZZ0	0	1	02	LJMP 3000H
ZZ0	0	1	30	force P2 to 30H
ZZ0	0	1	00	
ZZ0	0	1	00	discard fetch cycle
ZZ0	0	1	75	MOV PCON, 01H
ZZ0	0	1	87	make microcontroller idle
ZZ0	0	1	01	
ZZ0	0	1	01	discard fetch cycle
ZZ1	0	1	XX	parallel programming mode active

Note

1. Z = pin is output.



T is the half period of the clock signal supplied to TCLK.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, temperature, opcode).

Execution of an opcode goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.62 External access timing for programming mode entry.

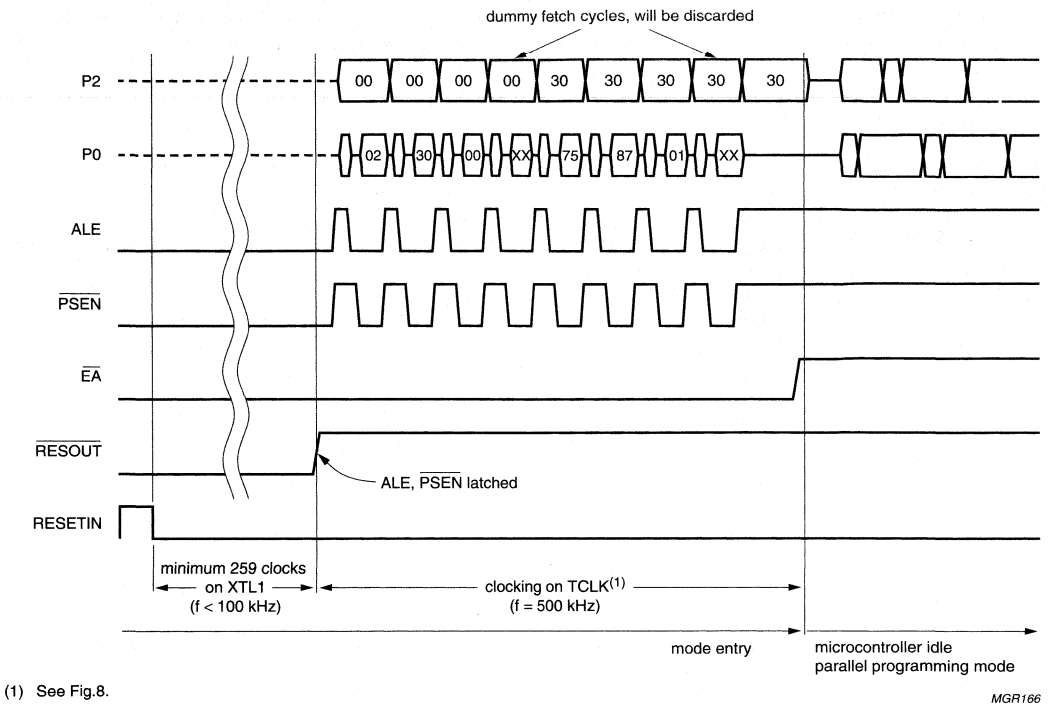


Fig.63 Program mode.

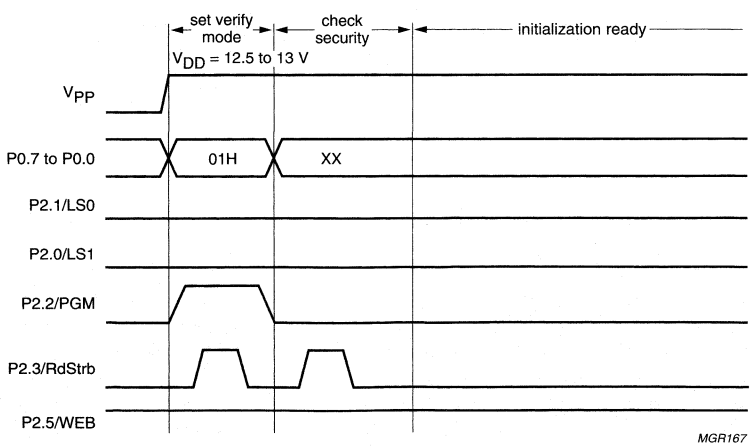


Fig.64 Parallel program mode initialization.

15.4 Address space

The PCA5007 has a 20 kbytes memory and therefore 15 address pins. Applying an address above 32 kbytes (address<15> = 1) leads to the selection of the extra rows. The user should not apply these addresses during programming.

15.5 Single byte programming

Programming and verifying is shown in Fig.65. The upper and lower address byte are loaded one after the other. The address latch control signals select the proper latch and the RdStrb signal opens the latch (level sensitive). The order of loading the latches is not important. The data is latched if write enable bar becomes active. After programming a byte, this byte can be verified without reloading the addresses. If more bytes are programmed after each other having the same upper address, it is not necessary to reload this upper address.

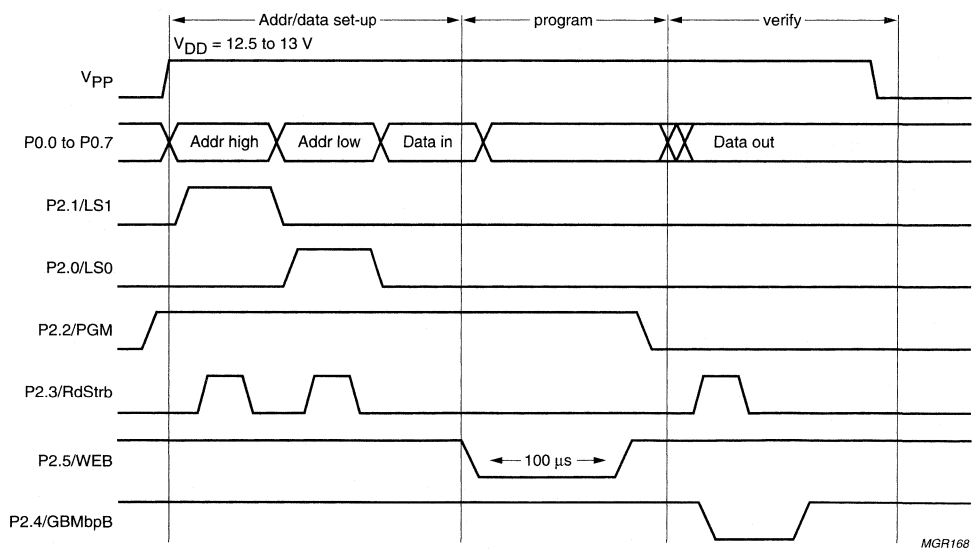


Fig.65 Single byte programming mode.

15.6 Multiple byte programming

A multiple byte programming mode has been implemented to increase programming speed. In this mode four bytes can be programmed in parallel. The addresses of these four bytes have to be equal except for bit 0 and bit 1. Loading the address and data latches is enabled by making PGM HIGH and GBMbpB LOW at the same time. Figure 66 shows the address and data set-up and the program pulse. Loading the upper address is only necessary if it differs from the upper address of the previous quadruple of bytes. In this mode the data latches are controlled by the RdStrb signal (level sensitive). Figure 67 shows the verification in this mode. It should be noted that data 3 is verified before data 0. If this is unwanted the lower address byte of data 0 has to be loaded before verifying data 0 and the lower address byte of data 1 before verifying data 1.

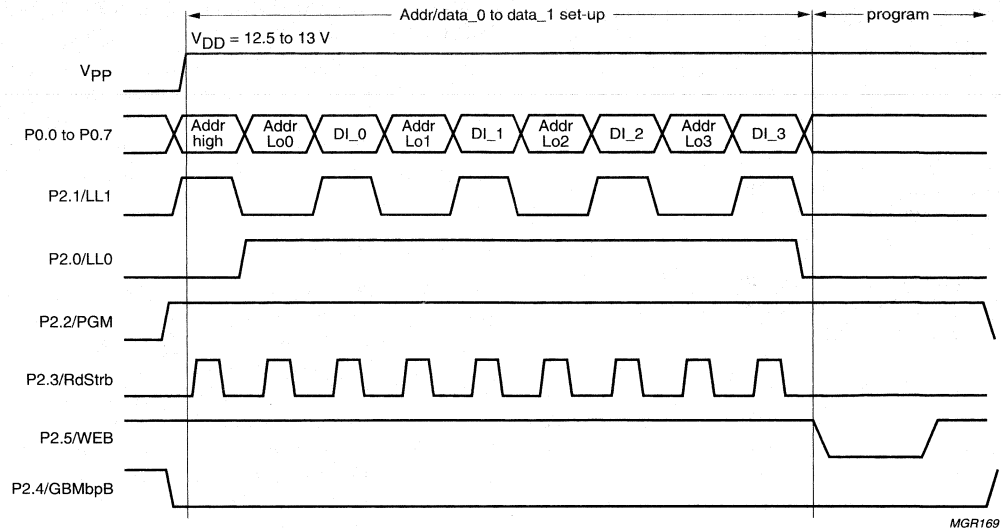


Fig.66 Multiple byte programming mode (address and data load, programming pulse).

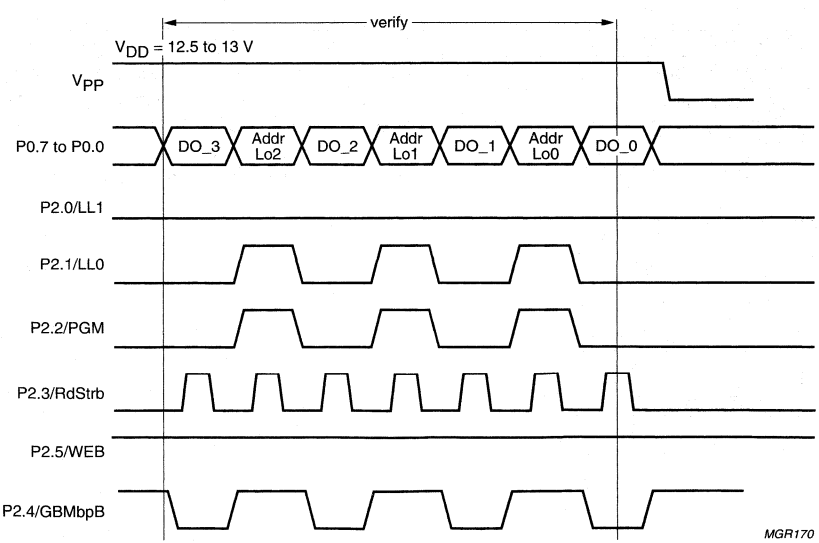


Fig.67 Multiple byte programming mode (verify).

15.7 High voltage timing

The external program voltage V_{PP} has to be HIGH while a program pulse is applied (WEB active). During verify it can be either high or equal to the supply voltage. V_{PP} has to be stable for at least 10 µs before a program pulse can be applied.

After applying a program pulse a recover time of 1 µs is needed to discharge the internal high voltage nodes. During this recover time the memory cannot be accessed for verify.

Due to the above mentioned set-up time programming time is reduced if V_{PP} is continuously HIGH during programming and verifying.

15.8 OTP test modes

OTP test modes will be selected from a test control latch which can be loaded in parallel programming over Port 0. The advantage of this is that the test modes of the OTP are independent of the microcontroller. Table 66 shows the OTP test modes coded in 7 bits. When a test mode is loaded the control signals on Port 2 keep their original functionality and can be used to execute the test mode.

Table 66 Definition of test modes

TCL(7 TO 0)	TEST MODE
00000000	normal mode (no test active)
XXXXXX01	verify mode (self timed)
XXXXXX10	margin 0 mode
XXXXXX11	margin 1 mode
XXXXX1XX	margin VP mode is active
XXXX1XXX	DC_Read mode is active
X001XXXX	drain stress test mode
X010XXXX	gate stress test mode
X011XXXX	mass programming test mode
X100XXXX	even column test mode
X101XXXX	odd column test mode
X110XXXX	even row test mode
X111XXXX	odd row test mode
1XXXXXXX	OTP interface test

The encoding is such that combinations of test modes are possible, for instance TCB(7 to 0) = 00001100 enables both the margin VP and DC_Read test modes.

The so called vt mode, needed to measure analog cell characteristics, can be entered by making both P2.6/SIG and P2.7/SEC active (see Fig.61). During normal programming this mode should not be entered therefore **it is forbidden to make P2.6/SIG and P2.7/SEC HIGH at the same time**.

15.8.1 Mass program mode

The mass program mode can be used to program checker boards. If this mode is active every internal data latch is connected to four bit lines and 128 bits can be programmed in parallel. To write a checker board 0011X0XX has to be loaded in the test register and the circuit has to be set in the parallel program mode (P2.2/PGM = 1 and P2.4/GBMbpB = 0). Then data from address 00H is loaded to address 00 03H down to 00 00H. For every even word line (A<6> = 0) a program pulse has to be given at low addresses X0000000 and X0001000. For the odd lines (A<6> = 1) the pulses have to be applied to low address x100_0100 and x100_1100. In the user address space a checker board can be programmed with 320 × 2 = 640 program pulses.

15.9 Signature bytes

Three signature bytes are available to identify the device. These bytes can be read by doing a verify while the SIG input (Port 2.6) is active. The contents of the signature bytes is given in Table 67. Applying a write pulse while the SIG input is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes are always readable independent on the security.

Table 67 Addresses and contents of the signature bytes

ADDRESS	CONTENTS
00 30H	15H
00 31H	C7H
00 60H	00H

15.10 Security

To prevent programming or reading of EPROM contents by third parties security can be set by programming the security bits. These bits are located outside the normal memory matrix and have input and output lines separated from the normal OTP I/Os. Three bits are present, but only two are actually used. The third bit can be used for future extensions. Different levels of security can be set by programming one or more bits. The bits are read in parallel at every read cycle and interpreted with the following definition:

- Level 0, bits 000, no security, no restrictions
- Level 1, bits 001, program disabled
- Level 2, bits 011, program and verify disabled.

The third security may be programmed without affecting the functionality. However only the combinations 000, 001, 011 and 111 are possible.

After reset security Level 1 is loaded. To enable programming a read or verify (GB pulse not necessary) is needed to check the actual security level.

The security bits can be programmed the same as normal bits. The bits have to be supplied to the three least significant bits of Port 0.

The SEC bit of Port 2 (bit 7) has to be HIGH during the program cycle. Loading an address is not necessary. If Port 2.7/SEC is HIGH during verify, the security bits can be read on the three least significant bits of Port 0. After programming 011 to the security bits only the security bits and the signature bytes can be verified and verifying the normal addresses is not possible any more. Verifying a normal address while security Level 2 has been programmed will result in reading 00H.

The programming time for the security bits is 200 µs instead of 100 µs for a normal bit. This extra time can be reached by applying one 200 µs program pulse or by applying two standard pulses.

Although in this OTP an unprogrammed cell is a logic 1 and a programmed cell is a logic 0, a logic 1 has to be programmed to increase the security level. The inversion is performed by the interface block.

Since the security is checked at every read or verify access, verifying is disabled immediately after programming security Level 2. Programming is disabled if a verify or a reset is applied after programming security Level 1 or higher.

16 APPENDIX 3: OS SHEET

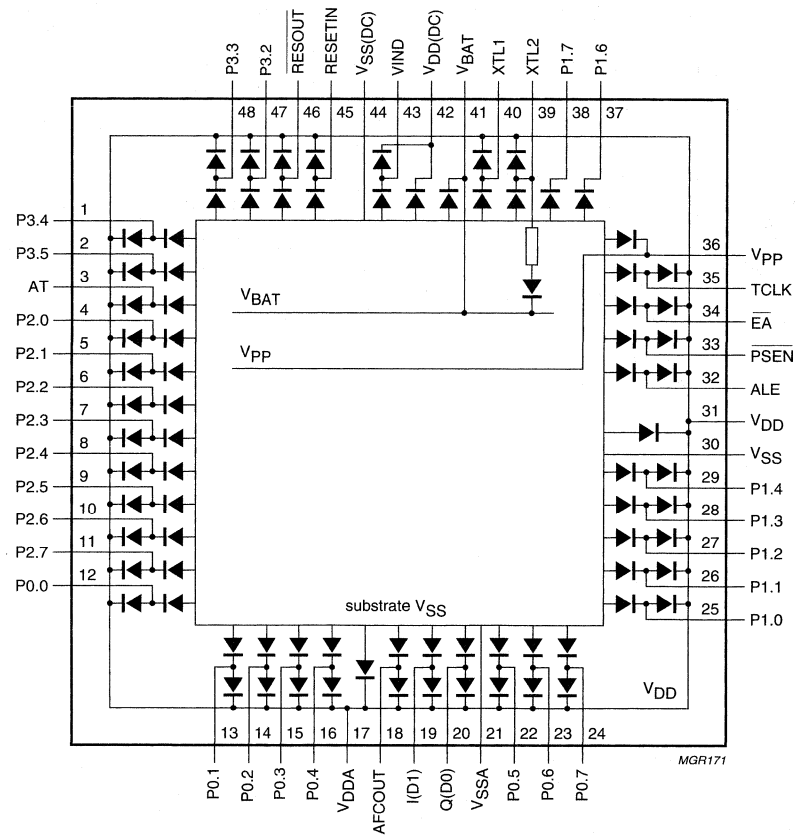


Fig.68 Open/short-circuit diagram for PCA5007.

17 APPENDIX 4: BONDING PAD LOCATIONS

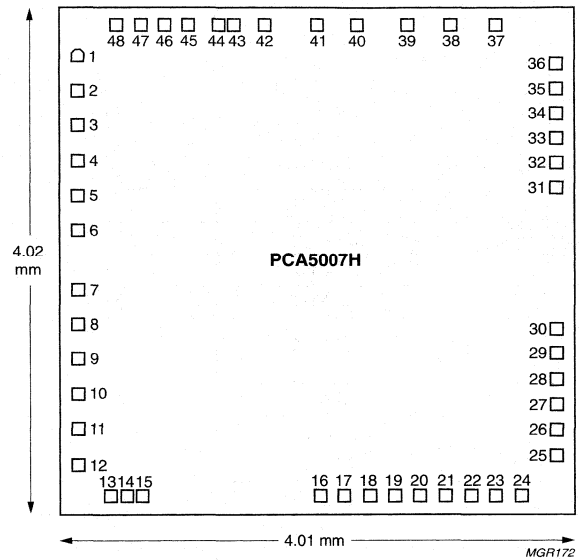


Fig.69 Bonding pad locations.

Table 68 Bonding pad locations (dimensions in μm)

PAD	SYMBOL	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
1	P3.4	91.0	3567.0	87.0
2	P3.5	91.0	3292.0	87.0
3	AT	91.0	3017.0	87.0
4	P2.0	91.0	2742.0	87.0
5	P2.1	91.0	2467.0	87.0
6	P2.2	91.0	2192.0	87.0
7	P2.3	91.0	1710.0	87.0
8	P2.4	91.0	1435.0	87.0
9	P2.5	91.0	1160.0	87.0

PAD	SYMBOL	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
10	P2.6	91.0	885.0	87.0
11	P2.7	91.0	610.0	87.0
12	P0.0	91.0	335.0	87.0
13	P0.1	330.0	91.0	87.0
14	P0.2	457.5	91.0	87.0
15	P0.3	580.0	91.0	87.0
16	P0.4	1972.5	91.0	87.0
17	V_{DDA}	2170.0	91.0	87.0
18	AFCOUT	2365.0	91.0	87.0
19	I(D1)	2555.0	91.0	87.0
20	Q(D0)	2747.5	91.0	87.0
21	V_{SSA}	2940.0	91.0	87.0
22	P0.5	3130.0	91.0	87.0
23	P0.6	3322.5	91.0	87.0
24	P0.7	3515.0	91.0	87.0
25	P1.0	3776.6	408.8	87.0
26	P1.1	3776.6	607.5	87.0
27	P1.2	3776.6	806.2	87.0
28	P1.3	3776.6	1005.0	87.0
29	P1.4	3776.6	1203.8	87.0
30	V_{SS}	3776.6	1400.0	87.0
31	V_{DD}	3776.6	2532.5	87.0
32	ALE	3776.6	2726.5	87.0
33	$\overline{PSEN}$	3776.6	2920.5	87.0
34	$\overline{EA}$	3776.6	3114.5	87.0
35	TCLK	3776.6	3308.5	87.0
36	V_{PP}	3776.6	3502.5	87.0
37	P1.6	3321.7	3811.5	87.0
38	P1.7	2982.4	3811.5	87.0
39	XTL2	2663.1	3811.5	87.0
40	XTL1	2283.8	3811.5	87.0
41	V_{BAT}	1964.5	3811.5	87.0
42	PowerPads_	1550.0	3811.5	84.0
43	PowerPads_	1310.0	3811.5	84.0
44	PowerPads_	1190.0	3811.5	87.0
45	RESETIN	953.2	3811.5	87.0
46	$\overline{RESOUT}$	766.2	3811.5	87.0
47	P3.2	579.2	3811.5	87.0
48	P3.3	392.2	3811.5	87.0

CONTENTS

Pager baseband controller PCA5010

1 FEATURES

- Operating temperature range: −10 to +55 °C
- Supply voltage range with on-chip DC/DC converter: 0.9 to 1.6 V
- Low operating and standby current consumption
- On-chip DC/DC converter generates the supply voltage for the PCA5010 and external circuitry from a single cell battery
- Battery low detector
- Low electromagnetic noise emission
- Full static asynchronous 80C51 CPU (8-bit CPU)
- Recovery from lowest power standby Idle mode to full speed operation within microseconds
- 32 kbytes of One-Time Programmable (OTP) memory and 1.25 kbyte of RAM on-chip
- 27 general purpose I/O port lines (4 ports with interrupt possibility)
- 15 different interrupt sources with selectable priority
- 2 standard timer/event counters T0 and T1
- I²C-bus serial port (single 100/400 kHz master transmitter and receiver)
- Subset of standard UART serial port (8-bit and 9-bit transmission at 4800/9600 bits/s)
- 76.8 kHz crystal oscillator reference with digital clock correction for real time and paging protocol
- Real-Time Clock (RTC)
- Receiver and synthesizer control
  - Receiver control by software through general purpose I/Os
  - Synthesizer control by software through general purpose I/Os
  - 6-bit DAC for AFC to the receiver local oscillator
  - Dedicated protocol timer.
- Decoding of paging data
  - POCSAG or APOC phase 1; advanced high speed paging protocols are also supported
  - Supported data rates: 1200, 1600, 2400, 3125 and 3200 symbols/s using a 76.8 kHz crystal oscillator
  - Demodulation of Zero-IF I and Q, 4 or 2 level FSK input or direct data input
  - Noise filtering of data input and symbol clock reconstruction
  - De-interleaving, error checking and correction, sync word detection address recognition, buffering and more is performed by software
  - All user functions (keypad interface, alerter control, display etc.) are implemented in software.
- Musical tone generator for beeper, controlled by the microcontroller
- Watchdog timer
- 48-pin LQFP package.

2 ORDERING INFORMATION

TYPE NUMBER[1]	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
PCA5010H/XXX	pre-programmed OTP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program.

3 GENERAL DESCRIPTION

The PCA5010 pager baseband controller is manufactured in an advanced CMOS/OTP technology.

The PCA5010 is an 8-bit microcontroller especially suited for pagers. For this purpose, features such as a 4 or 2 level FSK demodulator, filter, clock recovery, protocol timer, DC/DC converter optimized for small paging systems and RTC are integrated on-chip.

The device is optimized for low power consumption. The PCA5010 has several software selectable modes for power reduction: Idle and Power-down mode of the microcontroller and Standby and OFF mode of the DC/DC converter.

The instruction set of the PCA5010 is based on that of the 80C51. The PCA5010 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte.

This data sheet details the properties of the PCA5010. For details on the I^2C-bus functions see *"The I^2C-bus and how to use it"*. For details on the basic 80C51 properties and features see *"Data Handbook IC20"*.

4 BLOCK DIAGRAM

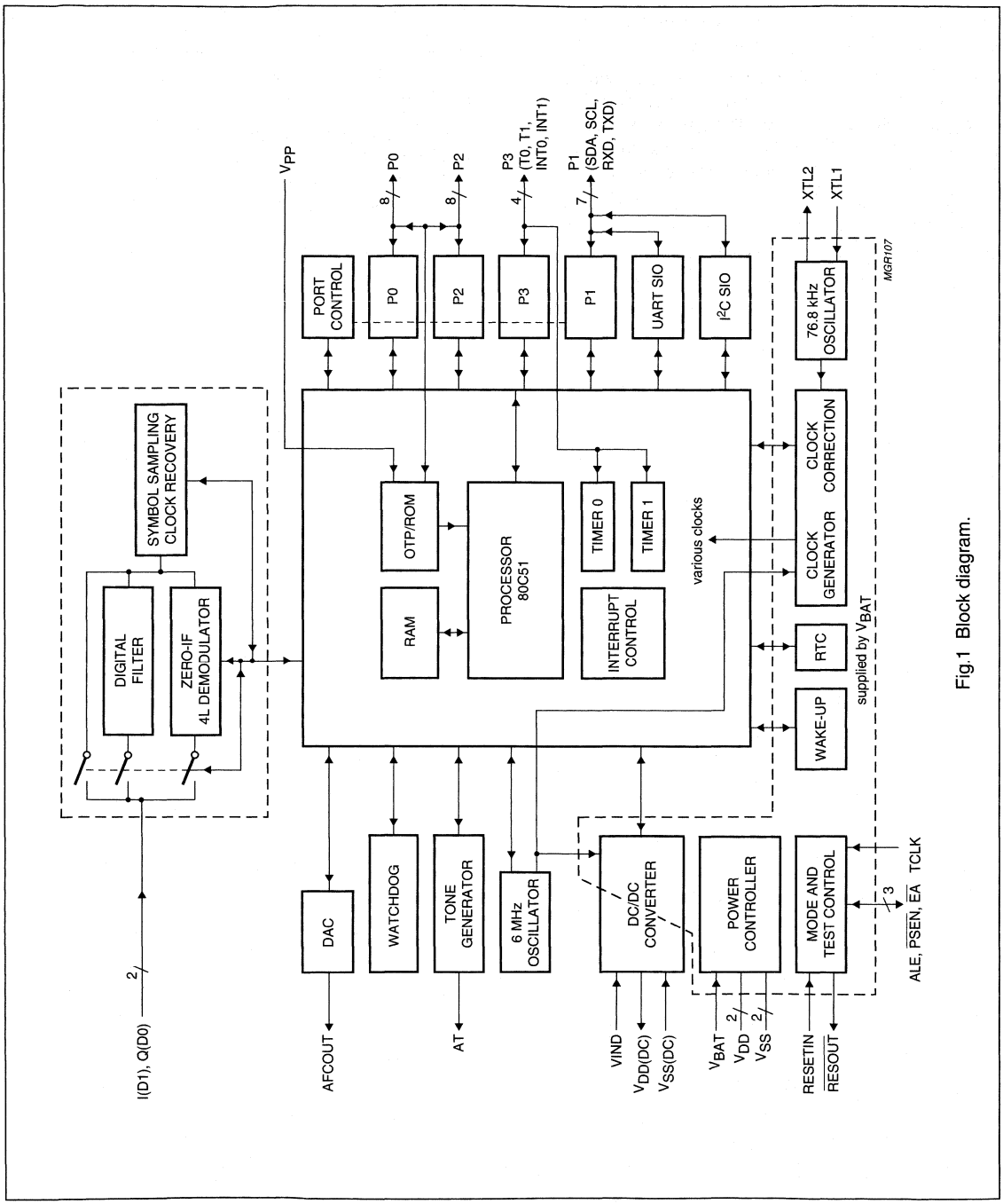


Fig.1 Block diagram.

5 PINNING INFORMATION

SYMBOL	PIN	TYPE	DESCRIPTION
P3.4 and P3.5	1 and 2	I/O	**Port 3:** P3.4 and P3.5 are configured as push-pull outputs only (Option 3R, see Section 6.6). Using the software input commands or the secondary port function is possible by driving the Port 3 output lines accordingly: P3.4 secondary function: T0 (counter input for T0) P3.5 secondary function: T1 (counter input for T1)
AT	3	O	Beeper high volume control output. Used to drive external bipolar transistor.
P2.0 to P2.7	4 to 11	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups (option 1S, see Section 6.6.3). As inputs, Port 2 pins that are externally pulled LOW will source current because of the internal pull-ups. (See Chapter 10: I_{pu}). Port 2 emits the high-order address byte during fetches from external program memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 2 is also used to control the parallel programming mode of the on-chip OTP.
P0.0 to P0.4	12 to 16	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1S, see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during OTP programming verification.
V_{DDA}	17	S	supply voltage for the analog parts of the PCA5010 and the receiver/synthesizer control signals (Port 0 pins)
AFCOUT	18	O	Buffered analog output of DAC for automatic receiver frequency control. A voltage proportional to the offset of the receiver frequency can be generated. Can be enabled/disabled by software.
I(D1)	19	I	Input from receiver: may be demodulated NRZ signal or Zero-IF. In phase limited signal.
Q(D0)	20	I	Input from receiver: may be demodulated NRZ signal or Zero-IF. Quadrature limited signal.
V_{SSA}	21	S	ground signal reference (for the analog parts) (connected to substrate)
P0.5 to P0.7	22 to 24	I/O	**Port 0:** Port 0 is a bidirectional I/O port with internal pull-ups (option 1R, 1R, 1S, see Section 6.6.3). Port 0 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during OTP programming verification.
P1.0 to P1.2	25 to 27	I/O	**Port 1:** Port 1 is an 8-bit quasi bidirectional I/O port with internal pull-ups. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current because of the internal pull-ups. (See Chapter 10: I_{pu}). P1.0 to P1.2 have external interrupts INT2 (X3) to INT4 (X5) assigned.
P1.3	28	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.3 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.3. This I/O then becomes the RXD/data line of the UART.

SYMBOL	PIN	TYPE	DESCRIPTION
P1.4	29	I/O	If the UART is disabled (ENS1 in S1CON.4 = 0) then P1.4 can be used as general purpose P1 port pin. If the UART function is required, then a logic 1 must be written to P1.4. This I/O then becomes the TXD/clock line of the UART. P1.4 has external interrupt INT6 (X6) assigned.
V_{SS}	30	S	ground (connected to substrate)
V_{DD}	31	S	supply voltage for the core logic and most peripheral drivers of the PCA5010 (see V_{DDA})
ALE	32	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory.
$\overline{PSEN}$	33	I/O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated for each code byte fetch.
$\overline{EA}$	34	I/O	**External Access Enable:** $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{EA}$ is held HIGH, the device executes from internal program memory unless the program counter contains an address greater the 7FFFH (32 kbytes).
TCLK	35	I	clock input for use as timing reference in external access mode and emulation
V_{PP}	36	S	Programming voltage (12.5 V) for the OTP. Is connected to V_{SS} in the application.
P1.6	37	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.6 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.6. This I/O then becomes the clock line of the I^2C-bus. P1.6 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
P1.7	38	I/O	If the I^2C-bus is disabled (ENS1 in S1CON.6 = 0) then P1.7 can be used as general purpose P1 port pin. If the I^2C-bus function is required, then a logic 1 must be written to P1.7. This I/O then becomes the data line of the I^2C-bus. P1.7 is equipped with an open-drain output buffer. The pin has no clamp diode to V_{DD}.
XTL2	39	O	output from the current source oscillator amplifier
XTL1	40	I	input to the inverting oscillator amplifier and time reference for pager decoder, real-time clock and timers
V_{BAT}	41	S	Supply terminal from battery. Is used for supplying parts of the chip that need to operate at all times.
$V_{DD(DC)}$	42	O	Supply voltage output of the DC/DC converter. An external capacitor is required.
VIND	43	I	Current input for the DC/DC converter. The booster inductor needs to be connected externally.
$V_{SS(DC)}$	44	S	ground (connected to substrate) OTP
RESETIN	45	I	Schmitt trigger reset input for the PCA5010. External R and C need to be connected to the battery supply. All internal storage elements (except microcontroller RAM) are initialized when this input is activated.

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{\text{RESOUT}}$	46	O	Monitor output for the emulation system. Is active (LOW) whenever a reset is applied to the microcontroller (a reset can be forced by RESETIN, watchdog or wake-up from DC/DC converter in off mode). A reset to the microcontroller initializes all SFRs and port pins; it has no impact on the blocks operating from V_{BAT}.
P3.2 and P3.3	47 and 48	I/O	**Port 3:** P3.2 and P3.3 are configured as push-pull output only (option 3R, see Section 6.6). Using the software input commands or the secondary port function is possible by driving the Port 3 output lines accordingly: P3.2 secondary function: $\overline{\text{INT0}}$ (external interrupt 0) P3.3 secondary function: $\overline{\text{INT1}}$ (external interrupt 1)

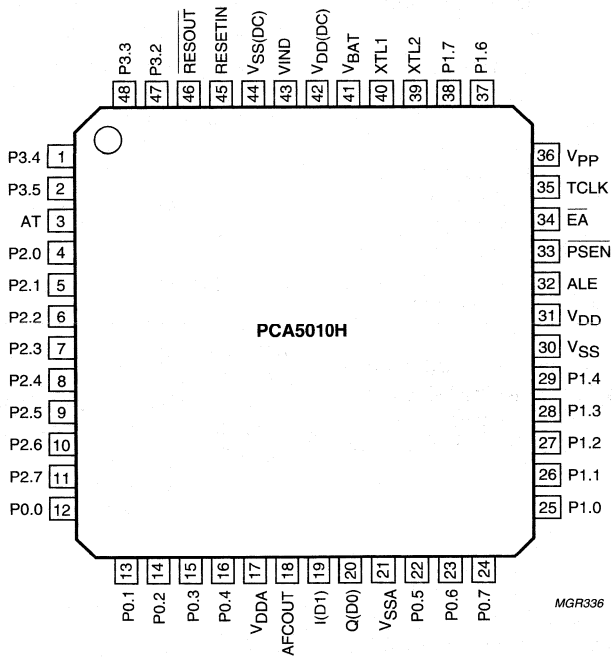


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCA5010 contains a high-performance CMOS microcontroller and the required peripheral circuitry to implement high-speed pagers for the modern paging protocols. For this purpose, features such as FSK demodulator, protocol timer, real-time clock and DC/DC converter have been integrated on-chip.

The microcontroller embedded within the PCA5010 implements the standard 80C51 architecture and supports the complete instruction set of the 80C51 with all addressing modes.

The PCA5010 contains 32 kbytes of OTP program memory; 1.25 kbyte of static read/write data memory, 27 I/O lines, two 16-bit timer/event counters, a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The PCA5010 devices have several software selectable modes of reduced activity for power reduction; Idle for the CPU and standby or off for the DC/DC converter. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The standby mode for the DC/DC converter allows a high efficiency of the latter at low currents and the off mode reduces the supply voltage to the battery level. In the off mode the RAM contents are preserved, real-time clock and protocol timer are operating, but all other chip functions are inoperative.

Two serial interfaces are provided on-chip; a UART serial interface and an I^2C-bus serial interface. The I^2C-bus serial interface has byte oriented master functions allowing communication with a whole family of I^2C-bus compatible slave devices.

6.2 CPU timing

The internal CPU timing of the PCA5010 is completely different to other implementations of this core. The CPU is realized in asynchronous handshaking technology, which results in extremely low power consumption and low EMC noise generation.

6.2.1 Basics

The implementation of the CPU of the PCA5010 as a block in handshake technology has become possible through the TANGRAM tool set, developed in the Philips Natlab in Eindhoven.

TANGRAM is a high level programming language which allows the description of parallel and sequential processes that can be compiled into logic on silicon. The CPU has the following features:

- No clock is needed. Every function within the CPU is self timed and always runs at the maximum speed that a given silicon die under the current operating conditions (supply voltage and temperature) allows.
- The CPU fetches opcodes with maximum speed until a special mode (e.g. Idle) is entered that stops this sequence.
- Only bytes that are required are fetched from the program memory. The dummy read cycles which exist in the standard 80C51 have been omitted to save power.
- To further speed up the execution of a program, the next sequential byte is always fetched from the code memory during the execution of the current command. In the event of jumps the prefetched byte is discarded.
- Since no clocks are required, the operating power consumption is essentially lower compared to conventional architectures and Idle power consumption is reduced to nearly zero (leakage only).
- Clocks are only required as timing references for timers/counters and for generating the timing to the off-chip world.

6.2.2 Execution of programs from internal code memory

When code is executed in internal access mode ($\overline{EA}$ = 1), the opcodes are fetched from the on-chip OTP. The OTP is a self timed block which delivers data at maximum speed. This is the preferred operating mode of the PCA5010.

6.2.3 Execution of programs from external code memory

When code is executed in external access mode ($\overline{EA}$ = 0), the opcodes are fetched from an off-chip memory using the standard signals ALE, $\overline{PSEN}$ and P0, P2 for multiplexed data and address information. In this mode the identical hardware configurations as for a standard 80C51 system can be used, even if the timing for ALE and $\overline{PSEN}$ is slightly different because it is generated from an internal oscillator.

6.3 Overview on the different clocks used within the PCA5010

Figure 3 gives an overview on the clocks available within the PCA5010 for the different functions.

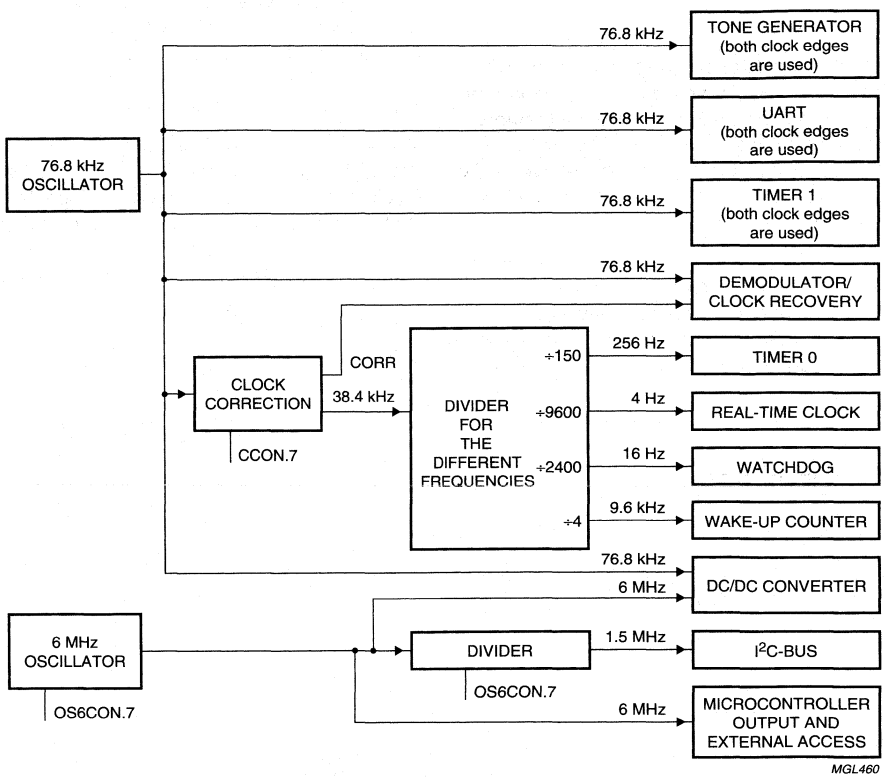


Fig.3 Overview on the clocks used within the PCA5010.

6.4 Memory organization

The PCA5010 has a program memory (OTP) plus data memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory (see Fig.4). If Ports P0 and P2 are not used as I/O signals these pins can be used to address up to 64 kbytes of external program memory. In this case, the CPU generates the latch signal (ALE) for an external address latch and the read strobe ($\overline{PSEN}$) for external Program Memory. External data memory is not supported.

6.4.1 PROGRAM MEMORY

After reset the CPU begins execution of the program memory at location 0000H. The program memory can be implemented in either internal OTP or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then program memory fetches are directed to the internal program memory. If the $\overline{EA}$ pin is strapped to V_{SS}, then program memory fetches are directed to external memory.

Programming the on-chip OTP is detailed in Chapter 15. Usually Philips will deliver programmed parts to a customer. Supply of blank engineering samples is possible, but then Philips cannot give any guarantee on the programmability and retention of the program memory.

6.4.2 DATA MEMORY

The PCA5010 contains 1280 bytes internal RAM (consisting of 256 bytes standard RAM and 1024 bytes AUX-RAM) and Special Function Registers (SFRs). Figure 4 shows the internal data memory space divided into the lower 128 bytes the upper 128 bytes and the SFR space and 1024 bytes auxiliary RAM. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The SFR locations 128 to 255 bytes are only directly addressable and the auxiliary RAM is indirectly addressable as external RAM (MOVX). External Data Memory (EDM) is not supported.

6.4.3 SPECIAL FUNCTION REGISTERS

The second 128 bytes are the address locations of the special function registers. Table 1 shows the special function registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 bit addressable locations in the SFR address space (those SFRs whose addresses are divisible by eight).

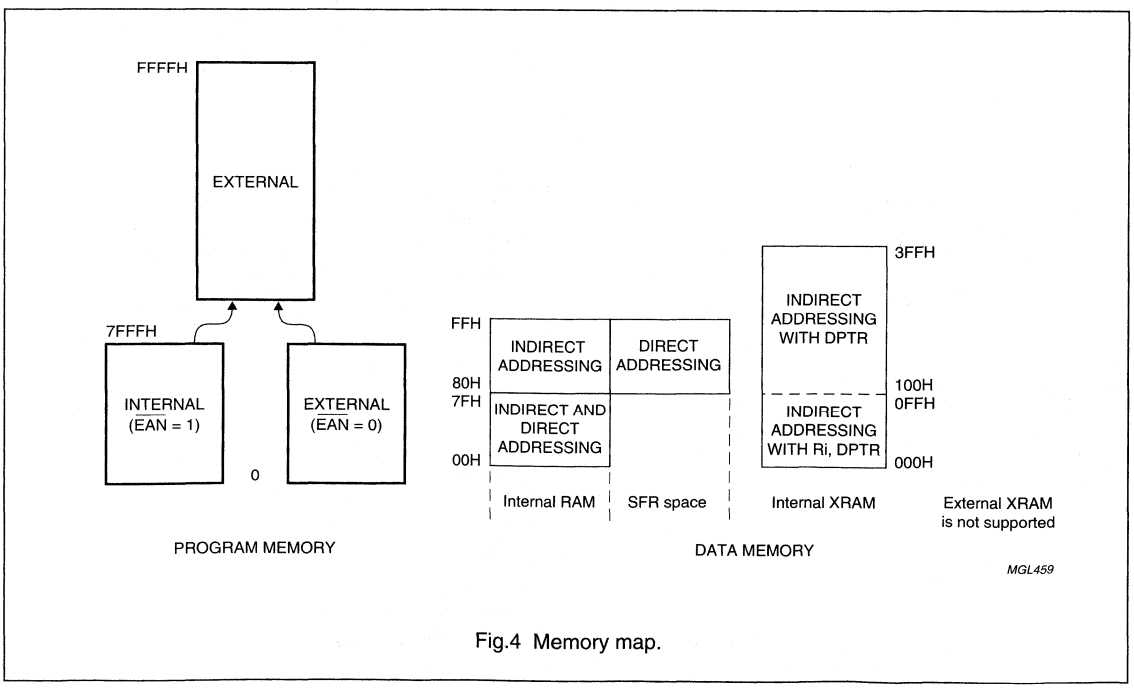


Fig.4 Memory map.

6.5 Addressing

The PCA5010 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register Direct or Register-Indirect
- Maximum 1280 bytes of internal data RAM through Direct or Register-Indirect
  - Bytes 0 to 127 of internal RAM may be addressed directly/indirectly. Bytes 128 to 255 of internal RAM share their address location with the SFRs and so may only be addressed Register-Indirect as data RAM.
  - Bytes 0 to 1024 of AUX-RAM can be addressed indirectly via MOVX. Bytes 256 to 1024 can only be addressed using indirect addressing with the data pointer, while bytes 0 to 255 may be also addressed using R0 or R1.
- Special function registers through Direct
- Program memory Look-Up Tables (LUTs) through Base-Register plus Index-Register-Indirect.

The PCA5010 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFRs), Arithmetic Logic Unit (ALU) and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

While the PCA5010 is executing code from the internal memory, ALE and $\overline{\text{PSEN}}$ pins are inactive with ALE = LOW and $\overline{\text{PSEN}}$ = HIGH.

External XRAM is not supported for this device, since P3.7 ($\overline{\text{RD}}$) and P3.6 ($\overline{\text{WR}}$) pins are not available. If the external XRAM is accessed accidentally, no $\overline{\text{PSEN}}$ or ALE cycle is done and actual P0 values are read. Internal XRAM access is not visible from outside the chip (no ALE, $\overline{\text{PSEN}}$, P0 and P2 activity).

Table 1 Special Function Registers Overview; note 1

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
80	P0									RW	9FH	bit addressable
81	SP									RW	07H	
82	DPL									RW	00H	
83	DPH									RW	00H	
87	PCON	SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL	RW	00H	
88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	RW	00H	bit addressable
89	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	RW	00H	
8A	TL0									RW	00H	
8B	TL1									RW	00H	
8C	TH0									RW	00H	
8D	TH1									RW	00H	
90	P1									RW	FFH	bit addressable
92	TGCON	ENB	CLK2	–	–	–	–	–	–	RW	00H	
93	TG0									RW	00H	
94	WUCON	RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET	RW	00H	see note 2
95	WUC0									RW	00H	see note 2
96	WUC1									RW	00H	see note 2
98	S0CON	SM0	SM1	–	REN	TB8	RB8	TI	RI	RW	00H	bit addressable
99	S0BUF									RW	00H	
9E	AFCON	ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0	RW	00H	
A0	P2									RW	FFH	bit addressable
A5	WDCON	COND	WD3	WD2	WD1	WD0	–	–	LD	RW	00H	
A8	IEN0/IE	EA	EWU	ES1	ES0	ET1	EX1	ET0	EX0	RW	00H	bit addressable
B0	P3									RW	C3H	bit addressable
B8	IP/IP0	–	PWU	PS1	PS0	PT1	PX1	PT0	PX0	RW	00H	bit addressable
C0	IRQ1	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2	RW	00H	bit addressable
CD	RTCON	MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET	RW	00H	see note 2
CE	RTC0									RW	00H	see note 2
D0	PSW	CY	AC	F0	RS1	RS0	OV		P[3]	RW	00H	bit addressable
D1	DCCON0	OFF	SBY	RXE	SBLI	–	–	STB[3]	BLI[3]	RW	03H	
D2	DCCON1	VBG1	VBG0	VLO1	VLO0	–	–	–	–	RW	00H	
D3	OS6CON	ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR	RW	00H	
D4	OS6M0									R	00H	
D8	S1CON	–	ENS1	STA	STO	SI	AA	–	CR0	RW	00H	bit addressable
D9	S1STA	SC4	SC3	SC2	SC1	SC0	0	0	0	R	78H	
DA	S1DAT									RW	00H	
E0	ACC									RW	00H	bit addressable
E8	IEN1	EMIN	EWD	EDC	EX6	ESC	EX4	EX3	EX2	RW	00H	bit addressable
E9	IX1	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2	RW	00H	

ADDR (HEX)	NAME	7	6	5	4	3	2	1	0	R/W	RESET VALUE	COMMENT
EC	DMD0	ENB	M	–	RES	LEV	BD2	BD1	BD0	RW	00H	
ED	DMD1	ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0	R	00H	ENA is RW
EE	DMD2	ENC	–	BF	–	TEST	B2	B1	B0	RW	00H	
EF	DMD3									RW	00H	
F0	B									RW	00H	bit addressable
F8	IP1	PMIN	PWD	PDC	PX6	PSC	PX4	PX3	PX2	RW	00H	bit addressable
FC	CCON	ENB	PLUS	TEST	CIV17	CIV16	–	BYPAS	SET	RW	00H	
FD	CC0	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0	RW	00H	
FE	CC1	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8	RW	00H	

Notes

1. An empty field in this map indicates a bit that can be read or written to by software.
2. Value only reset with RESETIN and not or only partly with an off-restart sequence.
3. This bit cannot be changed by writing to it.

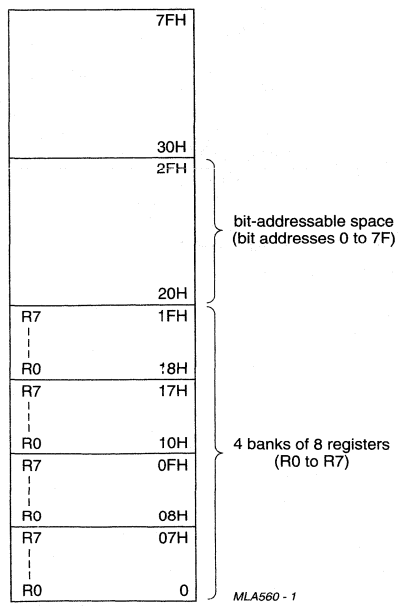


Fig.5 The lower 128 bytes of internal data memory.

6.6 I/O facilities

6.6.1 PORTS

The PCA5010 has 27 I/O lines treated as 27 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0 and 2 are complete, Port 1 has only 7 and Port 3 has only 4 pins externally available. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Is also used for external access, parallel OTP programming mode and emulation (see Table 2 for configuration details):

- Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals
- Provides access to the OTP data I/O lines in OTP parallel programming mode.

Port 1 Used for a number of alternative functions (see Table 3 for configuration details):

- Provides the inputs for the external interrupts INT2/P1.0 to INT4/P1.2 and INT6/P1.4
- SCL/P1.6 and SDA/P1.7 for the I^2C-bus interface are real open-drain outputs; no other port configurations are available
- RXD/P1.3 and TXD/P1.4 for the UART data input and output.

Port 2 Is also used for external access, parallel OTP programming mode and emulation (see Table 4 for configuration details):

- Provides the high-order address bus when expanding the device with external program memory
- Allows control of the on-chip OTP parallel programming mode.

Port 3 Pins are configured as strong push-pull outputs (see Table 5 for configuration details).
The following alternative Port 3 functions are available, but to avoid short-circuiting of the mentioned port pins, the input signals cannot be applied externally to the Port 3 pins. The alternative function can only be stimulated via the respective port output function:

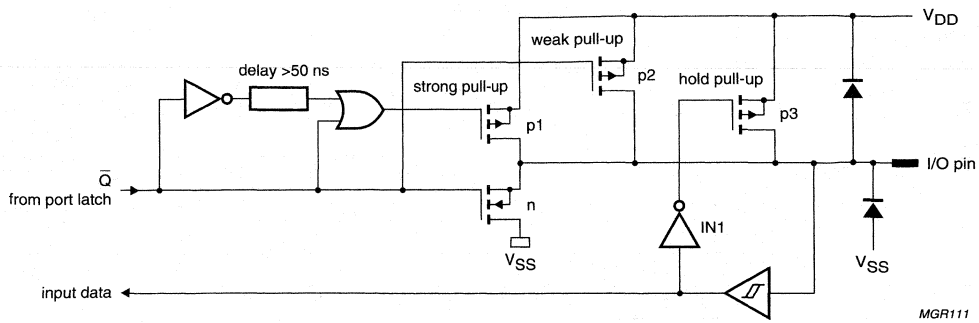
- External interrupt request inputs $\overline{INT0}$/P3.2 and $\overline{INT1}$/P3.3
- Counter inputs T0/P3.4 and T1/P3.5.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

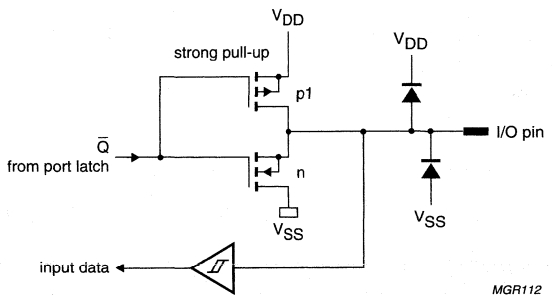
Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Standard ports have internal pull-ups. Figure 6a shows that the strong transistor p1 is turned on for only a short time after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter IN1. This inverter and p3 form a latch which holds the logic 1.

6.6.2 PORT I/O CONFIGURATION (OPTIONS)

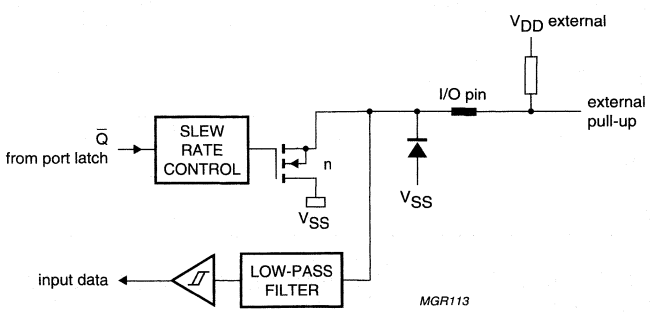
I/O port output configurations are determined on-chip according to one of the options shown in Fig.6. They cannot be changed by software.



a. Standard/quasi-bidirectional (option 1).



b. Push-pull (option 3).



c. Open-drain (only SDA/P1.7, SCL/P1.6) (option 2).

Fig.6 Port configuration options.

6.6.3 PORT I/O CONFIGURATION

Tables 2 to 6 show the hardwired configuration for the different I/Os of the PCA5010.

Table 2 Port 0 configuration; notes 1 and 2

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P0.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_enable (O)
P0.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_enable (O)
P0.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_clock (O)
P0.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (O)
P0.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	SPI_data (I)
P0.5	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	RXE (O)
P0.6	quasi bidirectional I/O (option 1R)	yes	hys	LOW	0.75 mA	ROE (O)
P0.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	bandwidth (O)/RSSI (I)

Notes

1. Option 1S means port configuration option 1 with post-reset state set to HIGH; option 1R means post-reset state will be LOW.
2. 'hys' means input stage with hysteresis.

Table 3 Port 1 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P1.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	Key
P1.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	RXD
P1.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	TXD
P1.5	not available					
P1.6	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SCL
P1.7	I^2C-bus open-drain I/O (option 2S) (slew rate limited)	no	hys	HIGH	2.25 mA	SDA

Table 4 Port 2 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.0	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.1	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.2	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.3	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P2.4	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.5	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.6	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data
P2.7	quasi bidirectional I/O (option 1S)	yes	hys	HIGH	0.75 mA	LCD_Data

Table 5 Port 3 configuration

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
P3.0	not available					
P3.1	not available					
P3.2	push-pull output (option 3R)	no	hys	LOW	3 mA	call LED
P3.3	push-pull output (option 3R)	no	hys	LOW	3 mA	vibrator
P3.4	push-pull output (option 3R)	no	hys	LOW	3 mA	back light
P3.5	push-pull output (option 3R)	no	hys	LOW	3 mA	LCD R/$\overline{W}$/RXD enable
P3.6	not available					
P3.7	not available					

The port configuration is fixed and cannot be reconfigured by software or OTP code.

Table 6 Other pins

PORT PIN	CONFIGURATION	PULL-UP	INPUT	RESET	DRIVE	POSSIBLE APPLICATION IN A PAGER
AT	push-pull output	no		LOW	3 mA	tone generator output
I(D1)	digital input	no	hys			
Q(D0)	digital input	no	hys			
TCLK	digital input	no	hys			
RESETIN	digital input	no	hys			reset input
$\overline{RESOUT}$	push-pull output	no		LOW	1.5 mA	reset output
XTL1	analog input/output (10 pF)	no	hys			to crystal quartz
XTL2	analog input/output (10 pF)	no				to crystal quartz
AFCOUT	analog output	no				
ALE	quasi bidirectional I/O	yes	hys	HIGH	1.5 mA	
$\overline{PSEN}$	quasi bidirectional I/O	yes	hys	HIGH	0.75 mA	
$\overline{EA}$	3-state I/O with bus keeper	hold	buffer	HIGH	0.75 mA	

6.7 Timer/event counters

The PCA5010 contains two 16-bit timer/event counters: Timer 0 and Timer 1 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match
- Generate a Pulse Width Modulated (PWM) output signal.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time interval or event counter.

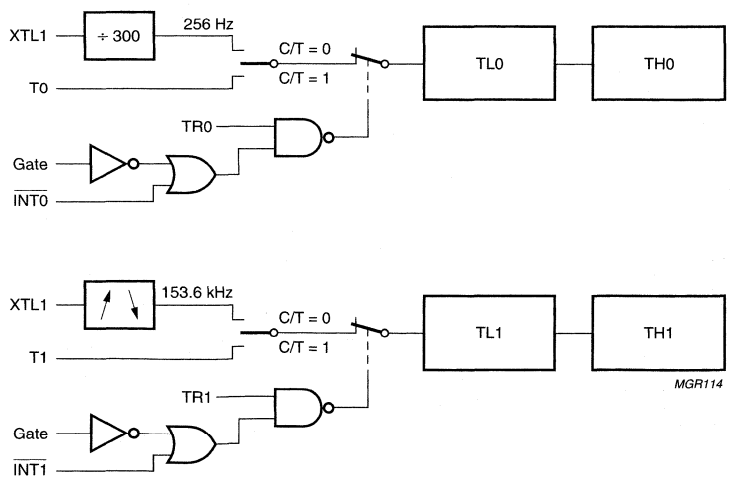
Mode 2 8-bit time interval or event counter with automatic reload upon overflow.

Mode 3 this mode of the standard 80C51 is not available.

In the timer mode the timers count events on the XTL1 input. Timer 0 counts through a prescaler at a rate of 256 Hz and Timer 1 counts directly on both edges of the XTL1 signal at a rate of 153.6 kHz. The nominal frequency of the XTL1 signal is 76.8 kHz.

In the counter mode the register is incremented in response to a HIGH-to-LOW transition at P3.4 (T0) and P3.5 (T1).

Besides the different input frequencies and the non-availability of Mode 3, both Timer 0 and Timer 1 behave exactly identical to the standard 80C51 Timer 0 and Timer 1.



Detailed configuration of the 4 available modes is found in the 80C51 family hardware description (*"Philips Semiconductors IC20 Data Handbook"*).

Fig.7 Timer/counter 0 and 1: clock sources and control logic.

6.8 I²C-bus serial I/O

The serial port supports the 2-line I²C-bus which consists of a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling. The implementation in the PCA5010 operates in single master mode as:

- Master transmitter
- Master receiver.

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register. The block diagram of the I²C-bus serial I/O is shown in Fig.8.

6.8.1 Differences to a standard I²C-bus interface

The I²C-bus interface of the PCA5010 implements the standard for master receiver and transmitter as defined in e.g. P83CL781/782 with the following restrictions:

- The baud rate is fixed to either 100 kHz (CR0 = 0) or 400 kHz (CR0 = 1) derived from the on-chip 6 MHz oscillator. Therefore bits CR1 and CR2 in the S1CON SFR are not available.
- Only single master functions are implemented.
  - Slave address (S1ADR) is not available
  - Status register (S1STA) reports only status defined for the MST/TRX and MST/REC modes
  - Multimaster operation is not supported.

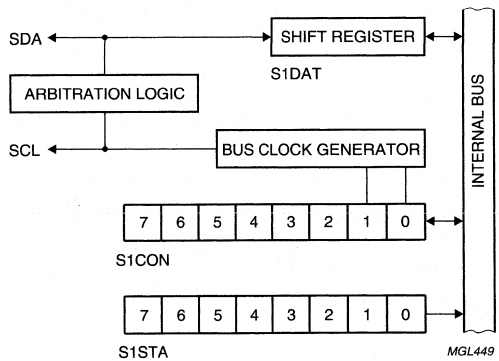


Fig.8 Block diagram of I²C-bus serial I/O.

6.8.2 TIMING

The timing of the I²C-bus interface is based on the internal 6 MHz clock. The phases of this clock divided-by-4 are used as a reference in the 400 kHz mode and divided-by-16 in the 100 kHz mode. In the following context 'T' (333 ns or 1.33 μs) denotes a single phase of this clock.

The transfer of a single bit lasts 9 T. SCL is HIGH for 5 T. When receiving data, the PCA5010 samples the SDA line after 3 T while SCL is HIGH.

The implemented I²C-bus Interface operates according to the timing diagram in Fig.9.

The open-drain I²C-bus outputs are implemented as slew rate controlled driver stages, to minimize the negative impact of I²C-bus activity on the pager sensitivity while the pager is receiving. Typical waveforms on P1.7 (SDA) and P1.6 (SCL) are shown in Fig.10.

Because SDA and SCL are open-drain type I/Os, only the falling edge is determined by the driver characteristics. The static sink current when driving LOW and the slope of the rising edges are determined by the capacitive I²C-bus load and its resistive termination (pull-up to V_{DD}).

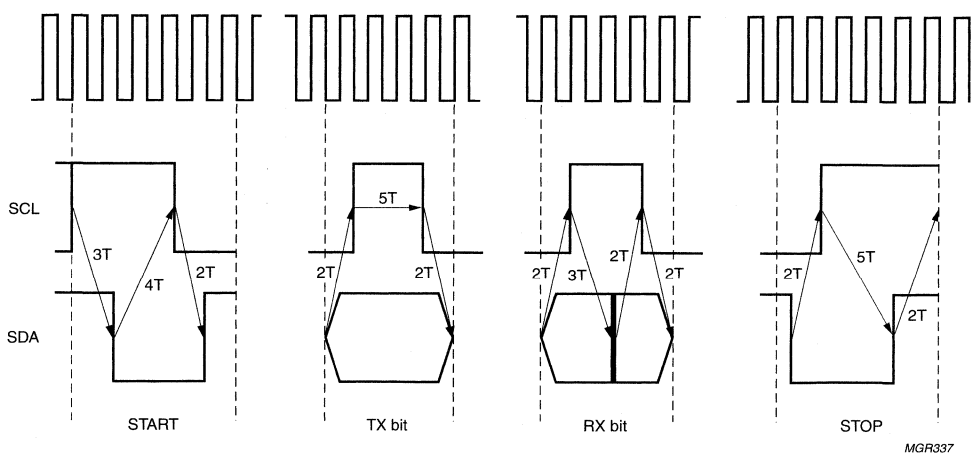
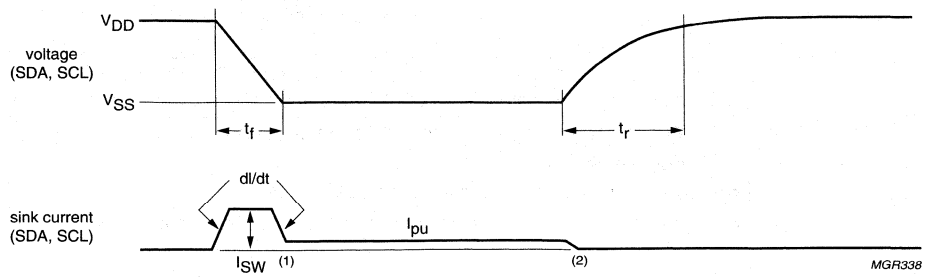


Fig.9 Timing of the I²C-bus interface.



(1) The falling slope depends on the capacitive load. Typical values at 2.2 V where C_L = 50 pF are: t_f = 100 ns; I_{SW} = 2 mA; dI/dt = 250 μA/ns.
(2) The rising slope is defined by external pull-up resistor and capacitive load (a typical t_r is 1 μs at 50 pF/20 kΩ.

Fig.10 Typical waveforms on SDA and SCL.

6.8.3 Serial Control Register (S1CON)

Table 7 Serial Control Register (S1CON, SFR address D8H)

7	6	5	4	3	2	1	0
–	ENS1	STA	STO	SI	AA	–	CR0

Table 8 Description of the S1CON bits

BIT	SYMBOL	FUNCTION
S1CON.7	–	CR2 is not available.
S1CON.6	ENS1	**Enable serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	**START flag**. If STA is set while the SIO is in master mode, SIO will generate a repeated START condition.
S1CON.4	STO	**STOP flag**. With this bit set while in master mode a STOP condition is generated. When a STOP condition is detected on the I²C-bus, the SIO hardware clears the STO flag.
S1CON.3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A START condition is generated in master mode • A data byte has been received or transmitted in master mode (even if arbitration is lost). If this flag is set, the I²C-bus is halted (by pulling down SCL). Received data is only valid until this flag is reset.
S1CON.2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • A data byte is received while the device is programmed to be a master receiver. When this bit is reset, no acknowledge is returned.
S1CON.1	–	CR1 is not available.
S1CON.0	CR0	Speed selection (with on-chip 6 MHz oscillator tuned to 6 MHz the nominal bus frequency is: CR0 = 0 is 83.3 kHz (6 MHz divided-by-72) CR0 = 1 is 333 kHz (6 MHz divided-by-18).

6.8.4 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 9 Data Shift Register (S1DAT, SFR address DAH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.8.5 Address Register (S1ADR)

The slave address register is not available since slave mode is not supported.

6.8.6 Serial Status Register (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus. S1STA is a read-only register. The status codes for all available modes of a single master I^2C-bus interface are given in Tables 12 to 14.

Table 10 Serial Status Register (S1STA and SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 11 Description of the S1STA bits

BIT	SYMBOL	FUNCTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code
S1STA.0 to S1STA.2	–	these 3 bits are held LOW

Table 12 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received

Table 13 MST/REC mode

S1STA VALUE	DESCRIPTION
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned

Table 14 Miscellaneous

S1STA VALUE	DESCRIPTION
78H	no information available (reset value); the serial interrupt flag SI, is not yet set

Table 15 Symbols used in Tables 12 to 14

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit = logic 0)
$\overline{ACK}$	no acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

6.9 Serial interface SIO0: UART

The UART interface of the PCA5010 implements a subset of the complete standard as defined in e.g. the P80CL580.

6.9.1 Differences to the standard 80C51 UART

The following deviations from the standard exist:

- If [SM1 and SM0] = 10 then Mode 1 (8-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- If [SM1 and SM0] = 01 then Mode 2 (9-bit data transmission) is selected, with a fixed baud rate (4800/9600 bits/s)
- Modes 0 and 3 and the variable baud rate selection using Timer 1 overflow is not available
- The SM2 bit has no function
- The time reference for modes 1 and 2 is taken from the 76.8 kHz oscillator, instead of the original $\frac{f_{OSC}}{12}$

6.9.2 UART modes

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte has not been read by the time the reception of the second byte is complete, the second byte will be lost. The serial port receive and transmit registers are both accessed via the special function register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 2 modes:

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a START bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in special function register S0CON (see Figs 11 and 12).

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a STOP bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the STOP bit is ignored (see Figs 11 and 13).

In both modes the baud rate can be selected to either 4800 or 9600 depending on the SMOD bit in the PCON SFR. If SMOD = 0 the baud rate is 4800, if SMOD = 1 the baud rate is 9600 with a 76.8 kHz quartz.

In both modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated by the incoming start bit if REN = 1.

6.9.3 Serial Port Control Register (S0CON)

The serial port control and status register is the special function register S0CON (see Table 16). The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 16 Serial Port Control Register (S0CON, SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	–	REN	TB8	RB8	TI	RI

Table 17 Description of the S0CON bits

BIT	SYMBOL	FUNCTION
S0CON.7	SM0	this bit along with the SM1 bit, is used to select the serial port mode; see Table 18
S0CON.6	SM1	this bit along with the SM0 bit, is used to select the serial port mode; see Table 18
S0CON.5	–	SM2 is not available
S0CON.4	REN	this bit enables serial reception and is set by software to enable reception, and cleared by software to disable reception
S0CON.3	TB8	this bit is the 9th data bit that will be transmitted in Mode 2; set or cleared by software as desired
S0CON.2	RB8	in Mode 2, this bit is the 9th data bit received; in Mode 1 it is the stop bit that was received
S0CON.1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
S0CON.0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2). Must be cleared by software.

Table 18 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	1	1	8-bit UART	$1/16 f_{osc}$ or $1/8 f_{osc}$
1	0	2	9-bit UART	$1/16 f_{osc}$ or $1/8 f_{osc}$

6.9.4 UART DATA REGISTER (S0BUF)

S0BUF contains the serial data to be transmitted or data which has just been received. Bit 0 is transmitted or received first.

Table 19 Data Shift Register (S0BUF, SFR address 99H)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.9.5 BAUD RATES

The baud rate in Modes 1 and 2 depends on the value of the SMOD bit in SFR PCON and may be calculated as:

$$\text{Baud rate} = \frac{2^{SMOD}}{16} \times f_{osc}$$

- If SMOD = 0, (which is the value on reset), the baud rate is $1/16 f_{osc}$
- If SMOD = 1, the baud rate is $1/8 f_{osc}$.

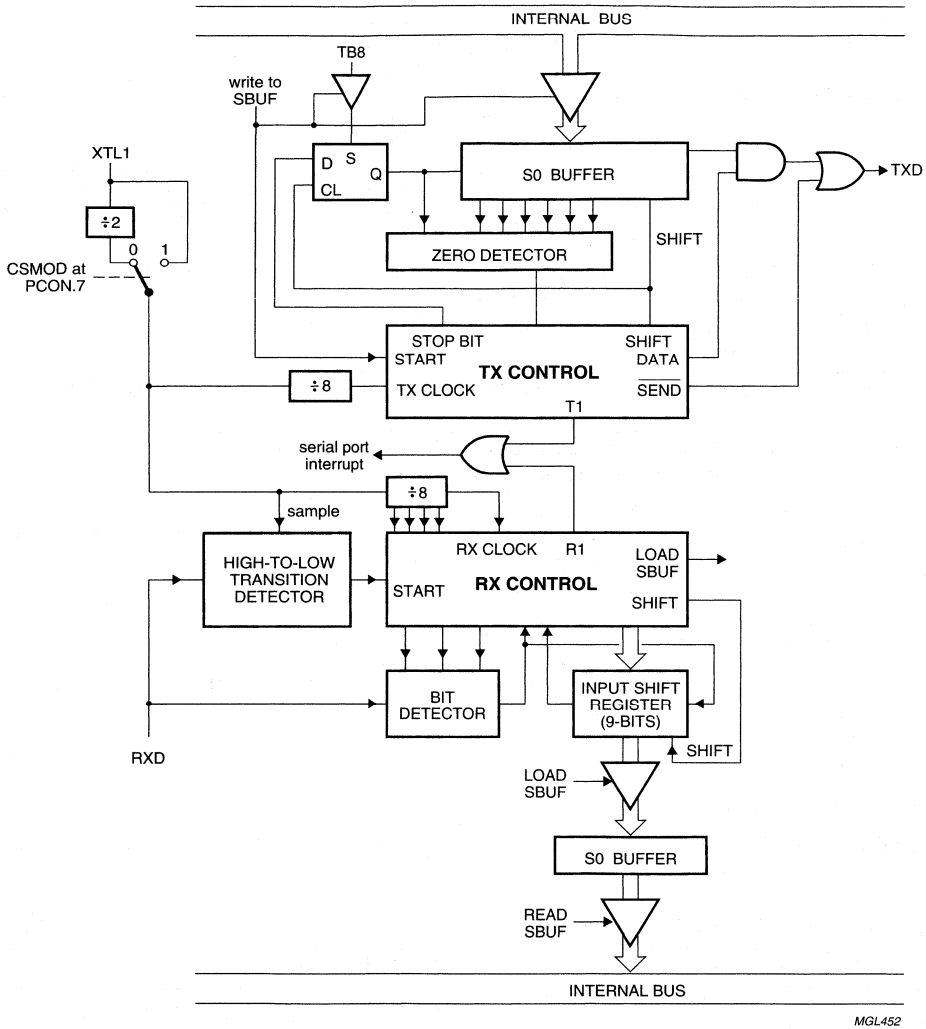


Fig.11 Serial port Mode 1 and Mode 2.

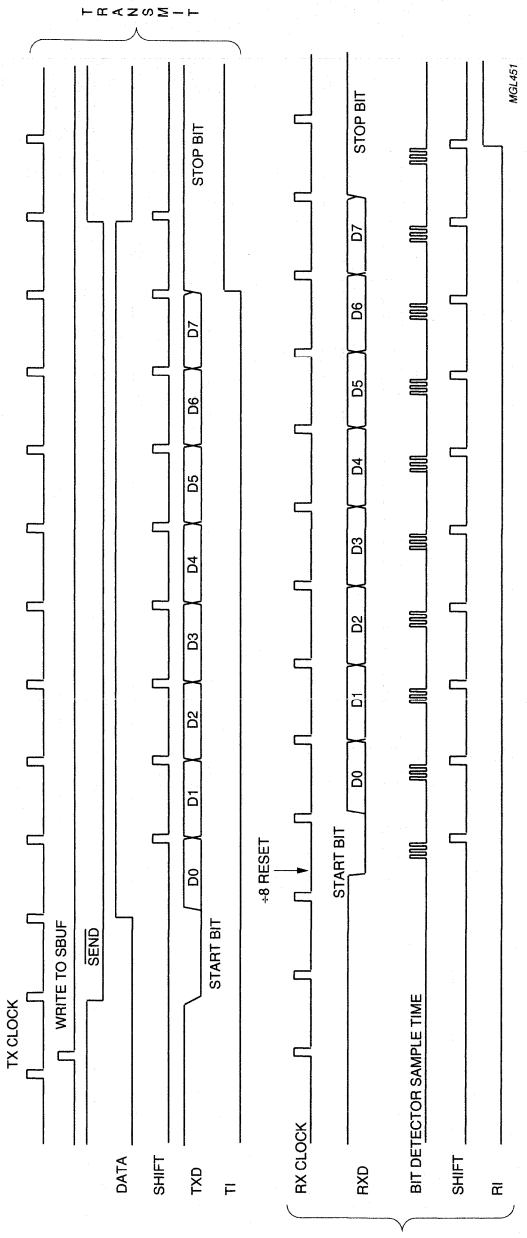


Fig.12 Serial port Mode 1 timing.

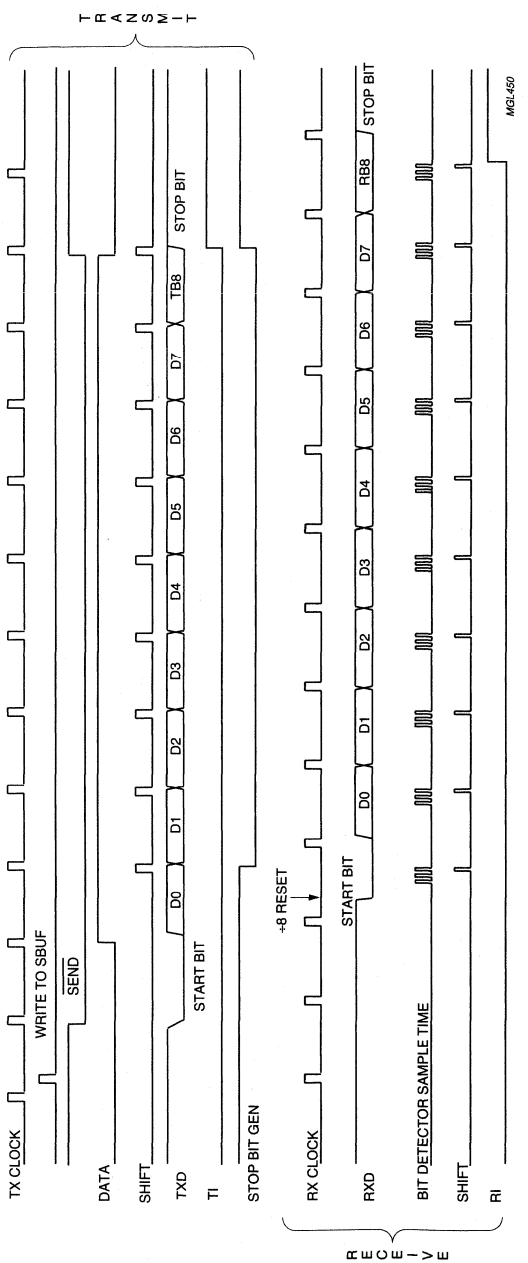


Fig.13 Serial port Mode 2 timing.

6.10 76.8 kHz oscillator

6.10.1 FUNCTION

The oscillator produces a reference frequency of 76.8 kHz. The frequency offset is compensated by a separate digital clock correction block. The oscillator operates directly on V_{BAT} and is always enabled.

6.10.2 OSCILLATOR CIRCUITRY

The on-chip inverting oscillator amplifier is a single NMOS transistor supplied with a constant current. The amplitude visible at terminals XTL1 and XTL2 is therefore not a full rail swing with a very high impedance. To reduce the power consumption, the input Schmitt trigger buffer is limited to approximately 100 kHz maximum frequency. The whole circuit operates directly at the battery supply. The 76.8 kHz oscillator cannot be disabled. It also continues its operation during DC/DC converter off or 80C51 stop mode.

The simplest application configuration is shown in Fig.14a. C1 and C2 can be added to operate a crystal at its optimal load condition. The resulting capacitance of the series connection of C1 and C2 must be smaller than 5 pF for a guaranteed start-up of the oscillator.

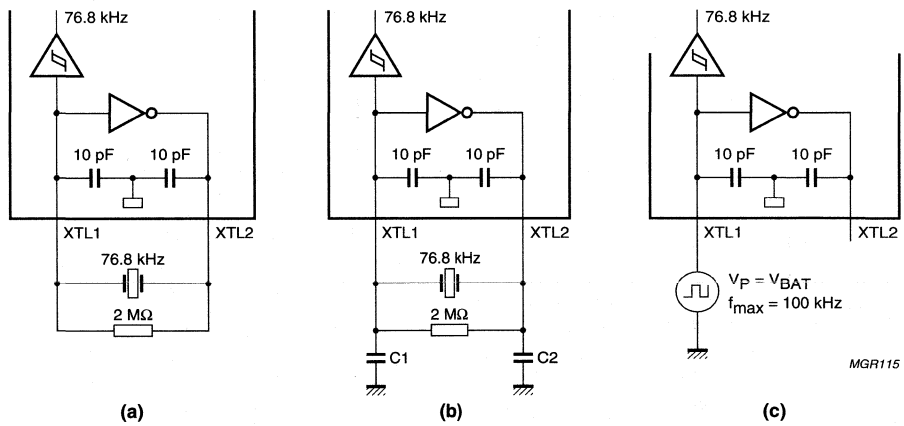


Fig.14 Oscillator circuit.

6.11 Clock correction

6.11.1 FUNCTION

The clock correction block is connected to the 76.8 kHz oscillator. It operates directly on V_{BAT}. By means of the clock correction circuit a digital adjustment of the 76.8 kHz oscillator signal is implemented.

An 18-bit interval counter inserts or deletes one pulse from the 76.8 kHz clock each time its count has expired. The interval is stored by the processor to the 18-bit interval register CIV. Addition/deletion is performed by hardware.

Crystal offset correction can be performed with a resolution of 5 ppm.

This block also generates the timing reference signals for other functional blocks such as the RTC (4 Hz), watchdog (16 Hz), Timer 0 (256 Hz), wake-up counter (9600 Hz) and the demodulator/clock recovery block. The generation of these timing references is always active and cannot be disabled.

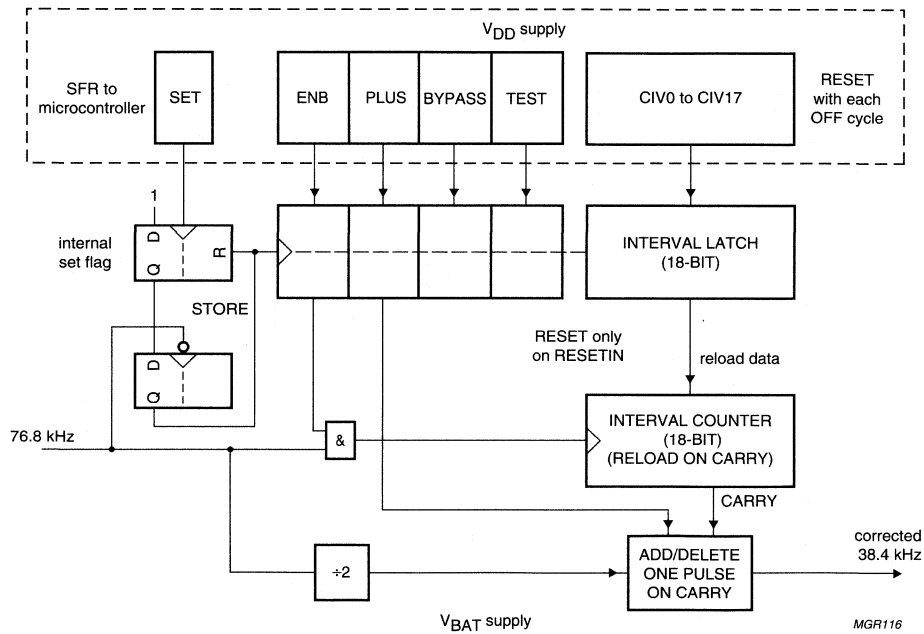


Fig.15 Block diagram of clock compensation.

6.11.2 Clock Correction Control Register (CCON)

The CCON special function register is used to control the clock correction by software.

Table 20 Clock Correction Control Register (CCON, SFR address FCH)

7	6	5	4	3	2	1	0
ENB	PLUS	TEST	CIV17	CIV16	–	BYPASS	SET

Table 21 Description of the CCON bits

BIT	SYMBOL	FUNCTION
CCON.7	ENB	**Enable clock correction**. If ENB = 1 has been set, then correction is enabled and will stay enabled even when the DC/DC converter is shut down and restarted.
CCON.6	PLUS	± **Sign for value**. If PLUS = 1 then clock pulses are inserted, or else deleted.
CCON.5	TEST	**Test signal**, must always be logic 0 in normal mode. It is used during test to bypass the first 9 FFs in the timing generator divider chain. If TEST = 1 the clock rate of the signals 9600 Hz and 256 Hz is doubled and the frequency on 16 Hz and 4 Hz is multiplied by 300.
CCON.4	CIV17	bit 17 of interval value, is used as extension of CC0 and CC1
CCON.3	CIV16	bit 16 of interval value, is used as extension of CC0 and CC1
CCON.2	–	unused.
CCON.1	BYPASS	**Test signal**, must always be logic 0 in normal mode. It is used during test to generate 76.8 kHz on all outputs of the timing generator (4 Hz, 16 Hz, 256 Hz and 9600 Hz).
CCON.0	SET	**A load signal to the interval register**. After a logic 0 to logic 1 transition of this bit the value of ENB, PLUS, TEST, BYPASS and CIV are copied into the local latches with the next 76.8 kHz clock pulse. A duration of one MOV instruction is long enough for the set operation to complete. The SFR values must remain stable for at least one oscillator period because the actual transfer happens synchronized with the local clock (see Figs 16 and 18).

6.11.3 Clock Correction Interval Registers (CC0 and CC1)

The CC0 and CC1 special function registers (together with CCON.3 and CCON.4) are used to define the interval between subsequent clock correction actions.

Table 22 Clock Correction Interval Register (CC0, SFR address FDH)

7	6	5	4	3	2	1	0
CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0

Table 23 Clock Correction Interval Register (CC1, SFR address FEH)

7	6	5	4	3	2	1	0
CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8

6.11.4 Example sequence to set another clock correction interval

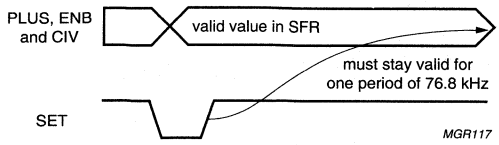


Fig.16 Sequence for setting the clock compensation.

MOV CC0, #(CIV7 to CIV0)

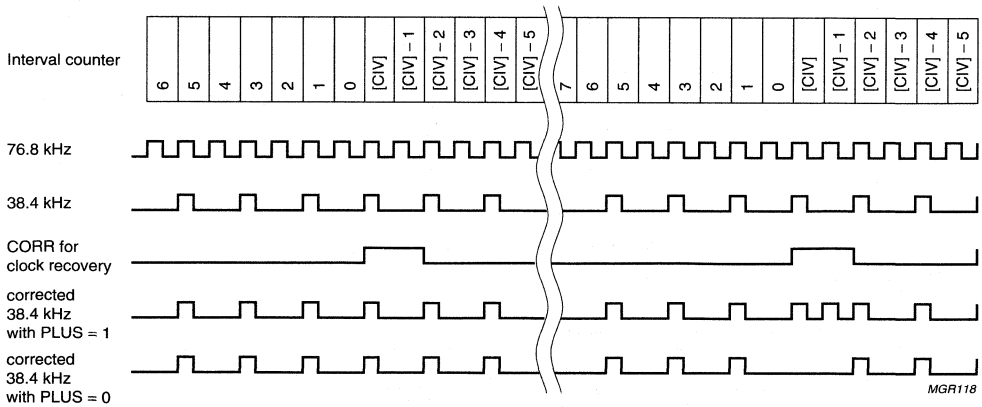
MOV CC1, #(CIV8 to CIV15)

MOV CCON, #D4H

MOV CCON, #D5H.

6.11.5 Timing

Figures 17 and 18 demonstrate how the clock correction works and how the access of the microcontroller is synchronized to the local operation.



After (CIV) clock ticks of 76.8 kHz or 38.4 kHz one correction is made.

Fig.17 Operation of clock compensation.

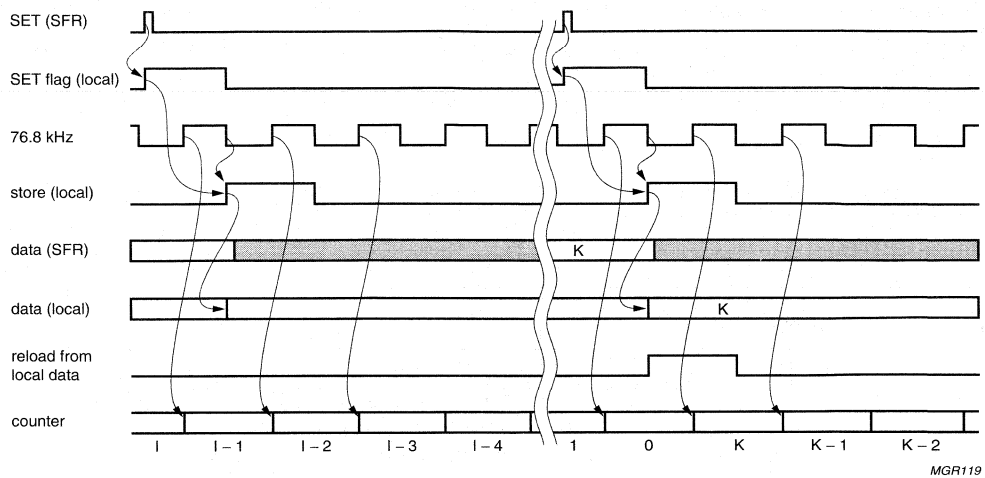


Fig.18 Synchronization of local counter operation and access from the microcontroller.

6.12 6 MHz oscillator

6.12.1 FUNCTION

The 6 MHz oscillator provides the clock for the DC/DC converter, the I²C-bus interface, the port I/Os and for the external memory access timing (ALE/$\overline{\text{PSEN}}$).

The 6 MHz oscillator is a 5 inverter stage current controlled ring oscillator. The oscillator is optimized for low operating current consumption.

The actual frequency of the oscillator can be measured by activating the MFR signal. An 8-bit counter will then be reset and will start counting at the first rising edge of the 76.8 kHz signal and stop counting at the next rising edge of the 76.8 kHz signal. The processor then can read the contents of the MFR counter.

The processor can adjust the oscillator frequency using the F0 to F4 signals (control of source current for ring oscillator).

The 6 MHz oscillator is enabled by hardware only during the start-up phase and whenever the DC/DC converter needs the 6 MHz clock. In all other cases the 6 MHz oscillator is switched of by hardware.

The DC/DC converter does not need the 6 MHz clock when set in standby mode.

If the 6 MHz output is required as a frequency source for other blocks (e.g. I²C-bus) the software needs to enable it explicitly by setting ENB = 1. Besides the DC/DC converter the following functions require the operation of the 6 MHz oscillator:

- I²C-bus block as basic time reference
- Port output logic. Software commands that write to the ports need this clock to complete the operation (if a program 'hangs', this could be the problem).
- Code fetching from external memories needs the clock for the ALE/$\overline{\text{PSEN}}$ timing (e.g. LJMP 5000H needs this clock for completion).

When the ENB bit has been set by software, the clock will be available internally after the start-up time of this oscillator. The start-up time is 2 to 3 periods of the 76.8 kHz reference frequency.

6.12.2 6 MHz Oscillator Control Register (OS6CON)

The OS6CON special function register is used to control the operation of the on-chip 6 MHz oscillator. The 6 MHz oscillator can be controlled as follows:

- It can be enabled or disabled. Disabling this oscillator when the DC/DC converter is in standby mode and no port I/O nor I^2C-bus activity is required saves current.
- The frequency of the oscillator can be adjusted by setting the SFx bits accordingly
- The actual frequency of this oscillator can be measured by writing the MFR bit to logic 1.

Table 24 6 MHz Oscillator Control Register (OS6CON, SFR address D3H)

7	6	5	4	3	2	1	0
ENB	–	$\overline{SF4}$	SF3	SF2	SF1	SF0	MFR

Table 25 Description of the OS6CON bits

BIT	SYMBOL	FUNCTION
OS6CON.7	ENB	**Enable oscillator**. If ENB = 1 then the function is enabled. The enable bit is only cleared when the processor writes the bit to logic 0, or if the DC/DC converter is put into 'OFF' state and a reset is generated during the following power-up sequence.
OS6CON.6	–	unused
OS6CON.5	$\overline{SF4}$	**Set frequency**. This 5-bit value adjusts the current of the ring oscillator and thus the frequency. Writing a small value decreases the frequency. The nominal frequency of 6 MHz is assigned to code ($\overline{SF4}$, SF3, SF2, SF1, SF0) = 00000. The resolution of the frequency adjustment is 200 kHz per step, the range is approximately 3 to 9 MHz. In order to start with the nominal frequency the MSB is inverted in this SFR.
OS6CON.4	SF3	
OS6CON.3	SF2	
OS6CON.2	SF1	
OS6CON.1	SF0	
OS6CON.0	MFR	**Measure frequency**. If a positive pulse is issued on this SFR-bit a frequency measurement cycle is executed. The duration of this cycle is one period of 76.8 kHz. The count of 6 MHz periods during the measurement cycle is reported back in OS6M0. The bit must be reset by software.

6.12.3 6 MHz Oscillator Measured Frequency Register (OS6M0)

The actual frequency of the 6 MHz on-chip oscillator can be calculated from the value in the OS6M0 special function register, after a Measure Frequency operation (MFR).

Table 26 6 MHz Oscillator Measured Frequency Register (OS6M0, SFR address D4H)

7	6	5	4	3	2	1	0
MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0

The value stored in this SFR is the counted number of 6 MHz cycles during one 76.8 kHz period. The frequency of the 6 MHz oscillator is therefore f = MF $\times$ 76800 Hz with a resolution of 76800 Hz.

6.12.4 Enabling of the 6 MHz oscillator

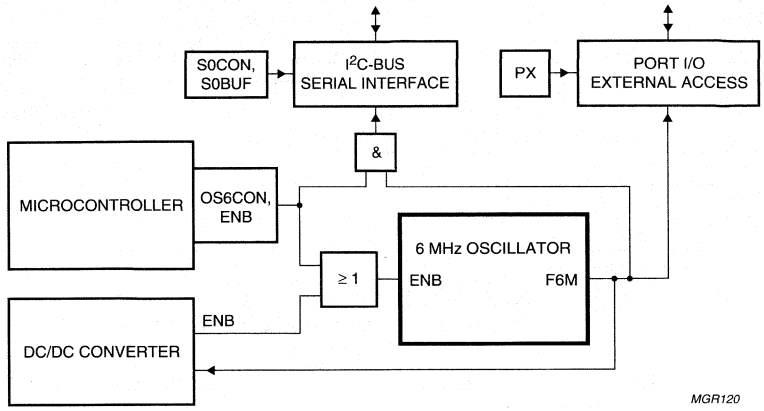


Fig.19 Relationship between 6 MHz oscillator, DC/DC converter and microcontroller.

6.13 Real-time clock

6.13.1 Function

The real-time clock consists of an 8-bit counter that is active at all times. To save power it is operated directly on V_{BAT}. It counts up on every 4 Hz clock pulse (corrected clock).

The RTC can be read from and written to by the processor. When it reaches 239, the signal MINUTE is activated. This signal resets the counter to 0 (at the next clock pulse), and generates an MIN-interrupt for the processor.

The microcontroller 'sees' the minute interrupt as if it was an X9 interrupt. It can be enabled and disabled and must be cleared as an X9 interrupt (CLR IQ9).

If the DC/DC converter is not active when this happens, the DC/DC converter is started first and a power-up/restart sequence of the microcontroller follows. The MIN bit remains set during this procedure.

6.13.2 Real-Time Clock Control Register (RTCON)

The RTCCON special function register is used to control the operation of the on-chip real-time clock function.

Table 27 RTC Control Register (RTCCON, SFR address CDH)

7	6	5	4	3	2	1	0
MIN	–	–	–	–	W/$\overline{R}$	LOAD	SET

Table 28 Description of the RTCON bits

BIT	SYMBOL	FUNCTION
RTCON.7	MIN	**MIN is activated when the counter reaches 239.** MIN is used to generate the interrupt request signal MINUTE. In order to complete the interrupt cycle and reset the interrupt source, the processor has to clear MIN. This must be done in a 2 step operation writing MIN and then applying a positive edge to SET.
RTCON.6	–	unused
RTCON.5	–	unused
RTCON.4	–	unused
RTCON.3	–	unused
RTCON.2	W/$\overline{R}$	Before the RTC time can be set by software, the updating of the SFR by the RTC must be disabled. This is done by writing the W/$\overline{R}$ bit to logic 1. The W/$\overline{R}$ bit is cleared by hardware after the next 4 Hz clock, when the RTC has been loaded with its next value.
RTCON.1	LOAD	**Load RTC with contents of RTC0.** LOAD is sampled with the positive edge of the set flag SET. If LOAD is not HIGH during a SET operation, only the MIN flag is (re)set by the command.
RTCON.0	SET	**Latch signal for the real-time clock.** With the pulse on SET the content of MIN is copied into the 'real' MIN latch. This is necessary because the RTC has to be active at all times independant of the microcontroller.

6.13.3 Real-Time Clock Data Register (RTC0)

Table 29 RTC Data Register (RTC0, SFR address CEH)

7	6	5	4	3	2	1	0
QSECS7	QSECS6	QSECS5	QSECS4	QSECS3	QSECS2	QSECS1	QSECS0

The value stored in this SFR is the actual 4 Hz count since the last MINUTE interrupt. The contents of this counter can be read from and written to by software. The contents of this counter are only initialized when RESETIN is activated. During an OFF sequence, the RTC continues its operation.

The value of the RTC data register is only updated while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is logic 0 the real-time clock continues its operation, the MINUTE interrupt occurs regularly, but the SFR is not updated.

6.13.4 Example sequence for programming the RTC:

Sequence to set another value into the RTC:

MOV RTCON, #06H; set LOAD, W/$\overline{R}$ bits

MOV RTC0, #(new value); load new RTC value into SFR

MOV RTCON, #07H; now set the data valid flag (SET) in the SFR.

Sequence to clear an interrupt of the RTC:

CLR IQ9; Interrupt request flag is IQ9

MOV RTCON, #00H; clear also MIN flag in the SFR

MOV RTCON, #01H; now set the data valid flag (SET) in the SFR.

6.13.5 Timing

The interface between 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.15).

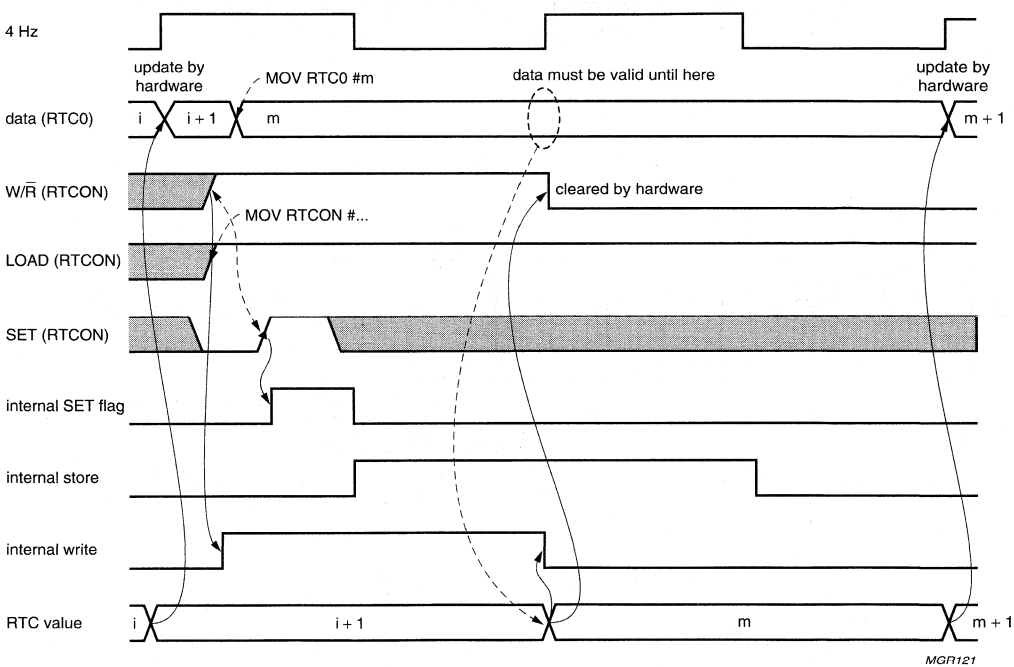


Fig.20 Operation of RTC to microcontroller interface.

6.14 Wake-up counter

6.14.1 FUNCTION

The wake-up counter is intended to be used as protocol timer. It can be programmed to wake-up the processor when the protocol needs an action. Amongst others this may be:

- Switching on the DC/DC converter at time 0
- Enabling the receiver at time 1
- Enabling the demodulator and clock recovery function at time 2 before relevant data is expected.

The time to wake-up is defined as a 16-bit value containing the number of 9600 Hz ticks. The maximum time interval that can be spawn with one cycle then equals 6.8 s.

The wake-up counter and it's reload latch are supplied by V_{BAT} and work independent of the 2 V supply. A reset to the microcontroller does not clear the wake-up counter control flags or the reload latch, but clears the reload register (see Fig.21).

The counter is implemented as a 16-bit ripple down counter. It can be loaded from the wake-up reload latch by a signal from the processor. When the counter is loaded it automatically starts if the RUN signal is active. When the counter reaches zero the wake-up signal becomes active and may generate an interrupt. The wake-up signal automatically reloads the counter (modulo N counter). The counter is stopped when the RUN signal is written to logic 0. Auto reloading of the counter is also possible, when the DC/DC converter is not operating (i.e. V_{DD} is below 1.8 V).

The contents of the wake-up counter cannot be read by the processor. Reading WUC0 and WUC1 reflects the contents of the 16-bit wake-up register (set by the microcontroller).

The interface between 2 and 1 V regions is implemented similar to the clock correction block. The sequence for writing values is identical (see Fig.16).

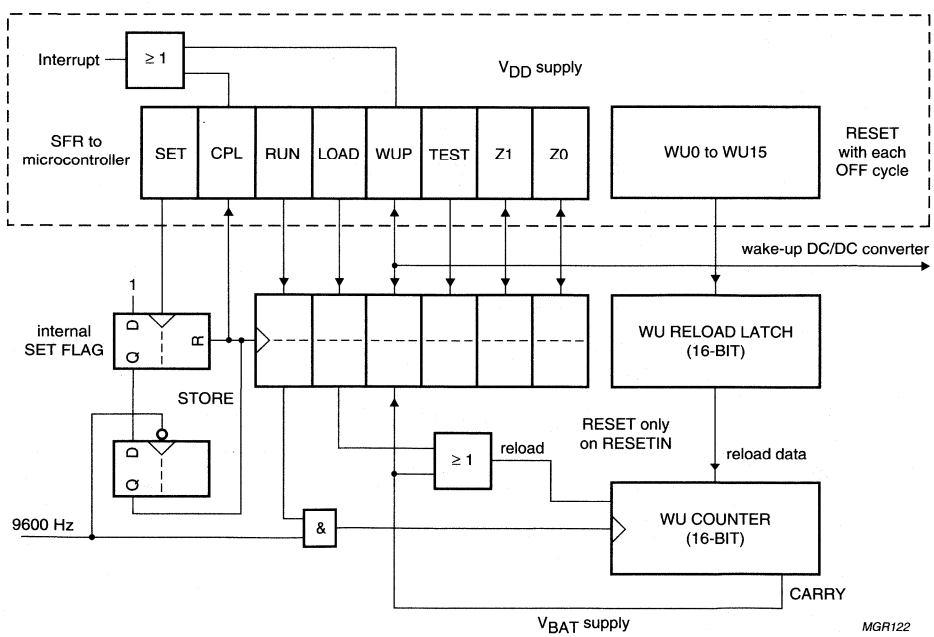


Fig.21 Block diagram of wake-up counter.

6.14.2 Wake-Up Counter Control Register (WUCON)

The WUCON special function register is used to control the operation of the wake-up counter by software.

Table 30 Wake-up Counter Control Register (WUCON, SFR address 94H)

7	6	5	4	3	2	1	0
RUN	WUP	TEST	CPL	Z1	Z0	LOAD	SET

Table 31 Description of the WUCON bits

BIT	SYMBOL	FUNCTION
WUCON.7	RUN	Control signal from the processor.
WUCON.6	WUP	**Latched wake-up signal**. The bit is set by hardware (or software) and generates a wake-up interrupt if enabled and the DC/DC converter STB-bit is set. The bit needs to be cleared by software (SFR and 1 V bits). A SET sequence is required to clear the flag on the 1 V side. Attention: reading the bit reads the contents of the 'real' wake-up flag on the 1 V side (read/modify/write commands will fail on this bit).
WUCON.5	TEST	**Test control signal**. (uses 76.8 kHz as clock input for high and low counter).
WUCON.4	CPL	**Set operation completed**. Bit set by hardware when the last operation is completed and the SFRs are again ready to accept new settings. The bit generates a wake-up interrupt if enabled. The bit needs to be cleared by software.
WUCON.3	Z1	2 bits that are only reset by a primary RESETIN. The bits can be written to and read from by the software. The bits are not cleared when the DC/DC converter is switched off. Same procedure for setting the bits as WU0 to WU15 (reading these bits returns the 'real' flags on the 1 V side; read/modify/write commands will fail on this bit).
WUCON.2	Z0	
WUCON.1	LOAD	**Load wake-up counter with contents of reload latch** (see Fig.21). Is sampled on the positive edge of SET.
WUCON.0	SET	Clock signal for writing to RUN or wake-up SFR (on 1 V level).

6.14.3 Wake-Up Data Registers (WUC0 and WUC1)

The WUC0 and WUC1 special function registers are used to define the interval to the next wake-up interrupt.

Table 32 Low Wake-Up Register (WUC0, SFR address 95H)

7	6	5	4	3	2	1	0
WU7	WU6	WU5	WU4	WU3	WU2	WU1	WU0

Table 33 High Wake-Up Register (WUC1, SFR address 96H)

7	6	5	4	3	2	1	0
WU15	WU14	WU13	WU12	WU11	WU10	WU9	WU8

WU0 to WU15 is a 16-bit register that is loaded by the processor. The contents of this register will be loaded into a 16-bit reload latch with a positive pulse on SET and into the 16-bit ripple down counter with a positive pulse on LOAD.

The value stored in the wake-up counter cannot be read by software. The contents of this counter are only initialized when RESETIN is activated. During an off sequence the wake-up counter continues its operation.

The wake-up-interrupt can only occur while the STB flag in the DCCON0 SFR is HIGH, i.e. the DC/DC converter is able to sustain the V_{DD} supply voltage. If the STB flag is logic 0 the wake-up counter continues its operation, the wake-up flag is set when expired (and can still be checked by software), but an interrupt is not generated.

6.14.4 Example sequence for controlling the wake-up counter

Sequence to set another reload value:

```
MOV WUC1, #(high VALUE)
MOV WUC0, #(low VALUE)
MOV WUCON, #82H; set RUN and LOAD bit
MOV WUCON, #83H; activate SET flag
MOV PCON, #01H; >>> IDLE, WAIT FOR CPL INTERRUPT.
```

6.14.5 Timing

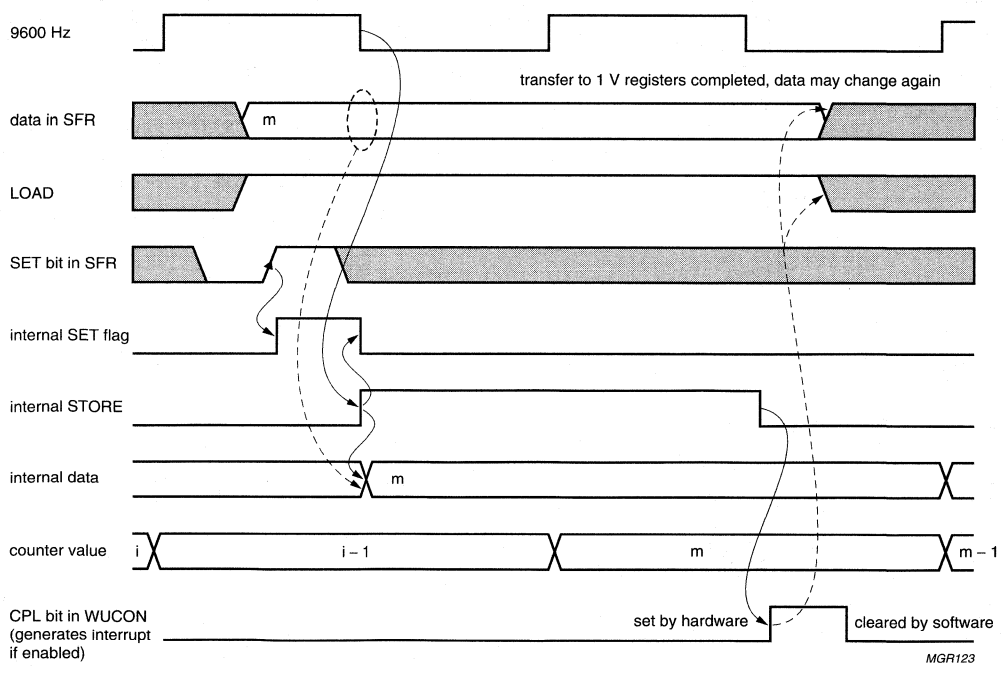


Fig.22 Operation of wake-up counter to microcontroller interface.

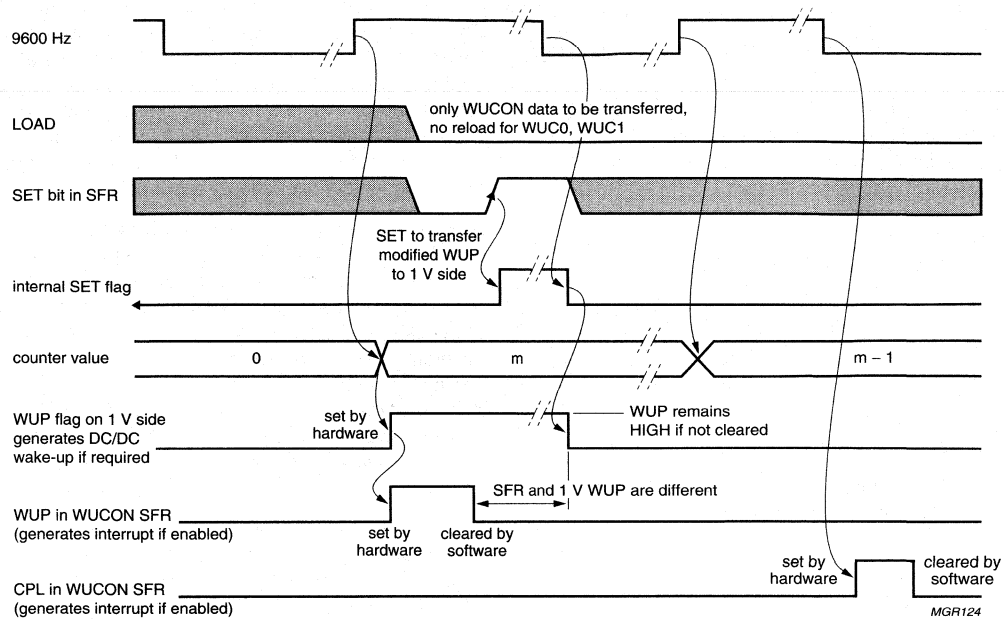


Fig.23 Wake-up interrupt sequence.

6.15 Tone generator

6.15.1 FUNCTION

The tone generator is implemented by a programmable divider from 76.8 kHz. An 8-bit value is used to define the cycle of a modulo N counter. The output of the modulo N counter is divided-by-2 to produce a symmetrical output signal. The counter is running when enabled.

The output frequency at the pin AT is defined as: $f_{AT} = \frac{76.8\ kHz}{TFREQ}$ if TFREQ ≥ 1. If TFREQ = 0 then f_{AT} = 76.8 kHz.

A secondary clock signal can be used as clock input to the modulo N counter. This input is required to generate the accurate resonance frequency of certain acoustic alerters (e.g. 512, 687, 1024, 1365, 2048, 2730 or 4096).

The tone volume can be controlled by setting the frequency on or off alerter resonance.

6.15.2 INTERFACES

SFR ADDR.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TGCON (92H)	ENB	CLK2	–	–	–	–	–	–
TG0 (93H)	TFREQ7	TFREQ6	TFREQ5	TFREQ4	TFREQ3	TFREQ2	TFREQ1	TFREQ0

SFR:

- TFREQ0 to TFREQ7: 8-bit register containing the divisor of the tone. Loaded by the processor.
- ENB: enable frequency generator. Control signal from processor.
- CLK2: use secondary clock input for tone generation. If set a 32768 Hz clock signal is generated from the primary 76800 Hz clock signal and used as a timing reference for the tone generator.

Inputs:

- 76.8 kHz: Input to the tone counter.

Outputs:

- AT Output for alerter. Is logic 0 when disabled:

$$f_{AT} = \frac{76.8\ kHz}{TFREQ}$$

6.15.3 Generation of the 32768 Hz reference

The 32768 Hz reference is generated from 76800 Hz according to the following algorithm:

```
forever do
  begin
    for 10 times do {
      from 7 clocks on 76.8 kHz generate
      3 pulses on 32 kHz
    }
    from 5 clocks on 76.8 kHz generate
    2 pulses on 32 kHz
  end
```

6.16 Watchdog timer

6.16.1 Function

The watchdog timer consists of an 8-bit down counter. The binary number defined with WD3 to WD0 defines the expiration time of the watchdog timer between 1 to 16 s. Once enabled this counter is running continuously. Once expired the timer produces firstly an interrupt and finally a reset. The software must reload the watchdog in regular intervals to avoid expiration.

A positive edge on the LD SFR bit (re)loads the counter with the value of WD3 to WD0, sets the LOW bits to logic 1 and activates this counter if it is not yet running. However, to prepare the (re)loading a positive edge must be applied to the COND bit in WDCON. In this way at least two locations in software must be passed before the counter can be reloaded.
After reset the counter is not running. Only after the first LD it is clocked continuously by a clock pulse of 16 Hz until the DC/DC converter is switched off or an external reset is applied.

If the next LD signal is not given within the defined expiry interval an overflow occurs and the processor will be reset (signal WDR). 1 clock cycle before the reset is applied an WDI interrupt is issued. This gives the opportunity to avoid the reset if required. The maximum watchdog expiry time is thus 254 × 16 Hz ticks to the WD interrupt and 255 × 16 Hz ticks to the reset. If the DC/DC converter is in the off mode, the watchdog timer is suspended.

6.16.2 Watch Dog Timer Control Register (WDCON)

The WDCON special function register is used to control the operation of the on-chip watchdog timer.

Table 34 Watchdog Control Register (WDCON, SFR address A5H)

7	6	5	4	3	2	1	0
COND	WD3	WD2	WD1	WD0	–	–	LD

Table 35 Description of the WDCON bits

BIT	SYMBOL	FUNCTION
WDCON.7	COND	**Load condition**. Control signal from processor.
WDCON.6	WD3	WD0 to WD3 is the preset value for the high nibble of the watchdog timer. The value is the number of seconds to expiry of the watchdog.
WDCON.5	WD2	
WDCON.4	WD1	
WDCON.3	WD0	

BIT	SYMBOL	FUNCTION
WDCON.2	–	unused
WDCON.1	–	unused
WDCON.0	LD	**Load watchdog timer with WD0 to WD3.** Control signal from processor.

6.16.3 SAMPLE SEQUENCE TO RELOAD THE WATCHDOG

The sequence to reload the watchdog with 1 s is:

MOV WDCON, #80H; prepare condition

MOV WDCON, #01H; reload the timer.

6.17 2 or 4-FSK demodulator, filter and clock recovery circuit

6.17.1 FUNCTION

The aim of the blocks demodulator and clock recovery circuitry is to take the signal from the receiver, to format it into symbols and to transfer it to the processor. The two blocks use the 76.8 kHz clock.

The demodulator decodes the incoming signal and generates a sequence of NRZ data. This data is fed to the clock recovery block which regenerates the synchronization clock. This clock is used to sample and to shift the symbols into the register DMD3. Each block is enabled separately. To save power, the functions should be disabled whenever not needed.

6.17.1.1 Demodulator and filter

The demodulator can operate both with 2-level or 4-level FSK input signals (selectable by means of bit LEV). For both types of input signals the so called demodulator, filter and direct modes are allowed. The operation mode is selected on the basis of M bit and BF bit.

In the demodulator mode (M = 0 and BF = X) the I and Q signals are decoded according to Table 36.

Operating in this mode, an offset compensation can be performed and the calculated offset value is stored into register DMD1, in the field AVG. The offset value can be used by the processor to adjust the analog AFC output voltage.

The offset coding is given in Table 37.

The performance of the demodulator for the different baud rates in 2L mode is shown in Fig.24 and for 4L mode in Fig.25. The graphs show the Bit Error Rate (BER) as a function of Eb/No (ratio of signal energy per bit to average noise power per unit bandwidth).

Both the filter and direct modes are intended for application with an external demodulator. In this case NRZ data is fed to the I and Q pins. In the 4-FSK case, the MSB is at pin I and the LSB is at pin Q. In the 2-FSK situation, only the I pin is used while pin Q must be connected to V_{SS}. In these two modes, the offset calculation and compensation cannot be performed.

In the filter mode (M = 1 and BF = 0), the data is filtered and then sent to the clock recovery. The filter characteristics of the implemented filter are shown in Fig.26.

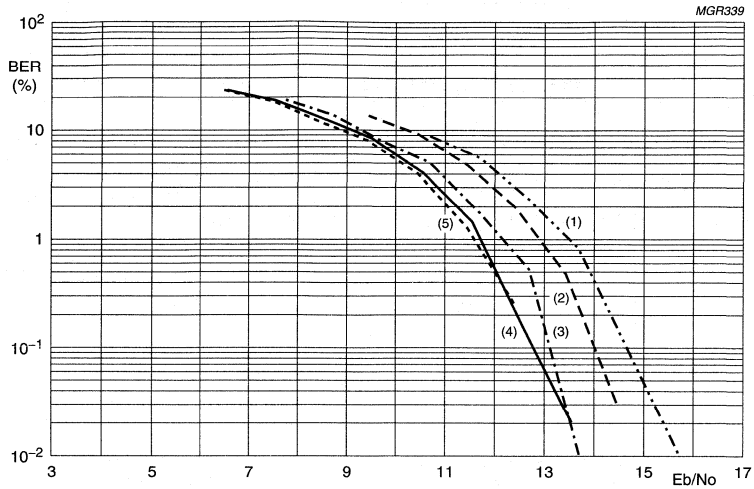
In the direct mode (M = 1 and BF = 1), no function of the demodulator is performed. Consequently there is no filtering on the data which is sent directly to the clock recovery.

Table 36 Modulation coding

FREQUENCY (Hz)	2-FSK		4-FSK	
	D1	D0	D1	D0
+4800	1	X	1	0
+1600	1	X	1	1
−1600	0	X	0	1
−4800	0	X	0	0

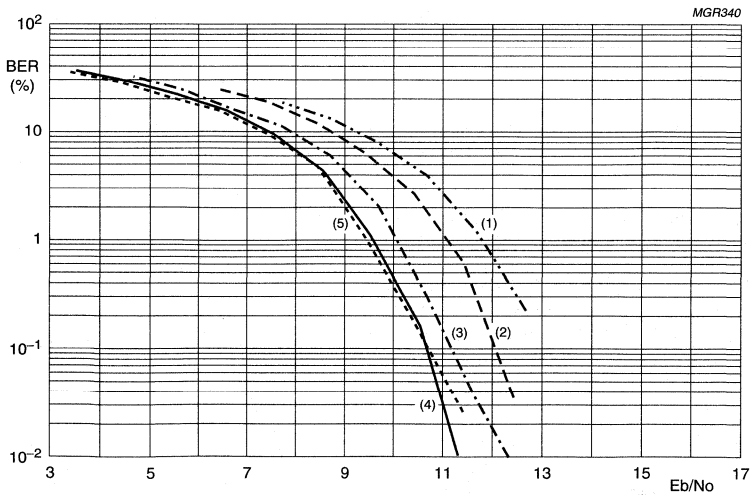
Table 37 Offset coding (2s complement)

OFFSET (Hz)	CODE (AVG6 TO AVG0)
−9450	0111111
−9300	0111110
...	...
−300	0000010
−150	0000001
0	0000000
150	1111111
300	1111110
...	...
9300	1000001
9450	1000000



(1) 2 level 1200.
(2) 2 level 1600.
(3) 2 level 3125.
(4) 2 level 2400.
(5) 2 level 3200.

Fig.24 Demodulator performance in 2L mode.



(1) 4 level 1200.
(2) 4 level 1600.
(3) 4 level 3125.
(4) 4 level 2400.
(5) 4 level 3200.

Fig.25 Demodulator performance in 4L mode.

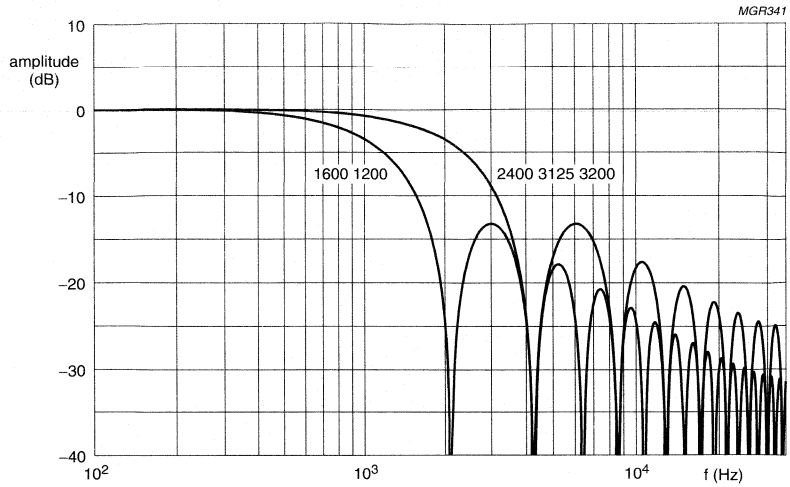


Fig.26 Filter characteristics in direct filter mode.

6.17.1.2 Clock recovery

The clock recovery regenerates the synchronization clock using the edges of the incoming NRZ data. When the NRZ data have no edges for a long time, the synchronization is maintained by means of the correction information from the clock correction block.

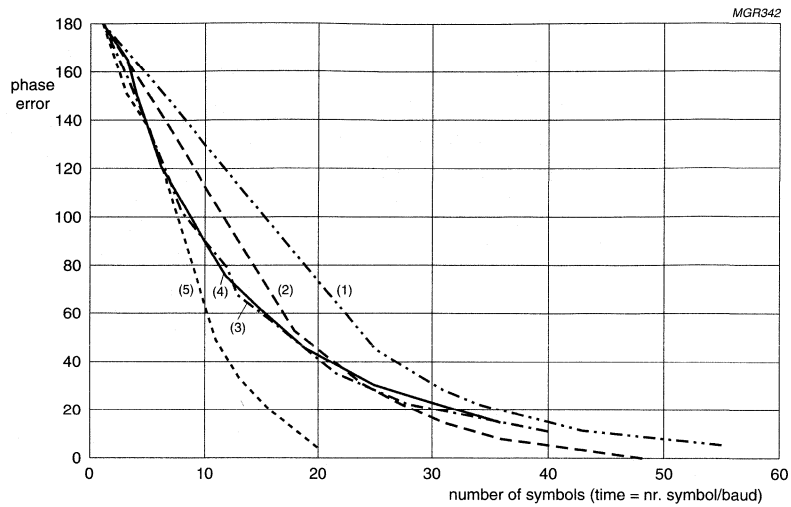
While the clock recovery is disabled, the momentary phase of the recovered clock is frozen. If the clock recovery is enabled at the same relative position within one bit, where it was disabled, then the recovered clock phase will be correct immediately.

The recovered clock is used to sample and shift to left into an internal register one bit each symbol period in 2-FSK and two bits in 4-FSK. The symbol period is determined by bits BD2 to BD0. On the basis of BD bits the demodulator filter length is also set.

In the clock recovery, a pulse (SYMCLK) is generated each n-bits, where n is defined by means of bits B2 to B0. This pulse is used to update the register DMD3. Moreover, it can be used as interrupt to the processor through the IRQ1.3 (symbol interrupt).

The interrupt informs the controller that n bits are available in the register DMD3.

The worst case time required to synchronize to incoming data, when completely out of phase, is plotted for the different baud rates in the following figure (see Fig.27).



(1) 2 level 1200.
(2) 2 level 1600.
(3) 2 level 3125.
(4) 2 level 2400.
(5) 2 level 3200.

Fig.27 Transient phase error due to an input signal phase step of 180 degrees for the different baud rates.

6.17.1.3 Baud rate selection

No bits are lost when switching between single and double baud rates as e.g. required for high speed protocol synchronization. Figure 27 shows how the PCA5010 reacts in this situation.

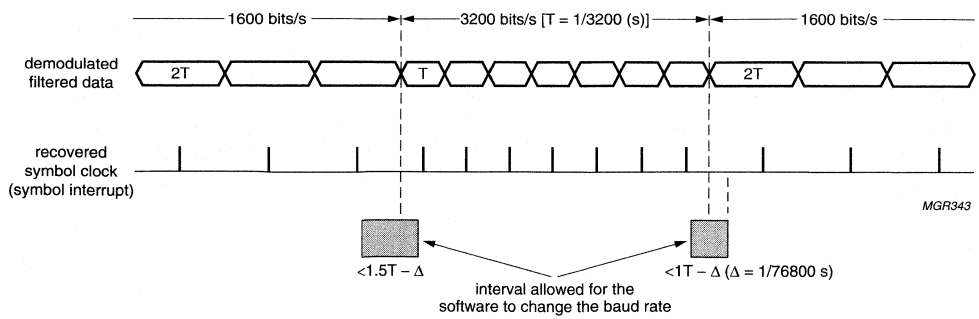


Fig.28 Switching between single and double baud rates (e.g. advanced high speed paging protocol synchronization).

6.17.2 Demodulator Control Register (DMD0)

The demodulator control register DMD0 contains the control bits for enabling the demodulator function and setting its mode and data rate.

Table 38 Demodulator Control Register (DMD0, SFR address ECH)

7	6	5	4	3	2	1	0
ENB	M	–	RES	LEV	BD2	BD1	BD0

Table 39 Description of the DMD0 bits

BIT	SYMBOL	FUNCTION
DMD0.7	ENB	enable demodulator function
DMD0.6	M	mode selection: logic 0 = I/Q from zero-IF receiver, logic 1 = NRZ data
DMD0.5	–	not used
DMD0.4	RES	reserved for future implementation
DMD0.3	LEV	if set to logic 0 2-FSK demodulation, if set to logic 1 4-FSK demodulation
DMD0.2	BD2	baud rate setting; see Table 40
DMD0.1	BD1	
DMD0.0	BD0	

Table 40 Baud rate for bits BD2, BD1 and BD0

BITS			BAUD RATE
BD2	BD1	BD0	
0	0	0	1200 symbols/s
0	0	1	2400 symbols/s
0	1	0	1600 symbols/s
0	1	1	3200 symbols/s
1	0	0	undefined
1	0	1	undefined
1	1	0	undefined
1	1	1	3125 symbols/s

6.17.3 Demodulator averaging Register (DMD1)

The demodulator averaging register DMD1 contains the control bit for enabling the averaging function, used for the offset compensation during demodulation and the coded average (offset) value.

Table 41 Demodulator averaging Register (DMD1, SFR address EDH)

7	6	5	4	3	2	1	0
ENA	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0

Table 42 Description of the DMD1 bits

BIT	SYMBOL	FUNCTION
DMD1.7	ENA	enable averaging function/offset calculation
DMD1.6	AVG6	7-bit value indicating the offset value of the demodulator. This is an indication of the LO offset frequency and will be used to determine the AFC output voltage. For coding see Table 37.
DMD1.5	AVG5	
DMD1.4	AVG4	
DMD1.3	AVG3	
DMD1.2	AVG2	
DMD1.1	AVG1	
DMD1.0	AVG0	

6.17.4 Clock Recovery Control Register (DMD2)

The clock recovery control register DMD2 contains the control bits for enabling the clock recovery function and setting its mode.

Whenever the clock recovery function is enabled (DMD2.7 = 1) the positive edge of the synchronized SYMCLK signal will force a SymClk interrupt through the IRQ1.3 request flag after [B2, B1 and B0] received bits (see Table 50).

Table 43 Clock Recovery Control Register (DMD2, SFR address EEH)

7	6	5	4	3	2	1	0
ENC	–	BF	–	TEST	B2	B1	B0

Table 44 Description of the DMD2 bits

BIT	SYMBOL	FUNCTION
DMD2.7	ENC	enable clock recovery function
DMD2.6	–	not used
DMD2.5	BF	bypass demodulator filter
DMD2.4	–	not used
DMD2.3	TEST	reserved, should always be logic 0
DMD2.2	B2	select number of bits per interrupt:
DMD2.1	B1	If LEV = 0 then 000 = 1-bit, 001 = 2-bit to 111 = 8-bit
DMD2.0	B0	If LEV = 1 then 00X = 2-bit, 01X = 4-bit, 10X = 6-bit, 11X = 8-bit

6.17.5 Demodulator Data Register (DMD3)

The demodulator data register DMD3 contains the (demodulated) recovered received symbols.

Table 45 Demodulator Data Register (DMD3, SFR address EFH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 46 Description of DMD3 bits

BIT	SYMBOL	FUNCTION
DMD3.7	D7	Recovered symbols. The number of relevant bits is set with DMD2[2 to 0].
DMD3.6	D6	
DMD3.5	D5	
DMD3.4	D4	
DMD3.3	D3	
DMD3.2	D2	
DMD3.1	D1	
DMD3.0	D0	

6.18 AFC-DAC

6.18.1 Function

The AFC digital-to-analog converter provides an analog signal to the receiver to reduce its frequency offset. The analog signal is available at pin 18 (AFCOUT).

For low noise sensitivity the DAC output is buffered and can drive a load impedance of 10 kΩ (max.). The output swing is from rail-to-rail V_{DD}. When the enable signal ENB is at logic 1 a linear binary conversion is performed according to Table 47.

Below 0.2 V the linearity of the output voltage is not ideal.

When ENB is logic 0 the AFCOUT pin is tied to V_{SS} and all currents are switched off.

Table 47 Coding of AFC-DAC

CODE	OUTPUT VOLTAGE
000000	0
000001	$1 \times {}^{1}/_{64}V_{DD}$
...	...
N	$N \times {}^{1}/_{64}V_{DD}$
...	...
111111	$63 \times {}^{1}/_{64}V_{DD}$

6.18.2 AFC-DAC Control/Data Register (AFCON)

The AFC-DAC Control/Data register AFCON contains the control bit for enabling the AFC-DAC and the data bits for setting the output voltage.

Table 48 AFC-DAC Control/Data Register (AFCON, SFR address 9EH)

7	6	5	4	3	2	1	0
ENB	–	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0

Table 49 Description of the AFCON bits

BIT	SYMBOL	FUNCTION
AFCON.7	ENB	Enable DAC output.
AFCON.6	–	Not used.
AFCON.5	AFC5	6-bit value for DAC output according to Table 47.
AFCON.4	AFC4	
AFCON.3	AFC3	
AFCON.2	AFC2	
AFCON.1	AFC1	
AFCON.0	AFC0	

6.19 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Fig.34. The PCA5010 acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT4 and INT6
- Timer 0 and Timer 1
- Wake-up counter
- I^2C-bus serial I/O
- UART transmitter and receiver
- Demodulator
- DC/DC converter
- Watchdog timer
- Real-time clock (MINUTE).

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (IEN0 and IEN1).

The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

6.19.1 Overview

The interrupt controller implemented in the PCA5010 has 15 interrupt sources, of which some are level sensitive and some are edge sensitive. The interrupt controller samples all active sources during one instruction cycle. Evaluation of the interrupts is then performed. A priority decoder decides which interrupt is serviced. Each interrupt has its own vector pointing to an 8 bytes long program segment. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt i.e. only two interrupt levels are possible. Between the RETI instruction (Return from Interrupt) and the LCALL to a next interrupt vector at least one instruction of the lower program level is executed (see Fig.29).

An interrupt is performed with a long subroutine call (LCALL) to vector address, which is determined by the respective interrupt. During LCALL the PC is pushed onto the stack. Returning from interrupt with RETI, the PC is popped from the stack.

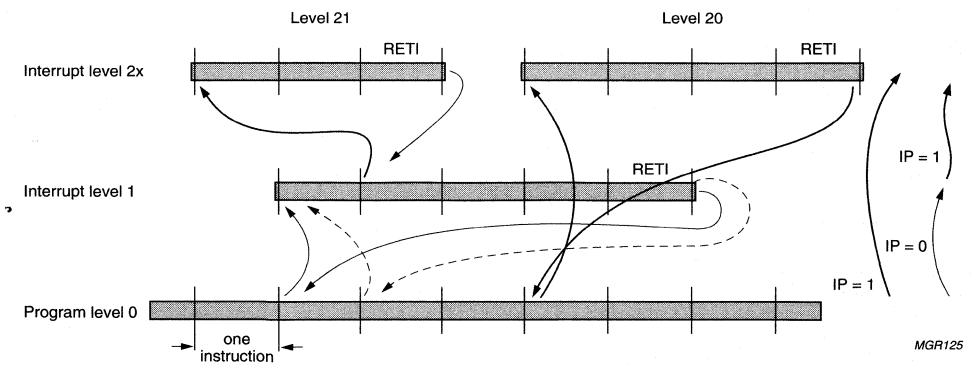


Fig.29 Interrupt hierarchy.

6.19.2 INTERRUPT PROCESS

Sample the interrupt lines: The interrupt lines are latched at the beginning of each instruction cycle.

Analyse the requests: The sampled interrupt lines will be analysed with respect to the relevant Interrupt Enable register (IEx) and Interrupt Priority register (IPx). The process will deliver the vector of the highest interrupt request and the priority information. Depending on the interrupt level and the priority of the interrupt in progress, an interrupt request to the core is performed. The vector address will be passed to the core process.

Interrupt request to core:

Level 0: The interrupt request to the core is performed, when at least one instruction is performed since the RETI from Level 1.

Level 1: The interrupt request is performed, when at least one instruction is performed since the RETI from Level 21 and the request has high priority.

Level 20: No request is performed.

Level 21: No request is performed.

Emulation: In break mode no interrupt request is performed.

Update the interrupt level:

Level 0: In the event of a high priority interrupt the new level will be Level 20. If it is a low priority interrupt, the new level will be Level 1.

Level 1: In the event of a high priority interrupt, the new level will be Level 21. A low priority interrupt is not performed, the level is unchanged. On RETI the new level will be Level 0.

Level 20: On RETI, the new level is Level 0.

Level 21: On RETI, the new level is Level 1.

Level 1: On RETI, the new level is Level 0.

Level 0: The new level is Level 0.

Clearing the flags: During the forced LCALL the interrupt flag of the relevant interrupt is cleared by hardware, if applicable, otherwise by software.

Emulation: During emulation the interrupts may be disabled. This is performed during break mode. With $\overline{INTD}$ asserted, all the interrupts are disabled.

Idle and power-down: When Idle (PCON.0) or power-down (PCON.1) is set, the interrupt controller waits for the according WUI signal. Because the interrupt controller is waiting for WUI, all activity in the circuit will be stopped, thus no handshake can be completed. The WUI signal for Idle is the OR of all the interrupt request bits and the reset. For power-down the WUI signal is built only with the Port 1 interrupt request flags and the reset.

6.19.3 INTERRUPT CONTROLLER RELATED SFRS

The implementation of the interrupt controller related SFRs for enabling and disabling interrupts is identical to a standard 80C51, but the interrupt sources have been changed according to Table 50.

Table 50 Interrupt controller related SFRs: IEN0 (A8H), IEN1 (E8H), IP0 (B8H), IP1 (F8H), IRQ1 (C0H), TCON (88H), WUCON (94H) and RTCON (CDH)

BITS	CONV. NAME	SOURCE	NOTES
IEN0 address A8H: interrupt enable for X0, X1, T0, T1, T2, S0, S1 and global interrupt enable			
0	EX0	P3.2	Enables or disables EXTERNAL0 interrupt. If EX0 = 0, the external interrupt 0 is disabled.
1	ET0	TIMER0	Enables or disables the TIMER 0 overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
2	EX1	P3.3	Enables or disables the EXTERNAL1 interrupt. If EX1 = 0, external interrupt 1 is disabled.
3	ET1	TIMER1	Enables or disables TIMER 1 overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
4	ES0	UART	Enables or disables the UART interrupt. If ES0 = 0, the UART interrupt is disabled.
5	ES1	I^2C	Enables or disables the I^2C-bus interrupt. If ES1 = 0, the I^2C-bus interrupt is disabled.
6	ET2	WAKE-UP	Enables or disables the WAKE-UP interrupt. If ET2 = 0, the WAKE-UP interrupt is disabled.
7	EA	/	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
IEN1 address E8H: interrupt enable for X2 to X9			
0	EX2	P1.0	Enables or disables interrupts on P1.0. If EX2 = 0, the corresponding interrupt is disabled.
1	EX3	P1.1	Enables or disables interrupts on P1.1. If EX3 = 0, the corresponding interrupt is disabled.
2	EX4	P1.2	Enables or disables interrupts on P1.2. If EX4 = 0, the corresponding interrupt is disabled.
3	EX5	SYMBOL	Enables or disables the SYMBOL interrupt. If EX5 = 0, the SYMBOL interrupt is disabled.
4	EX6	P1.4	Enables or disables interrupts on P1.4. If EX6 = 0, the corresponding interrupt is disabled.
5	EX7	DC/DC	Enables or disables the DC/DC converter interrupt. If EX7 = 0, the DC/DC converter interrupt is disabled.
6	EX8	WDI	Enables or disables interrupts on the watchdog. If EX8 = 0, the WDINT interrupt is disabled.
7	EX9	MIN	Enables or disables real-time clock interrupt. If EX9 = 0, the MINUTE interrupt is disabled.
IP0 address B8H: interrupt priority for X0, X1, T0, T1, S0 and S1			
0	PX0	P3.2	Defines the EXTERNAL0 interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.
1	PT0	TIMER0	Enables or disables the TIMER 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
2	PX1	P3.3	Defines the EXTERNAL1 interrupt priority level. PX1 = 1 programs it to the higher priority level.
3	PT1	TIMER1	Defines the TIMER 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.

BITS	CONV. NAME	SOURCE	NOTES
4	PS0	UART	Defines the UART interrupt priority level. PS0 = 1 programs it to the higher priority level.
5	PS1	I^2C	Defines the I^2C-bus interrupt priority level. PS1 = 1 programs it to the higher priority level.
6	PT2	WAKE-UP	Defines the WAKE-UP interrupt priority level. PT2 = 1 programs it to the higher priority level.
7	–	/	Unused.
IP1 address F8H: interrupt priority for X2 to X9			
0	PX2	P1.0	Defines the EXTERNAL2 interrupt priority level 1. PX2 = 1 programs it to the higher priority level.
1	PX3	P1.1	Defines the EXTERNAL3 interrupt priority level 1. PX3 = 1 programs it to the higher priority level.
2	PX4	P1.2	Defines the EXTERNAL4 interrupt priority level 1. PX4 = 1 programs it to the higher priority level.
3	PX5	SYMBOL	Defines the SYMBOL interrupt priority level 1. PX5 = 1 programs it to the higher priority level.
4	PX6	P1.4	Defines the EXTERNAL6 interrupt priority level 1. PX6 = 1 programs it to the higher priority level.
5	PX7	DC/DC	Defines the DC/DC converter interrupt priority level 1. PX7 = 1 programs it to the higher priority level.
6	PX8	WDI	Defines the WATCHDOG interrupt priority level 1. PX8 = 1 programs it to the higher priority level.
7	PX9	MIN	Defines the REAL-TIME CLOCK interrupt priority level 1. PX9 = 1 programs it to the higher priority level.
TCON address 88H: timer/counter mode control register			
0	IT0	P3.2	EXTERNAL0 interrupt type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
1	IE0	P3.2	EXTERNAL0 interrupt flag. Set by hardware when external interrupt detected. Cleared by hardware.
2	IT1	P3.3	EXTERNAL1 interrupt type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
3	IE1	P3.3	EXTERNAL1 interrupt flag. Set by hardware when external interrupt detected. Cleared by hardware.
4	TR0	TIMER0	TIMER 0 run control bit. Set/cleared by software to turn timer on/off.
5	TF0	TIMER0	TIMER 0 overflow flag. Set by hardware on timer/counter overflow. Cleared by hard or software.
6	TR1	TIMER1	TIMER 1 run control bit. Set/cleared by software to turn timer on/off.
7	TF1	TIMER1	TIMER 1 overflow flag. Set by hardware on timer/counter overflow. Cleared by hard or software.
IRQ1 address C0H: interrupt request register for X2 to X9			
0	IQ2	P1.0	Interrupt request flag from P1.0.
1	IQ3	P1.1	Interrupt request flag from P1.1.
2	IQ4	P1.2	Interrupt request flag from P1.2.

BITS	CONV. NAME	SOURCE	NOTES
3	IQ5	SYMBOL	Interrupt request flag from clock recovery circuit. Set by hardware or software. Cleared by software.
4	IQ6	P1.4	Interrupt request flag from P1.4.
5	IQ7	DC/DC	Interrupt request flag from DC/DC-CONVERTER. Set by hardware or software. Cleared by software.
6	IQ8	WDI	Interrupt request flag from watchdog timer. Set by hardware or software. Cleared by software.
7	IQ9	MIN	Interrupt request flag from real-time clock interrupt. Set by hardware or software. Cleared by software.
WUCON address 94H: wake-up counter control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Parallel load signal for wake-up counter.
2	Z0	–	
3	Z1	–	
4	CPL	–	Complete interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
5	unused	–	
6	WUP	–	WUP interrupt flag from wake-up counter timer. Set by hardware or software. Cleared by software.
7	RUN	–	RUN bit for wake-up counter.
RTCON address CDH: real-time clock control register			
0	SET	–	Latch signal to copy content of WUC to peripheral register.
1	LOAD	–	Load RTC0 value from SFR to RTC.
2	W/$\overline{R}$	–	Disable write back to SFR.
3 to 6	unused	–	
7	MIN	–	Interrupt request flag from RTC. Set by hardware or software. Cleared by software.

Notes

1. IEN0 and IEN1: These are two 8-bit registers that control the enabling of the 15 interrupt sources individually as well as a global enable/disable for all of the sources.
2. IP0 and IP1: These are two 8-bit registers that set priority for each interrupt source. IP0 actually contains only 7 bits as IP.7 is not implemented. This bit will always read as logic 0.

6.19.4 PORT 3 INTERRUPTS: P3.2 AND P3.3

INT0 and INT1 are level or edge sensitive.
The programming is performed with TCON. Since P3.2 and P3.3 are configured as push-pull outputs, these interrupts can only be triggered by output commands to these ports and not by external events.

TCON.0 (IT0): Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt (see Fig.30).

TCON.1 (IE0): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

TCON.2 (IT1): Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

TCON.3 (IE1): Interrupt 0 flag. Set by hardware when an external interrupt is detected. Cleared by hardware when the service routine is called.

6.19.5 WAKE-UP INTERRUPT

The wake-up interrupt (T2) is the level sensitive OR-function of WUP bit or CPL bit in the WUCON SFR. The wake-up interrupt is mapped to the T2 vector (see Fig.30). These flags are set by hardware and need to be cleared by software. For more information see Section 6.14.

WUCON.6 (WUP): WUP interrupt flag. Attention: writing and reading this SFR bit does not access the same flag. The flag is set by hardware and needs to be cleared by software.

WUCON.4 (CPL): Complete flag. The previous set instruction is completed. The settings of the SFR have been copied to the peripheral block. The flag is set by hardware and needs to be cleared by software.

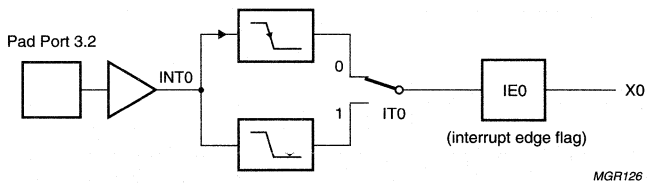


Fig.30 External interrupt Port 3.2 and Port 3.3 (INT0 and INT1).

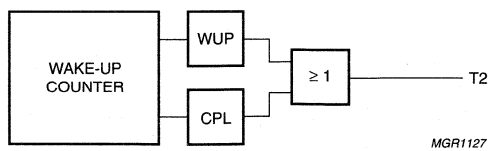


Fig.31 Wake-up interrupt.

6.19.6 PORT 1 INTERRUPTS: PORT 1.0 TO PORT 1.4 (INT2 TO INT6)

Four Port 1 lines can be used as external interrupt inputs (see Fig.30). When enabled (IEN1 SFR), each of these lines may wake-up the device from power-down. Using the IX1 register, each of these port lines may be set active to either HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will send an interrupt request, but must be cleared by software, i.e. via the interrupt software. The Port 1 interrupt request flags can only be set if the corresponding interrupt enable bit is set.

6.19.7 MORE INTERRUPTS: SYMCLK, DC/DC, WATCHDOG AND MINUTE

The decoder blocks generate events that can force an interrupt when enabled (IEN0 and IEN1 SFR). These interrupts are mapped to the corresponding P1 interrupt request flag register bits (see Fig.33). Each flag, if the interrupt is enabled, will send an interrupt request and must be cleared by software, i.e. via the interrupt service routine.

The IRQ bits are not set if the corresponding enable is not set.

IRQ1.3: (symbol interrupt): this interrupt request flag, if enabled, is set if the demodulator (clock recovery) has data ready, that should be read by the microcontroller. The event is called symbol clock or SymClk, because in one mode of operation one symbol is delivered per interrupt. The flag is set by hardware and needs to be cleared by software.

IRQ1.5: (DC/DC converter interrupt); this interrupt request flag, if enabled, is set if the DC/DC converter is not able to deliver the required current (STB flag cleared). The flag is set by hardware and needs to be cleared by software.

IRQ1.6: (watchdog interrupt); this interrupt request flag, if enabled, is set if the watchdog timer will expire within $^1/_{16}$ s. The flag is set by hardware and needs to be cleared by software.

IRQ1.7: (minute interrupt). This interrupt request flag, if enabled, is set each minute once by the real-time clock. The flag is set by hardware and needs to be cleared by software.

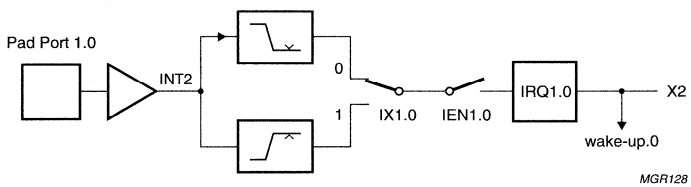


Fig.32 Interrupt Port 1.0.

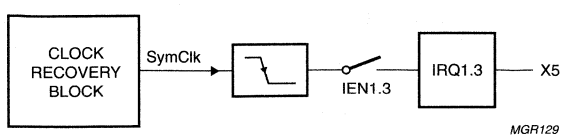


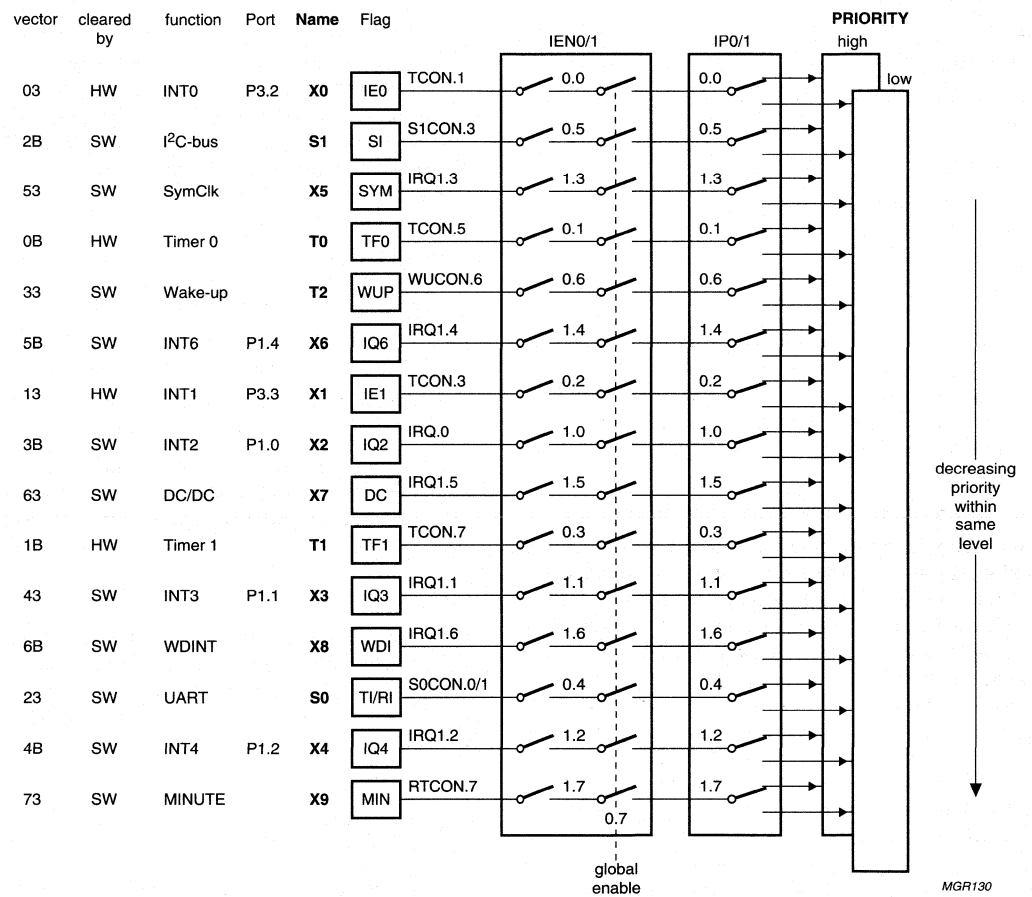
Fig.33 SymClk (as example for any of the 4 mentioned interrupts).

6.19.8 INTERRUPT HANDLING

Figure 34 shows the conventions for interrupt assignments and priorities.

Arbitration of several simultaneously sampled interrupts can be seen from Fig.34. The sampled interrupt with the highest priority will be handled first (assuming that the Interrupt Priority is default).

Setting of interrupt request flags for X2 to X9 is masked by the corresponding interrupt enable bit (IEN1).



Note: The signal level applied to the $\overline{EA}$ pin defines whether the interrupt vector code is fetched from external or internal ROM.

Fig.34 Interrupt assignment and priorities.

6.20 Idle and power-down operation

Idle and power-down are power saving modes of the microcontroller that can be activated when no CPU activity is required. Both modes do not stop the 76.8 kHz oscillator nor disable any peripheral function.

The following functions remain active during the Idle mode:

- Timer 0 and Timer 1
- Wake-up counter
- Watchdog counter
- Real-time clock
- Demodulator and clock recovery
- UART
- I^2C-bus
- External interrupt.

6.20.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 51.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are
   a) Watchdog reset if the watchdog had expired
   b) Off/on reset if the DC/DC converter is restarted from off mode (wake-up counter, RTC or P1 pins).

6.20.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last instruction executed in the normal operating mode before the power-down mode is activated. Once in the power-down mode, the CPU status is preserved together with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during power-down mode. The status of the external pins during power-down mode is shown in Table 51.

There are two ways to terminate the power-down mode:

1. Activation of an enabled external interrupt [INT2 to INT9] will cause PCON.1 to be cleared by hardware thus terminating the power-down mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the power-down mode.
2. The second way of terminating the power-down mode is with an internal or external hardware reset. Reset redefines all SFRs but does not affect the on-chip RAM. Possible sources of an internal reset are
   a) Watchdog reset if the watchdog had expired
   b) Off/on reset if the DC/DC converter is restarted from off mode (wake-up counter or P1 pins).

The power-down mode is not specially useful. It has been implemented for compatibility only. The Idle mode has the same power saving capability and allows much more flexible wake-up.

6.20.3 OFF MODE

The off mode has been designed as the power saving mode of the PCA5010. Shortly after entering this mode the DC/DC converter is switched off and V_{DD} is reduced to V_{BAT}. Directly after activating the off mode, the CPU must be set in Idle mode.

The off mode is entered by:

1. ORL DCCON0, #80H
2. ORL PCON, #01H.

The off mode can be exited by one of the following events:

- RTC minute event
- Wake-up counter event
- Event on any P1 pin
- RESETIN active HIGH.

Each of these events first starts the DC/DC converter to ramp up V_{DD} to 2.2 V. After an initial reset, generated by the DC/DC converter when V_{DD} is again at normal level, all 2 V blocks will restart their operation. The first instruction will be fetched from address 0.

The edge sensitive interrupts (minute and wake-up) from the internal sources have been lost during restart and must be polled from their SFRs. Events from P1 pins can be served after enabling the interrupts, since they are level sensitive.

6.20.4 Status of external pins

The status of the external pins during Idle and power-down mode is shown in Table 51.

Table 51 Status of external pins during normal, Idle and power-down modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Normal	internal	0	1	port data	port data	port data	port data
Idle	internal	1	1	port data	port data	port data	port data
	external	1	1	pull-up HIGH	port data	address	port data
Power-down	internal	0	0	pull-up HIGH	port data	port data	port data
	external	0	0	pull-up HIGH	port data	address	port data

6.20.5 Power Control Register (PCON)

The reduced power modes are activated by software using this special function register. PCON is not bit addressable.

Table 52 Power Control Register (PCON and SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	XRE	ENIS	–	GF1	GF0	PD	IDL

Table 53 Power Control Register (PCON, SFR address 87H)

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Control bit to double data rate of UART, when set to logic 1.
PCON.6	XRE	If set to logic 1 enables external XRAM from address 0 on, if set to logic 0 the first 1024 XRAM bytes are in internal XRAM, the higher addresses come from external XRAM; see note 1.
PCON.5	ENIS	**Enable ISYNC**. If bit is set, ISYNC can be monitored at pin $\overline{EA}$ in internal access mode. The binary value of ISYNC changes each time a new instruction is fetched from memory. This bit must not be set to logic 1 by user program!
PCON.4	–	Reserved.
PCON.3	GF1	**General purpose flag bit**.
PCON.2	GF0	**General purpose flag bit**.
PCON.1	PD	**Power-down bit**. Setting this bit activates the power-down mode; see note 2.
PCON.0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode; see note 2.

Notes

1. This device does not support external XRAM access. Therefore the XRE bit is meaningless and should never be written to logic 1.

2. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (00000000).

6.21 Reset

To initialize the PCA5010 a reset is performed by either of 2 methods:

- Applying an external reset signal to the RESETIN pin
- Via the on-chip watchdog timer.

The reset state of the output pins is given in separate tables (Tables 2 to 6). The reset state of SFRs is given in a separate overview (see Table 1).

While a reset is applied to the device the output $\overline{\text{RESOUT}}$ is driven LOW.

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

6.21.1 External reset using the RESETIN pin

The external reset input for the PCA5010 is the RESETIN pin. A Schmitt trigger is used at the input for noise rejection. Immediately after the RESETIN goes HIGH, an internal reset is executed. As a consequence the SFRs and port pins adopt their reset state, ALE and $\overline{\text{PSEN}}$ are held HIGH. As long as RESETIN pin stays HIGH, the reset state is maintained. When RESETIN goes LOW, the device start-up sequence is executed (see Section 6.22).

6.21.2 External power-on reset using the RESETIN pin

An automatic reset can be obtained by connecting the RESETIN pin to V_{BAT} via a capacitor and to V_{SS} via a resistor. At power-on, the voltage on the RESETIN pin is equal to V_{BAT} and decreases from V_{BAT} as the capacitor charges through the resistor to V_{SS}. $V_{RESETIN}$ must remain higher than the threshold of the Schmitt trigger for a duration of $t_{RESETIN}$ (see Chapter "AC characteristics"). The reset configuration is shown in Fig.35.

6.21.3 Internal Reset

The watchdog which is available in the PCA5010 (see Section 6.16) will force a reset if it is enabled and expires.

A reset is also forced, when the DC/DC converter restarts operation from off mode (see Section 6.22.3).

All resets to the microcontroller can be observed as negative pulses at the output $\overline{\text{RESOUT}}$.

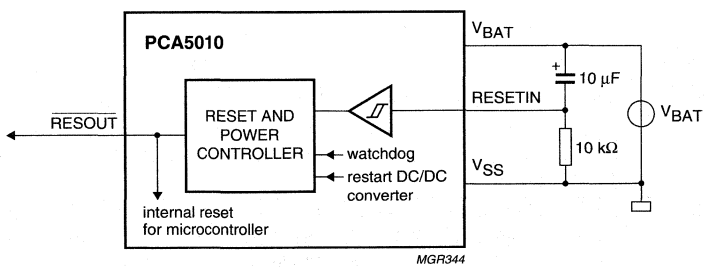


Fig.35 Application diagram for external power-on reset configuration.

6.22 DC/DC converter

6.22.1 FUNCTION

The DC/DC converter converts the voltage from a single primary cell (0.9 to 1.6 V) to a nominal 2.2 V V_{DD} for on-chip and off-chip use. For EMC reasons a special technique is used to minimize coil current ripples under all load conditions.

The voltage generated by the DC/DC converter is available at pin $V_{DD(DC)}$. The supply for all functions of the chip is taken from the V_{DD} and V_{DDA} pins. The user has to connect $V_{DD(DC)}$ to the other V_{DD} pins. The supply used for the reference and comparators is taken from V_{DDA}. A typical circuit configuration is shown in Fig.36.

For a certain current load (I_L) the controller settles to a stable voltage V_{DD} (I_L) in the window 2.15 to 2.25 V. Increasing the load decreases V_{DD} (I_L) by a small amount. When V_{DD} (I_L) drops below 2.15 V the DC/DC converter calculates a new set of coefficients and V_{DD} (I_L) settles again between 2.15 and 2.25 V (see Fig.45).

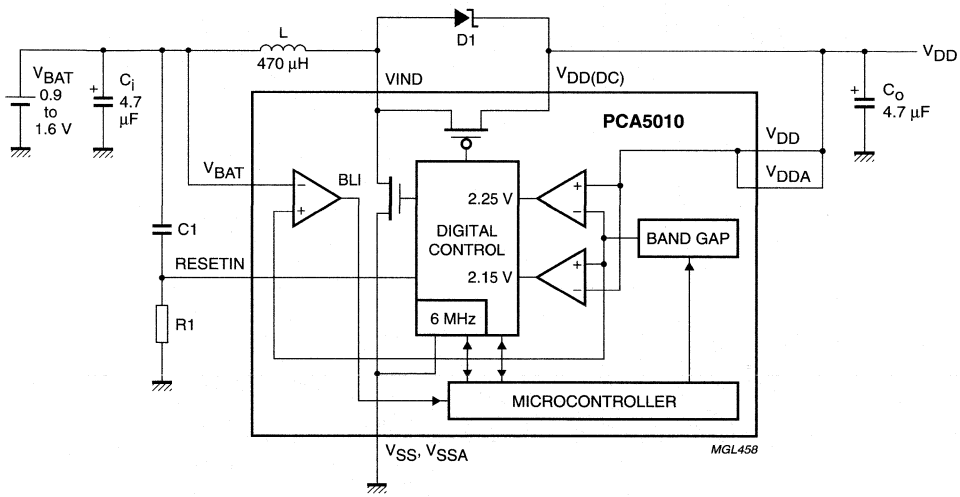


Fig.36 Typical operating circuit.

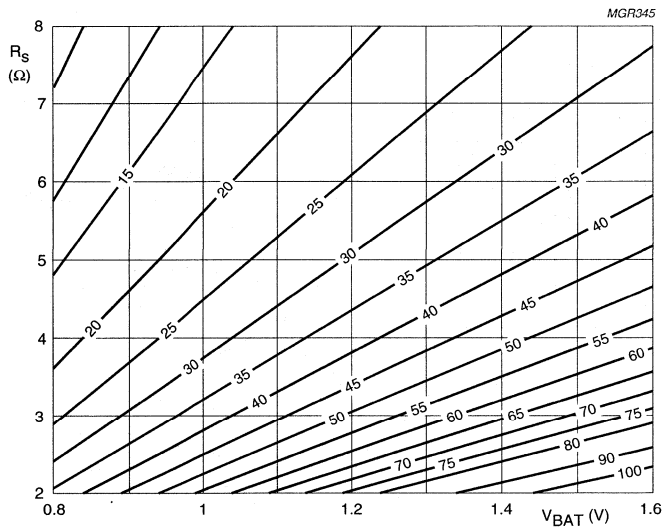
6.22.2 TYPICAL OPERATING CHARACTERISTICS

The maximum power delivered by the DC/DC converter is given by equation (1).

$$P_{o(max)} \leq \frac{(V_{BAT})^2}{4 \cdot R_s} \quad (1)$$

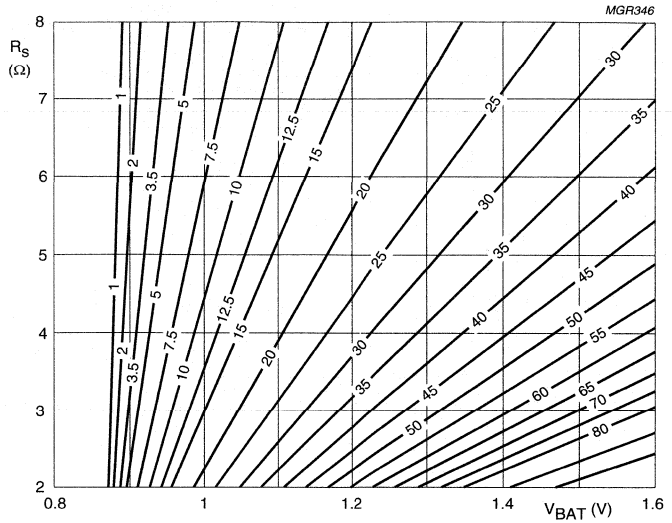
R_s is the total series resistance which is the sum of $R_{BAT} + R_{ind} + R_{sw} + ESR(C_o)$. In Figs 37 and 38 the maximum available output current I_L is shown as a function of V_{BAT} and R_s.

The efficiency is determined by the series resistance R_S and the current consumption of the converter itself. R_S is the sum of the battery resistance R_{BAT}, the DC resistance SRL of the coil, the on resistance of the MOSFET $R_{DS,on}$ and the ESR of the output capacitor C_o. Figure 39a shows the efficiency when using a 470 µH coil with a SRL of 5 Ω and a load capacitor of 4.7 µF with an ESR of 0.5 Ω. In Fig.39b the efficiency for the same configuration is shown but with a SRL of only 0.1 Ω. To increase efficiency for extremely low output currents, the converter should be set into standby mode (see Fig.40).



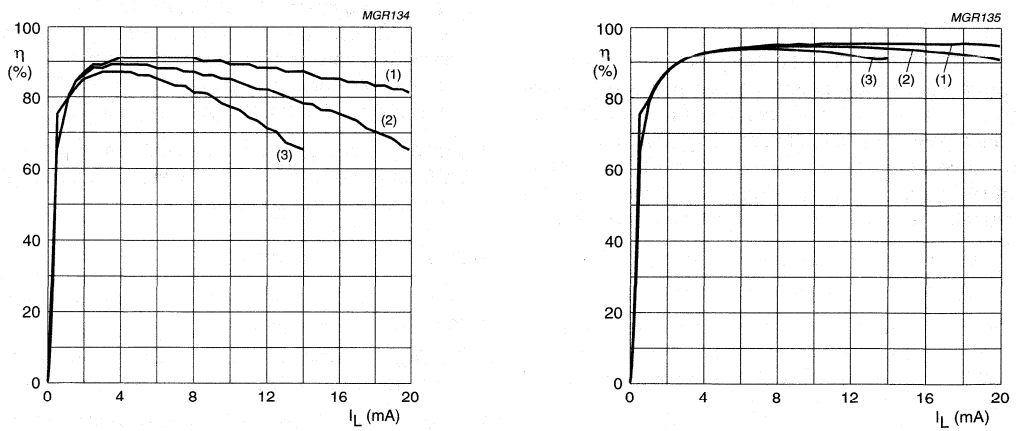
V_{DD} = 2.2 V; $R_S = R_{BAT} + R_{ind} + R_{sw}$.

Fig.37 Maximum available output current (mA) in normal mode.



V_{DD} = 2.2 V; $R_s = R_{BAT} + R_{ind} + R_{sw}$.

Fig.38 Maximum available output current (mA) in standby mode.

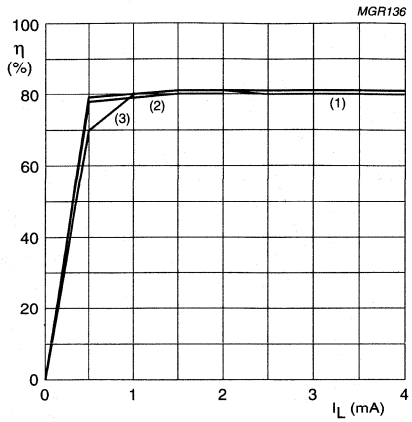


a. R_s = 6 Ω.

b. R_s = 1 Ω.

(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.39 Efficiency in normal mode as a function of load current.



(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 0.9 V.

Fig.40 Efficiency in standby mode as a function of load current.

6.22.3 START-UP DESCRIPTION

6.22.3.1 Start-up from reset

External RC together with an on-chip Schmitt trigger is used to generate a reset pulse after the insertion of a new battery (see Section 6.21). A reset pulse at the RESETIN pin resets the SFRs and the internal registers of the DC/DC converter to the factory programmed values and the start-up sequence shown in Fig.41 is started. The reset pulse must be essentially longer then the rise time of V_{BAT}.

The start-up sequence is divided into several steps:

1. Start-up 76.8 kHz crystal oscillator (256 clocks).
2. Boost up of V_{DD} to approximately 1.7 V using the 76.8 kHz clock. During this phase, the p-channel MOSFET is switched off and the charge is transferred via the external Schottky diode.
3. Start of the 6 MHz clock $\left(2 \times \frac{1}{76.8\ \text{kHz}}\right)$; (see Section 6.12).
4. Boost up V_{DD} to 2.2 V using the internal 6 MHz clock and the p-channel MOSFET. As soon as $V_{DD} \geq 2.15$ V, the stable flag is set to indicate that the system is powered up successfully and the microcontroller starts operation. The DC/DC converter now stays in the normal operating mode.

If a reset pulse is generated during normal operation, the DC/DC converter immediately resets the whole system and enters the start-up sequence.

6.22.3.2 Start-up from off mode

Start-up from off mode behaves exactly as start-up from external reset (see Fig.41) except that:

- The internal registers of the DC/DC converter are not reset; however the DC/DC converter SFRs are reset.

Off mode is exited when one of the following events occur:

- Key pressed
- Minute interrupt
- Wake-up interrupt.

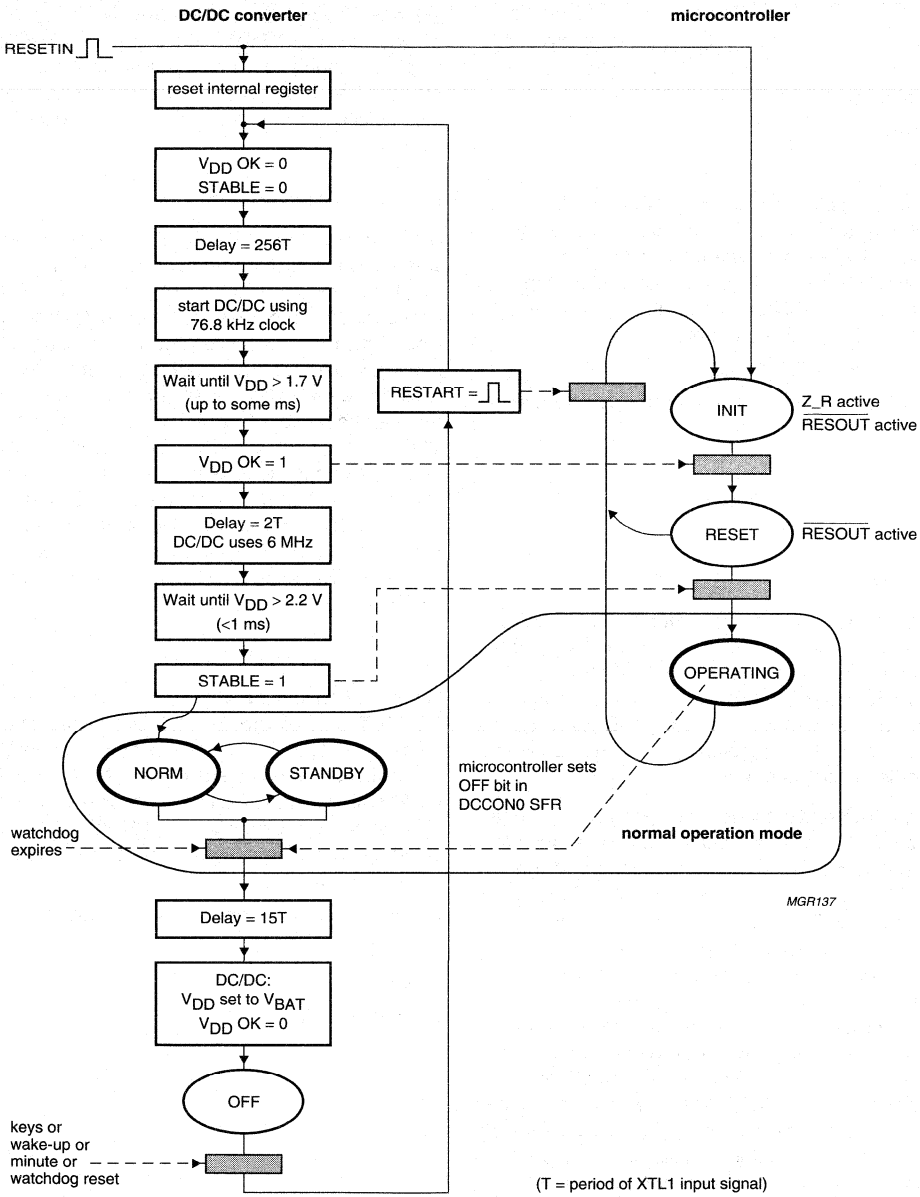


Fig.41 System power-up/off sequencing.

6.22.4 Description of operating modes

6.22.4.1 Normal operating mode

Once the system is powered-up successfully (STB = 1), the DC/DC converter is in normal operating mode. This mode has two sub modes:

- Normal mode
- Standby mode.

By setting/resetting the standby bit in DCCON0 (D1H), the DC/DC converter switches between normal mode and standby mode. Switching between these two modes is possible at any time by software if the controller is in normal operating mode. Normal operating mode can be exited by any of the following events:

- HIGH level at the RESETIN pin
- A watchdog reset, which will force the same sequence as an off command
- Writing the off bit in DCCON0.

Setting the off bit in DCCON0 forces the converter into DC/DC converter off mode.

6.22.4.2 Normal mode

Normal mode is the high efficiency mode of the DC/DC converter. In this mode the controller can keep V_{DD} stable at 2.2 V up to the maximum available current (see Fig.37). The output voltage is regulated in a small window and the current peaks in the coil are kept as small as possible (see Fig.45). After a reset and the following start-up sequence, the controller is in normal mode.

To shorten the settling time when the receiver is switched on or off, the DC/DC converter uses 2 sets of coefficients. One for low output current and one for high output current. When the RXE bit in DCCON0 is set, the DC/DC converter stores the actual coefficients for low output current and switches to the coefficients for high load current. At the same time the receiver should be enabled. When the battery voltage did not change very much since the last time the receiver was on, the settling time is only a few microseconds instead of a few hundreds of microseconds when not using the RXE bit. When switching off the receiver, the RXE bit in DCCON0 should be reset. In this case, the DC/DC converter stores the new values for high output current and restores the values for low output current. It should be noted that the RXE bit does not change the algorithm of the DC/DC converter but shortens the settling time dramatically.

When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. STB = 0 flags the inability to deliver enough current in normal mode or in standby mode. When the STB flag is set to logic 0, V_{DD} can drop very quickly, depending on the battery voltage and the load.

6.22.4.3 Standby mode

Standby mode is a low current mode which can be used when only the microcontroller is running and the quality of V_{DD} is not important. In standby mode the DC/DC converter uses the 76.8 kHz clock instead of the 6 MHz clock. This reduces the current consumption of the DC/DC converter. The maximum output current in this mode is limited to a few milliamps (see Fig.38). In standby mode V_{DD} can be set to 1.9, 2.0, 2.1 or 2.2 V by setting the VLO1 and VLO0 bits in DCCON1 to the corresponding values. When the load is so high that the required output current cannot be delivered, the DC/DC converter resets the signal STB and a DC/DC interrupt is issued to the processor via IRQ SFR IRQ1.5. In this case, the microcontroller should switch off the different loads and switch to normal mode.

6.22.4.4 Off mode

Off mode can only be entered by setting the off bit in DCCON0 by software. The DC/DC converter waits for 15 periods of the 76.8 kHz clock before it sets V_{DD} to V_{BAT} and switches off completely (see Fig.41). In the off mode the PMOS is conducting and therefore it is guaranteed that V_{DD} never drops below V_{BAT} – 100 mV. When the DC/DC converter is in off mode, one of the following events can restart the converter:

- P1X (independent from interrupt enabling or polarity)
- Minute
- Wake-up
- RESETIN pulse.

6.22.5 VOLTAGE/CURRENT RIPPLE

The ripples are determined by V_{BAT}, inductance L, C_o, ESR (Equivalent Series Resistance of C_o, switching frequency and the load current I_L. The ripples are illustrated in Fig.43. If ESR = 0 Ω, then $V_{ripple} = \Delta V$.

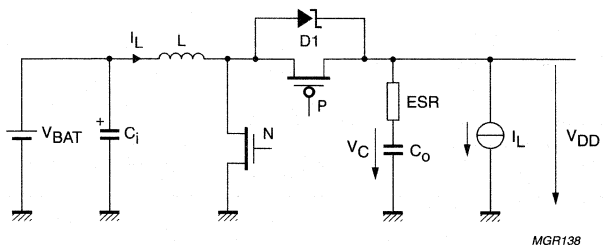


Fig.42 Circuit to analyse ripples.

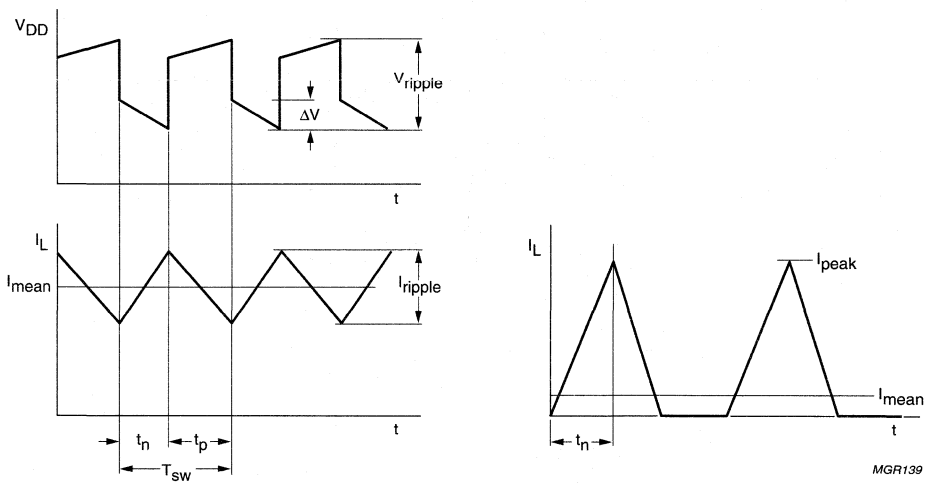


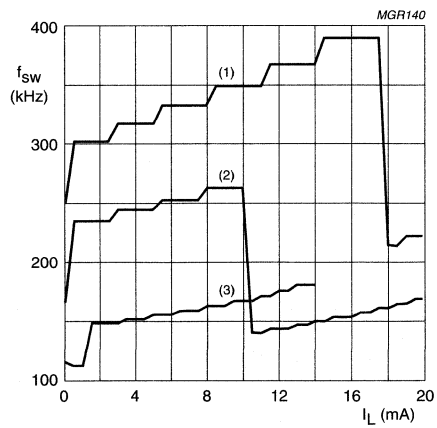
Fig.43 zoom in on the voltage and current ripples.

Table 54 Ripples in normal operation mode

MODE			
STANDBY		**NORM**	
$I_{peak} = V_{BAT} \times \frac{t_n}{L}$	t_n = 6.51 µs	$I_{ripple} = V_{BAT} \times \frac{t_n}{L}$	t_n = 1, 2 or 4 µs
		$I_{Lmean} = \frac{I_L}{D_p}$	$0.2 \leq D_p \leq 0.73$
$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 6.51 µs	$\Delta V = \frac{I_L \times t_n}{C_o}$	t_n = 1, 2 or 4 µs
$V_{ripple} = \frac{V_{BAT} \times t_n}{L} \times ESR$	t_n = 6.51 µs	$V_{ripple} = \left(I_{mean} + \frac{1}{2} \times \frac{V_{BAT} \times t_n}{L}\right) \times ESR$	t_n = 1, 2 or 4 µs

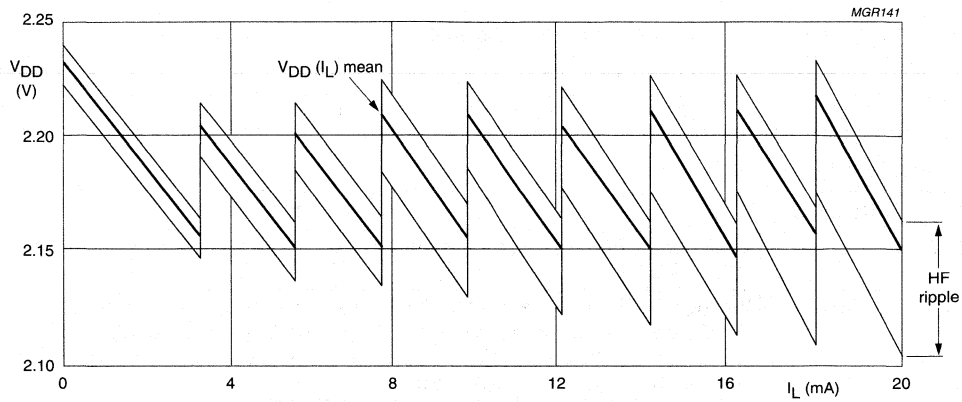
6.22.6 SWITCHING FREQUENCIES

Depending on the load and more importantly on the battery voltage the controller uses different on and off-times for the NMOS and PMOS transistors. This results in different switching frequencies. If the 6 MHz ring oscillator is trimmed to 6 MHz (see Section 6.12) the switching frequency is 120 kHz ≤ f_{sw} ≤ 400 kHz. A typical frequency behaviour is shown in Fig.44.



L = 470 µH, SRL = 5 Ω, C_o = 4.7 µF, ESR = 0.5 Ω.
(1) V_{BAT} = 1.5 V.
(2) V_{BAT} = 1.2 V.
(3) V_{BAT} = 1.0 V.

Fig.44 Switching frequencies.



V_{BAT} = 1.2 V; L = 470 µH; SRL = 5 Ω; C_o = 4.7 µF; ESR = 0.5 Ω.

Fig.45 V_{DD} as a function of load current.

6.22.7 V_{DD} ADJUSTMENT

V_{DD} can be shifted in four steps by adjusting the band gap voltage. The band gap voltage is set with the two bits VBG1 and VBG0 in DCCON1 according to Table 55.

Table 55 V_{DD} adjustment

VBG1	VBG0	OUTPUT VOLTAGE
0	0	V_{DD}
0	1	V_{DD} – 50 mV
1	0	V_{DD} + 50 mV
1	1	V_{DD} + 100 mV

6.22.8 BATTERY LOW MEASUREMENT

Battery low measurement is enabled by setting the SBLI bit in DCCON0. 0.5 ms after setting SBLI to logic 1 the BLI bit in DCCON0 contains the measurement result. When BLI = 0 the battery voltage is below 1.1 V. When BLI = 1 V_{BAT} is above 1.1 V. When SBLI = 1 V_{BAT} is measured continuously. Setting SBLI to logic 0 disables the V_{BAT} comparator and BLI is set to logic 1. After a reset pulse at RESETIN, SBLI is reset to logic 0.

6.22.9 DC/DC Control Register (DCCON0)

The DCCON0 special function register is used to control the operation of the on-chip DC/DC converter.

Table 56 DC/DC Control Register (DCCON0, SFR address D1H)

7	6	5	4	3	2	1	0
OFF	SBY	RXE	SBLI	–	–	STB	BLI

Table 57 Description of the DCCON0 bits

BIT	SYMBOL	FUNCTION
DCCON0.7	OFF	Writing this SFR bit to logic 1 puts the DC/DC converter in the off mode (independent of other control bits).
DCCON0.6	SBY	Writing this SFR bit to logic 1 puts the DC/DC converter in the standby mode, where the DC/DC converter is clocked from the 76.8 kHz oscillator and the ripple voltage will be higher. If the DC/DC converter is unable to deliver enough current in SBY mode, the software has to reset the SBY mode.
DCCON0.5	RXE	Writing this SFR bit to logic 1 uses the stored set of coefficients from a local register to force the DC/DC converter into the state which is appropriate for the required current. The contents of this local register are maintained when the DC/DC converter is set into off state. For the first time after connecting V_{BAT} a set of default coefficients is used. Writing this bit to logic 0 copies the actual coefficients used momentary by the DC/DC converter back to the local register.
DCCON0.4	SBLI	Writing this SFR bit to logic 1 enables the circuitry for measurement of the battery voltage. The new BLI value is valid 0.5 ms later. In order to make a new measurement, the receiver should draw current (continuous mode of DC/DC converter). If SBLI is logic 0 (BLI measurement disabled) BLI will go to HIGH.
DCCON0.3	–	Unused.
DCCON0.2	–	Unused.
DCCON0.1	STB	**Set by the DC/DC converter after power-up**. Reset by DC/DC converter if the converter is not able to deliver the required power. The signal is set in SBY and non SBY mode. This bit is read only.
DCCON0.0	BLI	**Battery low indicator**. Set by DC/DC converter if V_{BAT} < 1100 mV ±50 mV. This bit is read only.

6.22.10 DC/DC Adjust Control Register (DCCON1)

The DCCON1 special function register is used to adjust the exact voltage levels of the on-chip DC/DC converter.

Table 58 DC/DC Adjust Control Register (DCCON1 and SFR address D2H)

7	6	5	4	3	2	1	0
VBG1	VBG0	VLO1	VLO0	–	–	–	–

Table 59 Description of the DCCON1 bits

BIT	SYMBOL	FUNCTION
DCCON1.7	VBG1	**Adjust for band gap voltage**; used to trim the band gap voltage [00] = 1.260 V, [01] = 1.233 V, [10] = 1.286 V, [11] = 1.312 V.
DCCON1.6	VBG0	
DCCON1.5	VLO1	**Adjust for DC/DC converter output voltage in standby mode**; [00] = 1.9 V, [01] = 2.0 V, [10] = 2.1 V, [11] = 2.2 V.
DCCON1.4	VLO0	
DCCON1.3	–	unused
DCCON1.2	–	unused
DCCON1.1	–	unused
DCCON1.0	–	unused

7 INSTRUCTION SET

The PBB family uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes power consumption in Idle and active modes as well as byte efficiency and execution speed. Typical execution times and energy consumption at a V_{DD} of 2.2 V are given in Table 60. **Attention**: for most opcodes the numbers for execution speed and energy are also strongly dependant on the data (ADD, SUBB, DEC, INC, MUL, DIV, DA, conditional jumps etc.) and the operand address (CPU internal SFRs or SFRs in a peripheral block).

Table 60 Instruction set

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [µs]	ENERGY [NJ]	OPCODE (HEX)
Arithmetic operations						
ADD	A,Rn	add register to A	1	0.498	1.831	2*
ADD	A,direct	add direct byte to A	2	0.631	2.501	25
ADD	A,@Ri	add indirect RAM to A	1	0.529	1.990	26, 27
ADD	A,#data	add immediate data to A	2	0.583	2.262	24
ADDC	A,Rn	add register to A with carry flag	1	0.508	1.864	3*
ADDC	A,direct	add direct byte to A with carry flag	2	0.637	2.525	35
ADDC	A,@Ri	add indirect RAM to A with carry flag	1	0.539	2.030	36, 37
ADDC	A,#data	add immediate data to A with carry flag	2	0.597	2.304	34
SUBB	A,Rn	subtract register from A with borrow	1	0.497	1.861	9*
SUBB	A,direct	subtract direct byte from A with borrow	2	0.630	2.527	95
SUBB	A,@Ri	subtract indirect RAM from A with borrow	1	0.528	2.021	96, 97
SUBB	A,#data	subtract immediate data from A with borrow	2	0.582	2.287	94
INC	A	increment A	1	0.459	2.475	04

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
INC	Rn	increment register	1	0.457	1.737	0*
INC	direct	increment direct byte	2	0.586	1.982	05
INC	@Ri	increment indirect RAM	1	0.493	1.982	06, 07
DEC	A	decrement A	1	0.459	1.489	14
DEC	Rn	decrement register	1	0.457	1.74	1*
DEC	direct	decrement direct byte	2	0.590	2.488	15
DEC	@Ri	decrement indirect RAM	1	0.489	1.972	16, 17
INC	DPTR	increment data pointer	1	0.384	1.345	A3
MUL	AB	multiply A and B	1	0.378	1.242	A4
DIV	AB	divide A by B	1	0.733	2.532	84
DA	A	decimal adjust A	1	0.426	1.363	D4
Logic operations						
ANL	A,Rn	AND register to A	1	0.495	1.857	5*
ANL[1]	A,direct	AND direct byte to A	2	0.623	2.494	55
ANL	A,@Ri	AND indirect RAM to A	1	0.525	2.021	56, 57
ANL	A,#data	AND immediate data to A	2	0.583	2.272	54
ANL	direct,A	AND A to direct byte	2	0.650	2.639	52
ANL	direct,#data	AND immediate data to direct byte	3	0.719	3.138	53
ORL	A,Rn	OR register to A	1	0.459	1.605	4*
ORL[1]	A,direct	OR direct byte to A	2	0.584	2.248	45
ORL	A,@Ri	OR indirect RAM to A	1	0.486	1.767	46, 47
ORL	A,#data	OR immediate data to A	2	0.539	2.015	44
ORL	direct,A	OR A to direct byte	2	0.614	2.405	42
ORL	direct,#data	OR immediate data to direct byte	3	0.679	2.886	43
XRL	A,Rn	exclusive-OR register to A	1	0.459	1.715	6*
XRL[1]	A,direct	exclusive-OR direct byte to A	2	0.584	2.361	65
XRL	A,@Ri	exclusive-OR indirect RAM to A	1	0.486	1.873	66, 67
XRL	A,#data	exclusive-OR immediate data to A	2	0.540	2.128	64
XRL	direct,A	exclusive-OR A to direct byte	2	0.614	2.550	62
XRL	direct,#data	exclusive-OR immediate data to direct byte	3	0.679	3.017	63
CLR	A	clear A	1	0.374	1.265	E4
CPL	A	complement A	1	0.398	1.511	F4
RL	A	rotate A left	1	0.383	1.388	23
RLC	A	rotate A left through the carry flag	1	0.383	1.390	33
RR	A	rotate A right	1	0.382	1.381	03
RRC	A	rotate A right through the carry flag	1	0.383	1.382	13
SWAP	A	swap nibbles within A	1	0.371	1.394	C4

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
Data transfer						
MOV	A,Rn	move register to A	1	0.377	1.406	E*
MOV	A,direct	move direct byte to A	2	0.509	2.080	E5
MOV	A,@Ri	move indirect RAM to A	1	0.408	1.568	E6, E7
MOV	A,#data	move immediate data to A	2	0.426	1.752	74
MOV	Rn,A	move A to register	1	0.344	1.347	F*
MOV	Rn,direct	move direct byte to register	2	0.602	2.654	A*
MOV	Rn,#data	move immediate data to register	2	0.415	1.839	7*
MOV	direct,A	move A to direct byte	2	0.477	2.024	F5
MOV	direct,Rn	move register to direct byte	2	0.536	2.294	8*
MOV	direct,direct	move direct byte to direct byte	3	0.661	2.950	85
MOV	direct,@Ri	move indirect RAM to direct byte	2	0.564	2.438	86, 87
MOV	direct,#data	move immediate data to direct byte	3	0.679	3.017	75
MOV	@RI,A	move A to indirect RAM	1	0.378	1.517	F6, F7
MOV	@Ri,direct	move direct byte to indirect RAM	2	0.633	2.629	A6, A7
MOV	@Ri,#data	move immediate data to indirect RAM	3	0.448	2.019	76, 77
MOV	DPTR,#data 16	load data pointer with a 16-bit constant	3	0.519	2.267	90
MOVC	A,@A+DPTR	move code byte relative to DPTR to A	1	0.775	3.570	93
MOVC	A,@A+PC	move code byte relative to PC to A	1	0.770	3.374	83
MOVX	A,@Ri	move external RAM (8-bit address) to A	1	0.707	2.732	E2, E3
MOVX	A,@DPTR	move external RAM (16-bit address) to A	1	0.710	2.605	E0
MOVX	@Ri,A	move A to external RAM (8-bit address)	1	0.629	2.595	F2, F3
MOVX	@DPTR,A	move A to external RAM (16-bit address)	1	0.631	2.439	F0
PUSH	direct	push direct byte onto stack	2	0.600	2.543	C0
POP	direct	pop direct byte from stack	2	0.606	2.548	D0
XCH	A,Rn	exchange register with A	1	0.513	1.847	C*
XCH	A,direct	exchange direct byte with A	2	0.645	2.526	C5
XCH	A,@Ri	exchange indirect RAM with A	1	0.544	2.024	C6, C7
XCHD	A,@Ri	exchange LOW-order nibble indirect RAM with A	1	0.486	1.904	D6, D7
Boolean variable manipulation						
CLR	C	clear carry flag	1	0.293	1.075	C3
CLR	bit	clear direct bit	2	0.597	2.509	C2
SETB	C	set carry flag	1	0.293	1.084	D3
SETB	bit	set direct bit	2	0.611	2.603	D2
CPL	C	complement carry flag	1	0.320	1.134	B3
CPL	bit	complement direct bit	2	0.583	2.471	B2
ANL	C,bit	AND direct bit to carry flag	2	0.540	2.187	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	0.563	2.388	B0

MNEMONIC		DESCRIPTION	BYTES	EXEC. TIME [μs]	ENERGY [NJ]	OPCODE (HEX)
ORL[2]	C,bit	OR direct bit to carry flag	2	0.561	2.341	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	0.561	2.341	A0
MOV	C,bit	move direct bit to carry flag	2	0.610	2.542	A2
MOV	bit,C	move carry flag to direct bit	2	0.610	2.542	92
Program and machine control						
ACALL	addr11	absolute subroutine call	2	0.840	3.384	•1 addr
LCALL	addr16	long subroutine call	3	1.082	4.562	12
RET		return from subroutine	1	1.082	4.562	22
RETI		return from interrupt	1	1.082	4.562	32
AJMP	addr11	absolute jump	2	0.670	2.524	♦1 addr
LJMP	addr16	long jump	3	0.840	3.384	02
SJMP	rel	short jump (relative address)	2	0.670	2.524	80
JMP	@A+DPTR	jump indirect relative to the DPTR	1	1.049	4.015	73
JZ	rel	jump if A is zero	2	0.639	2.224	60
JNZ	rel	jump if A is not zero	2	0.754	2.896	70
JC	rel	jump if carry flag is set	2	0.620	2.128	40
JNC	rel	jump if carry flag is not set	2	0.733	2.705	50
JB	bit,rel	jump if direct bit is set	3	0.788	3.095	20
JNB	bit,rel	jump if direct bit is not set	3	0.902	3.708	30
JBC	bit,rel	jump if direct bit is set and clear bit	3	0.894	3.520	10
CJNE	A,direct,rel	compare direct to A and jump if not equal	3	0.855	3.307	B5
CJNE	A,#data,rel	compare immediate to A and jump if not equal	3	0.794	3.024	B4
CJNE	Rn,#data,rel	compare immediate to register and jump if not equal	3	0.787	3.139	B*
CJNE	@Ri,#data,rel	compare immediate to indirect and jump if not equal	3	0.822	3.333	B6, B7
DJNZ	Rn,rel	decrement register and jump if not zero	2	0.857	3.474	D*
DJNZ	direct,rel	decrement direct and jump if not zero	3	0.991	4.178	D5
NOP		no operation	1	0.284	1.027	00

Notes

1. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct field addresses one of the I/O ports (P0 to P3) then the standard 80C51 uses the port pin input state for the operation while the PCA5010 uses the SFR contents.
2. This opcode works in a slightly different way to a standard 80C51 CPU. If the direct bit field addresses one of the port bits, then the state of the corresponding port pin is written to the port SFR after execution of the instruction.

Table 61 Notation for data addressing modes

SYMBOL	DESCRIPTION
Rn	working registers R0 to R7
direct	128 internal RAM locations and any special function register (SFR).
@Ri	indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2-kbyte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

Table 62 Hexadecimal opcode cross-reference

SYMBOL	DESCRIPTION
*	8, 9, A, B, C, D, E and F
•	11, 31, 51, 71, 91, B1, D1 and F1
◆	01, 21, 41, 61, 81, A1, C1 and E1

7.1 Instruction Map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC@Ri					INC Rn				
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC@Ri					DEC Rn				
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri					ADD A,Rn				
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri					ADDC A,Rn				
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri					ORL A,Rn				
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri					ANL A,Rn				
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri					XRL A,Rn				
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data					MOV Rn,#data				
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri					MOV direct,Rn				
9	MOV DPTR,#data 16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri					SUBB A, Rn				
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,direct					MOV Rn,direct				
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel					CJNE Rn,#data,rel				
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri					XCH A,Rn				
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri					DJNZ Rn,rel				
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri		CLR A	MOV * A,direct	MOV A,@Ri					MOV A,Rn				
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A		CPL A	MOV direct,A	MOV @Ri,A					MOV Rn,A				

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* MOV A, ACC is not a valid instruction.

8 LIMITING VALUES

According to the Absolute Maximum Ratings System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{BAT}	battery supply voltage	−0.5	+2.0	V
V_{DD}	supply voltage	−0.5	+5.0	V
V_I	input voltage (all inputs)	−0.3	V_{DD} + 0.3	V
$I_{I/O}$	maximum sink/source current for all input/output pins	−10	+10	mA
I_{BAT}, I_{IND}	maximum supply current for pins V_{BAT} and VIND	−	100	mA
I_{DD}	maximum supply current for any supply pin	−	50	mA
P_{tot}	total power dissipation	−	100	mW
$V_{ESD(HBM)}$	maximum ESD stress level applied to V_{PP} pin using human body model	−	2000	V
$V_{ESD(MM)}$	maximum ESD stress level applied to V_{PP} pin using machine model	−	200	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature (for all devices)	−10	+55	°C

Note

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise specified.

9 EXTERNAL COMPONENTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Discrete components					
L	inductor	330	470	1000	µH
C_o	output capacitor	−	4.7	10.0	µF
R_{FB}	feedback oscillator resistance	2.0	2.2	−	MΩ
R_{X1}	parasitic serial resistance of quartz	−	−	20	kΩ

10 DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.2 V; V_{BAT} = 1.2 V; T_{amb} = −10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified; DC/DC converter configured as indicated in note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Battery supply						
V_{BAT}	battery operating voltage	note 2	0.9	1.2	1.6	V
$I_{BAT(reset)}$	static reset supply current	V_{BAT} = 1.2 V; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7; I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	5	µA
$I_{DD(reset)}$	static reset supply current	V_{DD} = 2.2 V; pin RESETIN at V_{BAT}; XTL1 at V_{SS}; P1.6, P1.7, I, Q, $\overline{EA}$, TCLK, V_{PP} at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	0.5	10	µA
R_{NFET}	NFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V; note 3	–	1.1	2	Ω
R_{PFET}	PFET pin-to-pin resistance	T_{amb} = 25 °C; V_{DD} = 2.2 V; note 3	–	1.2	2	Ω
$I_{L(NFET)}$	NFET leakage current		–	–	1	µA
$I_{L(PFET)}$	PFET leakage current		−1	–	–	µA
$I_{NFET(max)}$	maximum allowed NFET current		–	–	50	mA
$I_{PFET(max)}$	maximum allowed PFET current		–	–	50	mA
DC/DC converter in off mode						
V_{DD}	DC supply voltage output		V_{BAT} − 0.1	–	V_{BAT}	V
$I_{BAT(off)}$	current consumed from V_{BAT} by the DC/DC converter itself	V_{DD} = V_{BAT}; all inputs at V_{SS} or V_{DD}; all outputs and I/Os open-circuit	–	6	–	µA
DC/DC converter in standby mode						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5010 and external chips	note 4; programmable in 4 steps	1.8	1.9	2.3	V
		1.9: [VLO, VLO] = 00	–	1.9	–	V
		2.0: [VLO, VLO] = 01	–	2.0	–	V
		2.1: [VLO, VLO] = 10	–	2.1	–	V
		2.2: [VLO, VLO] = 11	–	2.2	–	V
V_{DROP}	DC voltage drop due to load	I_L = 500 µA; notes 4 and 5	–	–	100	mV
$V_{ripple(p-p)}$	ripple voltage (peak-to-peak value)	notes 5 and 6	–	50	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{BAT(stb)}$	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 7 and 8	–	25	–	µA
$I_{DD(max)(stb)}$	maximum delivered continuous supply current	V_{BAT} = 0.9 V; R_s = 8 Ω; notes 8 and 9; see Fig.38	1	–	–	mA
$\eta_{(stb)}$	efficiency of DC/DC converter in standby mode	V_{BAT} = 1.2 V; I_{DD} = 100 µA; note 8	–	80	–	%
DC/DC converter in high current mode (non standby)						
V_{DD}	DC supply voltage generated by the on-chip DC/DC converter for the PCA5010 and external chips	note 4	2.2 – 6%	2.2	2.2 + 6%	V
$V_{DD(av)}$	mean DC voltage	notes 4 and 5	2.1	2.2	2.3	V
$V_{HFripple(p-p)}$	ripple voltage for frequencies above 20 kHz (peak-to-peak value)	notes 5 and 8	–	–	100	mV
$V_{LFripple(p-p)}$	low frequency ripple voltage caused by load variations (peak-to-peak value)	notes 3, 5 and 8	–	–	100	mV
$I_{BAT(norm)}$	current consumed from V_{BAT} by the DC/DC converter itself	T_{amb} = 25 °C; notes 8 and 10; see Fig.51	–	110	–	µA
$I_{DD(max)}$	maximum delivered supply current	V_{BAT} = 0.9 V; R_s= 8 Ω; notes 8 and 9; see Fig.37	10	–	–	mA
		V_{BAT} = 1.0 V; R_s = 5 Ω; notes 8 and 9	20	–	–	mA
$\eta_{(norm)}$	efficiency of DC/DC converter	note 8				
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 3 mA	–	90	–	%
		$V_{BAT} \geq$ 1.2 V; I_{DD} = 10 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 3 mA	–	85	–	%
		V_{BAT} = 0.9 V; I_{DD} = 10 mA	–	75	–	%
External supply current from V_{DD} = 2.2 V and V_{BAT} = 1.2 V						
V_{DD}	DC supply voltage (V_{DD} and V_{DDA} pins)	note 11; see Fig.64	2.2	2.2	2.5	V
I_{BAT}	operating battery current	T_{amb} = 25 °C; 76.8 kHz quartz	–	2	–	µA
$I_{DD(stb)}$	operating standby mode supply current from V_{DD}	T_{amb} = 25 °C; note 7	–	12	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(RX)}$	operating receive mode supply current from V_{DD}	T_{amb} = 25 °C; note 10	–	85	–	µA
Supply current from internal or external V_{DD} = 2.2 V						
$I_{DD(micro)}$	I_{DD} due to operation of microcontroller	T_{amb} = 25 °C; note 12	–	0.7	–	mA/MIPS
$I_{DD(UART)}$	increase in I_{DD} due to operation of the UART	T_{amb} = 25 °C	–	5	–	µA
$I_{DD(IIC)}$	increase in I_{DD} due to operation of the I^2C-bus master	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(T0)}$	increase in I_{DD} due to operation of timer/counter0	T_{amb} = 25 °C	–	0	–	µA
$I_{DD(T1)}$	increase in I_{DD} due to operation of timer/counter1	T_{amb} = 25 °C	–	2	–	µA
$I_{DD(AFC)}$	supply current due to operation of AFC-DAC	T_{amb} = 25 °C	–	60	–	µA
$I_{DD(SBLI)}$	supply current due to battery measurement active (SBLI = 1)	T_{amb} = 25 °C	–	20	–	µA
$I_{DD(6MHz)}$	increase in I_{DD} due to activation of 6 MHz oscillator in standby mode	T_{amb} = 25 °C; frequency adjusted to 6 MHz	–	50	–	µA
OTP programming (OTP data retention can only be guaranteed if the devices are preprogrammed by Philips Semiconductors; data retention cannot be guaranteed for customer programmed samples)						
$V_{DD(prog)}$	supply voltage during programming	note 11	2.2	–	3.6	V
V_{PP}	program supply voltage		12.5	–	13	V
I_{PP}	program supply current	note 13	–	24	–	mA
$T_{amb(prog)}$	operating ambient temperature during programming		21	–	27	°C
Band gap (reference voltage for all comparators)						
V_{BG}	band gap voltage	[VBG1, VBG0] = 00	1.23	1.26	1.29	V
		[VBG1, VBG0] = 01	–	1.233	–	V
		[VBG1, VBG0] = 10	–	1.286	–	V
		[VBG1, VBG0] = 11	–	1.312	–	V
Initial V_{DD} OK detection						
$V_{DD(OK)}$	V_{DD} OK indication	T_{amb} = 25 °C	1.5	1.85	2.0	V
Battery low indicator						
V_{BLI}	battery low indication	[VBG1, VBG0] = 00	1.05	1.1	1.15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins I(D1), Q(D0) and TCLK						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	0.1	µA
Digital input pin RESETIN						
V_{IL}	input low level		–	–	$0.2V_{BAT}$	V
V_{IH}	input high level		$0.8V_{BAT}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–0.1	–	0.1	µA
Digital input/output pin $\overline{EA}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
$I_{NMOS(h)}$	NMOS hold current	V_{DD} = 2.2 V; V_I = 0.6 V	–	–	200	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–200	–	–	µA
Digital output pin $\overline{RESOUT}$						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
Digital input/output pins $\overline{PSEN}$						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
Digital input/output pins ALE						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	1.5	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–1.5	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
Microcontroller input/output ports P0, P1 and P2 pins (except P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	0.75	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–0.75	mA
I_{pu}	weak pull-up current	V_{DD} = 2.2 V; V_I = 0 V	–20	–7	–2	µA
$I_{PMOS(h)}$	PMOS hold current	V_{DD} = 2.2 V; $V_I = V_{DD}/2$	–200	–70	–20	µA
Microcontroller output port P3 pins						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.6 V	4	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.6$ V	–	–	–6	mA
Open drain pins SDA and SCL (P1.6 and P1.7)						
V_{IL}	LOW-level input voltage	output not sinking current	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	output not sinking current	$0.8V_{DD}$	–	–	V
I_L	leakage current	$V_I = V_{DD}$	–1	–	+1	µA
$I_{sink(stat)}$	static output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	2.25	–	–	mA
$I_{sink(stat)(sc)}$	static output sink short-circuit current	V_{DD} = 2.2 V; $V_I = V_{DD}$	2.2	6	14	mA
AT output pin						
$I_{(o)sink}$	output sink current	V_{DD} = 2.2 V; V_I = 0.4 V	3	–	–	mA
$I_{(o)source}$	output source current	V_{DD} = 2.2 V; $V_I = V_{DD} - 0.4$ V	–	–	–3	mA
76.8 kHz oscillator						
$V_{IL(XTL1)}$	LOW-level input voltage XTL1		–	–	0.3	V
$V_{IH(XTL1)}$	HIGH-level input voltage XTL1		1	–	–	V
$I_{LI(XTL1)}$	leakage current at XTL1	$V_I = V_{BAT}$ or V_{SS}	–1	–	+1	µA
I_{bias}	bias current from XTL2 to V_{SS}	V_{BAT} = 1.6 V; XTL1 at V_{SS}	0.5	0.8	1.1	µA
I_{op}	operating current consumption	V_{BAT} = 1.6 V; R_{FB} = 2.2 MΩ	–	2	–	µA
g_m	transconductance	I_o = ±0.3 µA	5	20	60	µA/V
V_{WP}	DC working point		–	550	–	mV
AFC-DAC						
V_{AFC}	resolution		–	$1/64V_{DD}$	–	V
ΔAFC	deviation for codes between 010000 and 100000 from straight line		–0.25LSB	–	+0.25LSB	
$R_{L(DAC)}$	allowed resistive load at DAC output		10	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{L(DAC)}$	allowed capacitive load at DAC output		–	–	50	pF
$I_{source(DAC)}$	AFCOUT source current	V_{DD} = 2.2 V; $V_{AFCOUT} = V_{DD} - 0.4$ V; code = 111111	–	–895	–100	µA
$I_{sink(DAC)}$	AFCOUT sink current	V_{DD} = 2.2 V; V_{AFCOUT} = 0.4 V; code = 000000	10	25	–	µA

Notes

1. DC/DC converter configured with inductor of L = 470 µH, SRL = 5 Ω, input capacitance of C_i = 4.7 µF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 µF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. The required V_{BAT} for starting the circuit after connecting it to the battery is 1.1 V. But once in place, the battery can be used until it is discharged to 0.9 V.
3. This parameter is not tested during production; it is guaranteed by design.
4. This parameter is not tested during production; it is covered by other measurements.
5. The accuracy of the voltage is defined by maximum offset and ripple voltage. DC offset is defined by the accuracy of the internal band gap reference and the offset of comparators, whereas the ripple voltage is defined by the limits of the allowed voltage window of the regulated V_{DD}.
6. The ripple in standby mode is defined by V_{BAT}, L, t_n and ESR (see Table 54).
7. PCA5010 set to standby mode by software: 76.8 kHz oscillator running, DC/DC converter running in standby mode, all timer/counters disabled except RTC, microcontroller Idle, all outputs open-circuit, no I_{DD} delivered to external circuits.
8. This parameter depends on external components and is not tested during production; hence no guarantee.
9. R_s = total series resistance = R_{BAT} + SRL + $R_{DS(on)}$ + ESR.
10. PCA5010 set to receive mode by software: 76.8 kHz and 6 MHz oscillator running, DC/DC converter running in normal mode, wake-up counter, clock compensation, watchdog timer, T0 and T1 enabled, demodulator set to direct input data, AFC disabled, microcontroller Idle, all outputs open-circuit, no I_{DD} delivered to external circuits.
11. The minimum supply voltage is determined by the start-up sequence of the device. When the start-up sequence is completed, the supply voltage can be lowered to 1.8 V.
12. The microcontroller operates with approximately 1.9 million instructions per second at a V_{DD} = 2.2 V. The current consumption at this V_{DD} is 0.7 mA/MIPS (peripheral blocks as e.g. timers, DC/DC converter, I²C-bus, UART, demodulator etc., are excluded). The current required from V_{DD} is then 1.35 mA (typ.). This scales to

$$I_{BAT} = \frac{V_{DD}}{V_{BAT}} \times I_{DD} = 2.5 \text{ mA sunk from } V_{BAT}.$$

13. In mass program mode the current can increase to 100 mA.

11 AC CHARACTERISTICS

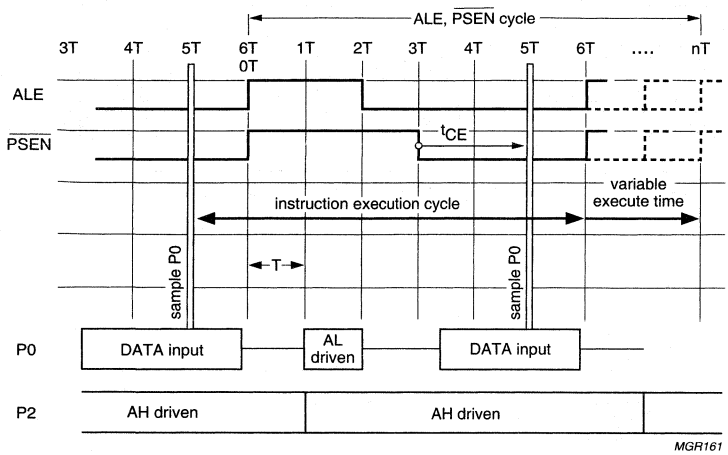
V_{BAT} = 0.9 to 1.6 V; V_{SS} = 0 V; T_{amb} = −10 to +55 °C; all voltages referenced to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC/DC converter; see note 1						
t_{on}	turn on time	off to normal operation; I_L < 500 µA; note 2	–	–	5	ms
$t_{ch(mode)}$	mode change time	enable to standby and reverse; note 2	–	–	1	ms
t_{step}	load step accommodation delay until stable	load step from 10 µA to 6 mA; note 3	–	–	1	ms
f_{sw}	switching frequency	in normal mode; note 2	120	250	400	kHz
t_{sw}	switching period	in standby mode; note 4	1 or 1.5 t_{XTL1}	–	–	µs
$t_{ch(L)}$	inductor charge time	in standby mode; note 4	–	0.5 or 1 t_{XTL1}	–	µs
RESET signal						
$t_{RESETIN(min)}$	minimum duration of RESETIN pulse		20	–	–	µs
Microcontroller						
$t_{instr(int)}$	internal instruction execution time	internal access, V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	550	–	ns
$t_{instr(ext)}$	external instruction execution time	external access, V_{DD} = 2.2 V; T_{amb} = 25 °C; note 5	–	650	–	ns
76.8 kHz oscillator						
f_{xtal}	crystal frequency	note 3	76784	76800	76816	Hz
$f_{i(max)}$	maximum input frequency through input buffer		–	–	100	kHz
C_1	input capacitance		–	10 ± 15%	–	pF
C_2	output capacitance		–	10 ± 15%	–	pF
6 MHz oscillator						
$f_{i(osc)}$	oscillator input frequency	[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 00000 (reset condition)	3	5.4	8	MHz
		[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 10000	1	2.7	5	MHz
		[$\overline{SF4}$, SF3, SF2, SF1, SF0] = 01111	6	7.6	11	MHz
$f_{i(osc)} \pm \Delta f$	adjusted frequency		5.85	6	6.15	MHz
$t_{d(en)}$	enable oscillator delay	note 2	–	20	30	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ZIF (I and Q) demodulator						
f_{offset}	offset from 0 frequency	note 2	6	–	–	kHz
$t_{(ENA-AVG)}$	ENA to valid AVG value	3 kHz offset; note 2	–	–	100	ms
t_{ENB}	ENB to valid demodulator output	note 2	–	–	1	symbol duration
t_{ENC}	ENB to correct recovered clock	note 2	phase error curves apply (see Fig.27)			
All outputs						
$t_{r,f}$	rise and fall times for outputs	C_L = 20 pF	–	15	–	ns
Open-drain pins SDA and SCL (P1.7 and P1.6)						
t_n	noise suppression filter		–	60	–	ns
$\Delta V/\Delta t$	slope for the falling edge	R_L = 20 kΩ; C_L = 50 pF; V_{DD} = 2.2 V	–	50	–	ns/V
dI/dt	slope for both edges	R_L = 20 kΩ; C_L = 50 pF	–	250	–	μA/ns
$I_{o(sink)(swL)}$	dynamic output sink current during switching low (Miller compensated)	V_{DD} = 2.2 V; R_L = 20 kΩ; C_L = 50 pF	–	2	–	mA
OTP programming characteristics						
$V_{SU;PP}$	V_{PP} set-up time		10	–	–	μs
$t_{W(prog)}$	program pulse width		100	–	–	μs
$t_{W(prog)(sec)}$	program pulse security bits		200	–	–	μs
$t_{W(prog)(rec)}$	program pulse recover time		1	–	–	μs
AFC-DAC						
$t_{start(DAC)}$	start-up time disabled DAC to stable output for code 111111	note 2	–	50	100	μs
PSRR	power supply ripple rejection (V_{DD} -> DAC)		–	0	–	dB
t_{slew}	slew time for analog output from 10 to 90% for a voltage step of 1 V	code 010000 <-> 110000	–	2.5	–	μs

Notes

1. DC/DC converter configured with inductor of L = 470 μH, SRL = 5 Ω, input capacitance of C_i = 4.7 μF, ESR = 0.5 Ω, V_{DD} output capacitor C_o = 4.7 μF, ESR = 0.5 Ω, R_{BAT} < 1 Ω.
2. This parameter is not tested during production; it is guaranteed by design.
3. This parameter depends on external components.
4. At high load or low battery voltage the inductor charge time can be extended to a full XTL1 period, while the minimum inductor discharge time is a half XTL1 period.
5. The execution time is strongly dependant on command type and addressing mode (see also Table 60).



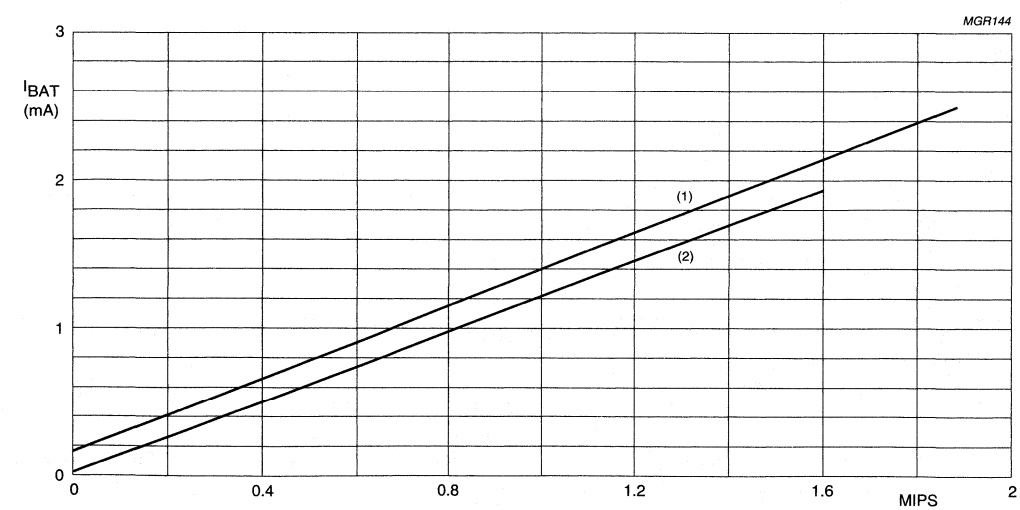
T being the half period of the internal 6 MHz oscillator for normal external access and of TCLK for emulation, programming and test modes.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, Temperature, Opcode).

Execution of an op-code goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.46 External access timing.

12 CHARACTERISTIC CURVES

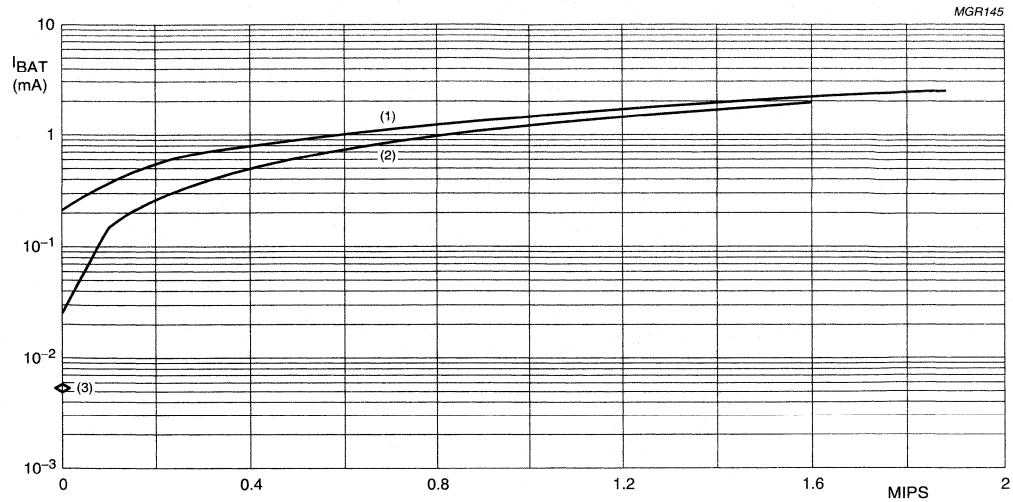


V_{BAT} = 1.2 V.

(1) DC/DC converter in normal mode.

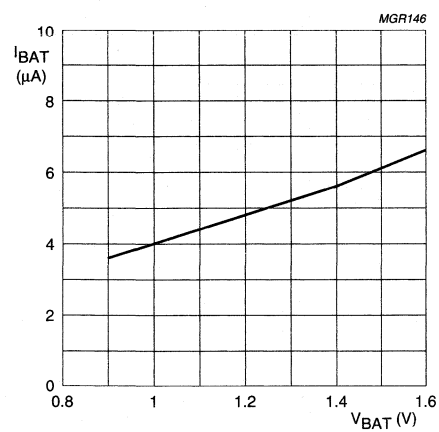
(2) DC/DC converter in standby mode.

Fig.47 Measured battery current consumption as function of mean microcontroller instruction rate.



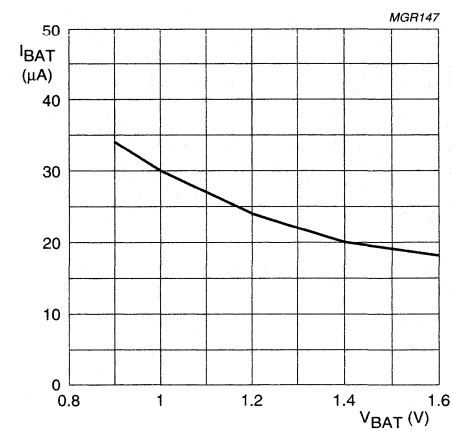
V_{BAT} = 1.2 V.
(1) DC/DC converter in normal mode.
(2) DC/DC converter in standby mode.
(3) DC/DC converter in off mode.

Fig.48 Measured battery current consumption as function of mean microcontroller instruction rate.



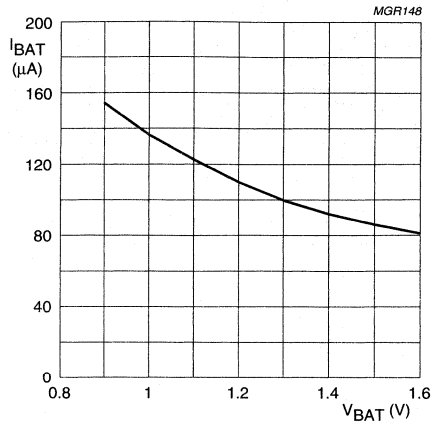
V_{DD} = V_{BAT}, microcontroller idle, all functions disabled.

Fig.49 Supply current in off mode.



V_{DD} = 1.9 V, microcontroller idle, all functions disabled.

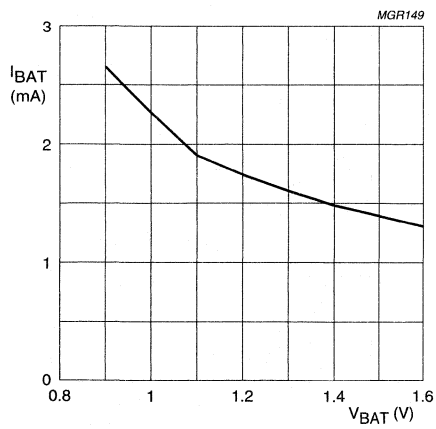
Fig.50 Supply current in standby mode.



V_{DD} = 2.2 V, microcontroller idle, all functions disabled.

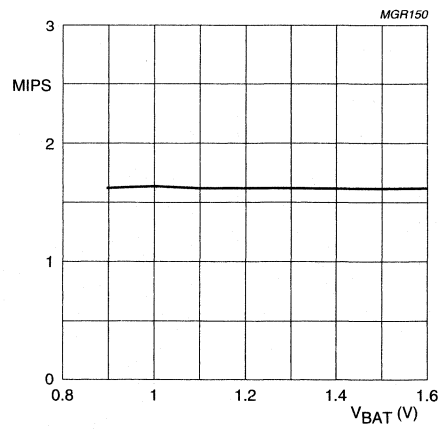
Note: This curve cannot be directly measured by varying V_{BAT}, because the shown current is the battery current in discontinuous mode. Changing the battery voltage can force the DC/DC converter to enter continuous mode. At a given battery voltage a mode change from continuous to discontinuous mode happens only after a load reduction.

Fig.51 Supply current in normal mode.



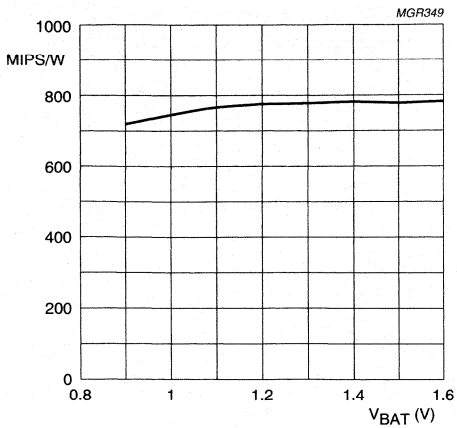
V_{DD} = 1.9 V, microcontroller running at approximately 1.6 MIPS, all other functions disabled.

Fig.52 Supply current in standby mode.



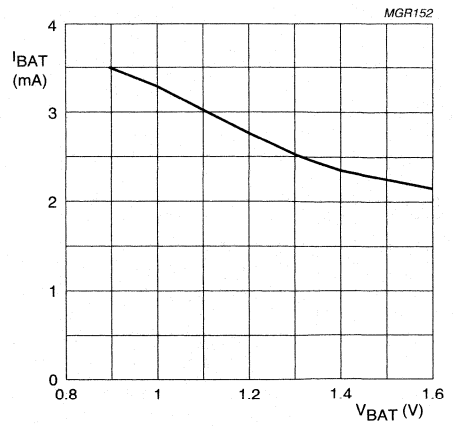
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.53 CPU speed performance with DC/DC in standby mode.



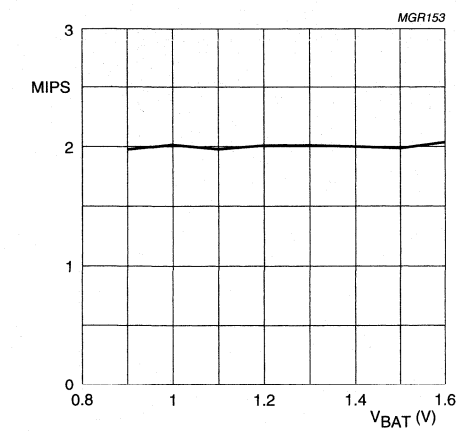
V_{DD} = 1.9 V, microcontroller running at maximum speed.

Fig.54 Overall power/speed performance with DC/DC in standby mode.



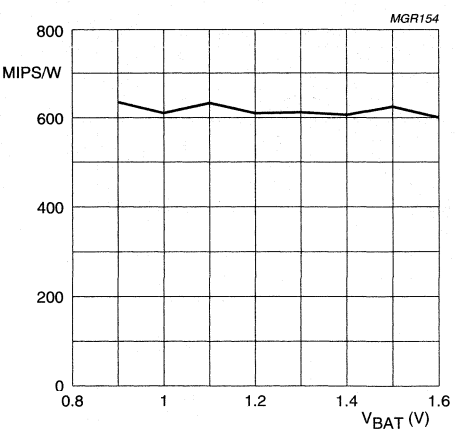
V_{DD} = 2.2 V, microcontroller running at approximately 2 MIPS, all other functions disabled.

Fig.55 Supply current in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.56 CPU speed performance with DC/DC converter in normal mode.



V_{DD} = 2.2 V, microcontroller running at maximum speed.

Fig.57 Overall power/speed performance with DC/DC converter in normal mode.

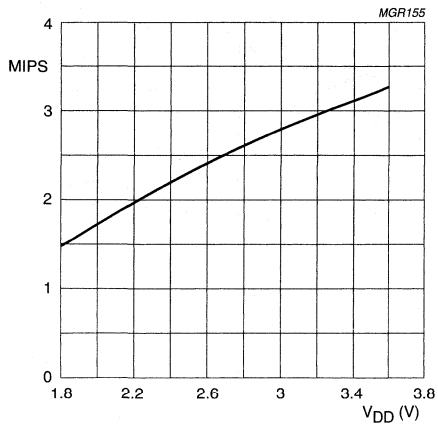


Fig.58 Speed performance PCA5010 when V_{DD} is externally supplied (DC/DC converter not used).

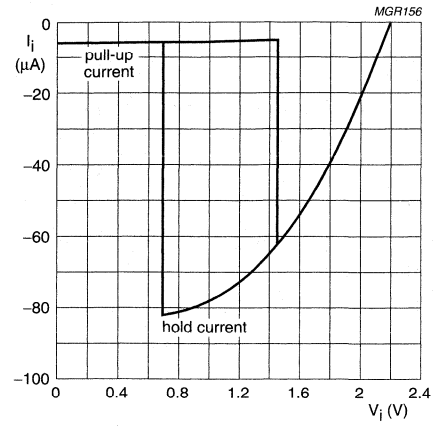


Fig.59 Typical impedance characteristic of standard port in input mode.

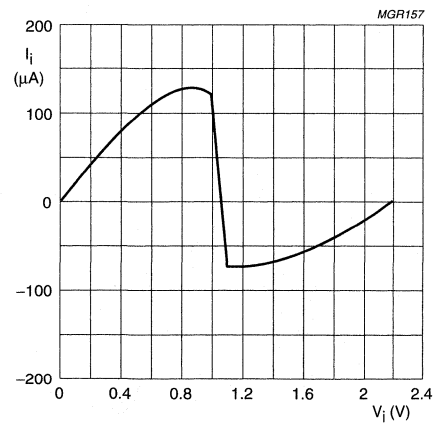
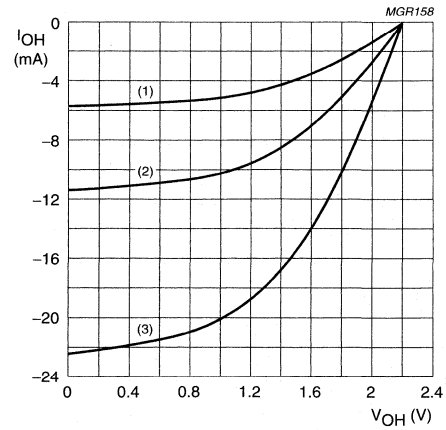
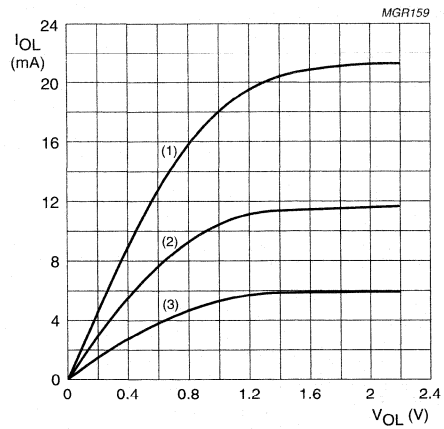


Fig.60 Typical impedance characteristic of $\overline{EA}$ pin in input mode.



(1) Pins P0.X, P1.X, P2.X, $\overline{PSEN}$ and $\overline{EA}$.
(2) Pins $\overline{RESOUT}$ and ALE.
(3) Pins P3.X and AT.

Fig.61 Typical output characteristics driven HIGH (digital output/port pins except P1.6 and P1.7).



(1) Pins P3.X and AT.
(2) Pins $\overline{\text{RESOUT}}$ and ALE.
(3) Pins P0.X, P1.X, P2.X, $\overline{\text{PSEN}}$ and $\overline{\text{EA}}$.

Fig.62 Typical output characteristics LOW (digital output/port pins except P1.6 and P1.7).

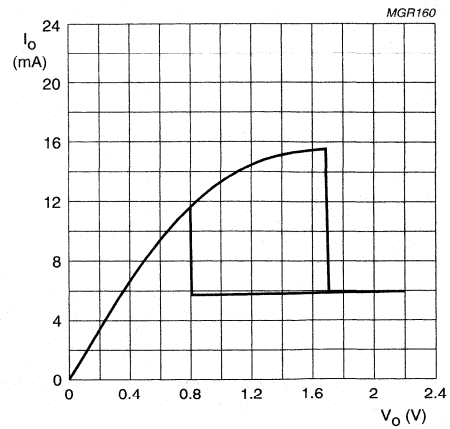


Fig.63 Typical output characteristics LOW for P1.6 and P1.7.

13 TEST AND APPLICATION INFORMATION

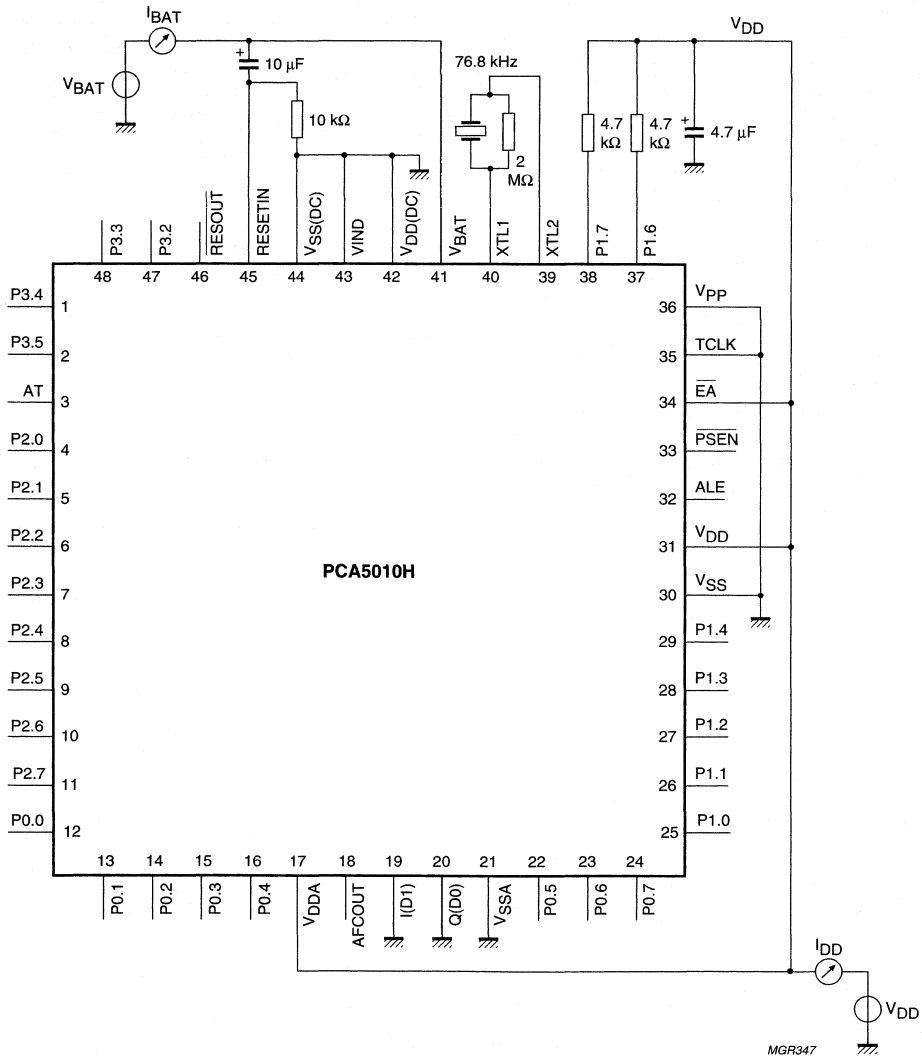


Fig.64 Test circuit for current measurements with external V_{DD} supply.

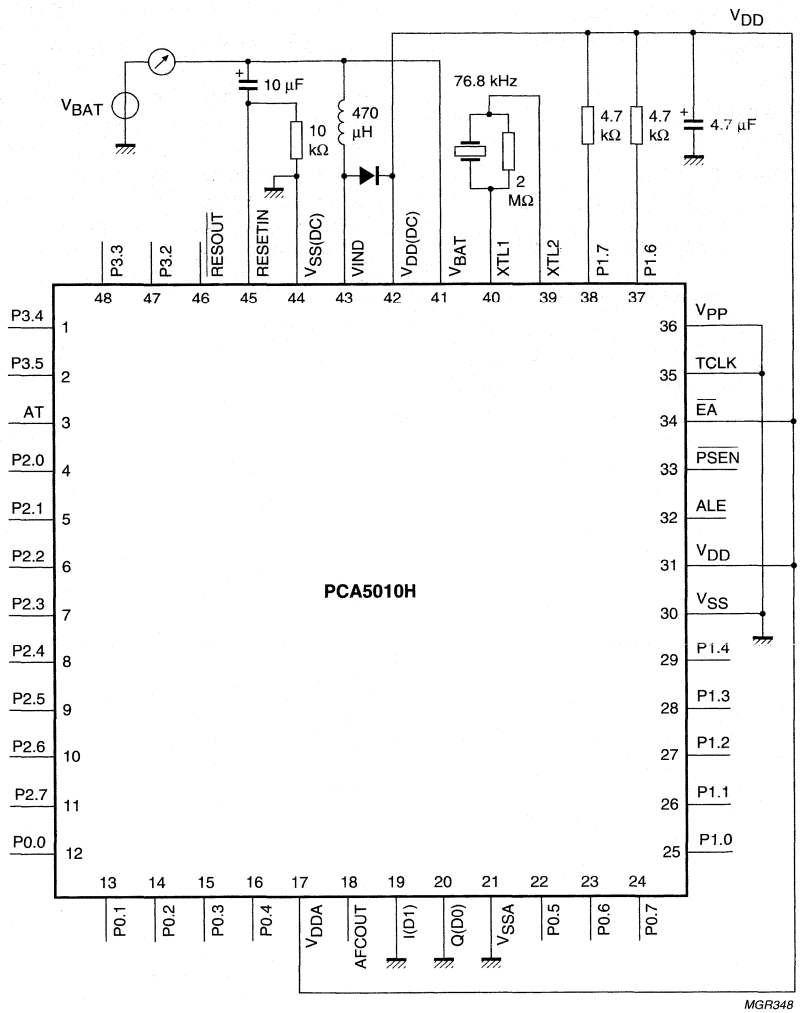


Fig.65 Test circuit for current measurements with on-chip DC/DC converter active.

14 APPENDIX 1: SPECIAL MODES OF THE PCA5010

14.1 Overview

During the rising edge of the external $\overline{\text{RESOUT}}$ signal, the state of the pins ALE, $\overline{\text{PSEN}}$, $\overline{\text{EA}}$ and P2.X is sampled and stored. The following decoding (ALE, $\overline{\text{PSEN}}$ and P2) is used to force the PCA5010 into different operating modes:

[1, 1, X] → RUN mode

[0, 1, X] → EMUlation modes (for P2 decoding refer to Metalink documents)

[1, 0, Y] → test mode, submode Y

[0, 0, X] → OTP parallel programming mode.

The customer will usually only see the normal RUN mode.

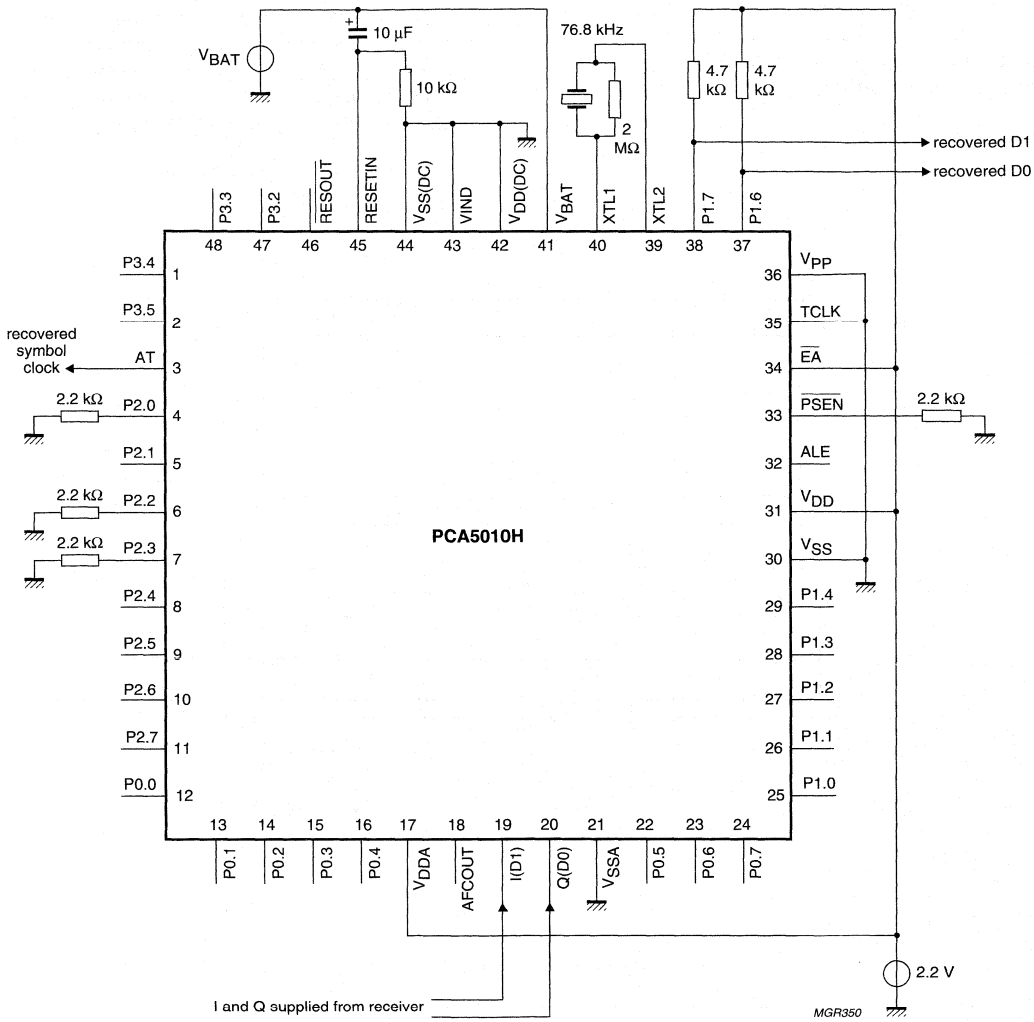
14.2 OTP parallel programming mode

The OTP parallel programming mode is used to access the on-chip OTP directly from the device pins for programming and verification. The OTP parallel programming mode and its initialization are explained in detail in Chapter 15.

14.3 Test modes

The test modes of the PCA5010 are used during the production test of the circuit. Test modes are not intended to be used by customers except test mode 2, the demodulator and clock recovery test mode.

Test mode 2 may be used by customers for BER measurements in closed-loop systems. The following application diagram (see Fig.66) shows an application which enters this mode during start-up. After the test mode is entered the PCA5010 starts execution of code from the internal program memory. This code must enable the demodulator and clock recovery in the required modes. If the microcontroller is requested to make port I/O, then a frequency of approximately 6 MHz with V_{DD} level needs to be supplied at the TCLK pin.



The OTP must contain code that enables the demodulator and clock recovery in the desired operating modes.

Fig.66 Application diagram for entering the demodulator test mode after reset.

15 APPENDIX 2: THE PARALLEL PROGRAMMING MODE

15.1 Introduction

This document describes the parallel programming mode of the PCA5010. Parallel programming mode is the mode where the OTP is programmed by an EPROM programmer or by a tester.

15.2 General description

The PCA5010 is packaged in a LQFP48 package. Port 0 and Port 2 are available for programming. To program the OTP of the PCA5010, multiplexing of addresses and data is necessary. Port 0 is a bidirectional data port, used for the memory addresses and the program and verify data. Port 2 is an input port which controls the parallel programming mode. A coarse block diagram of the OTP interface in parallel programming mode is given in Fig.67.

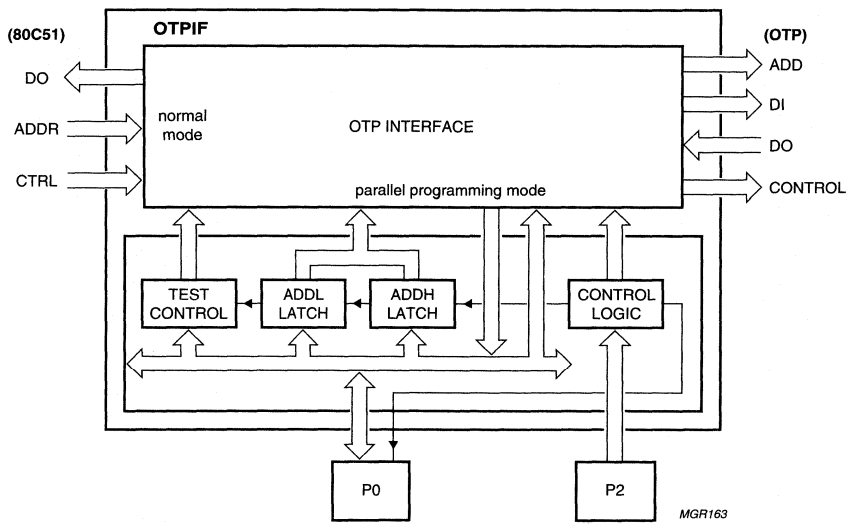


Fig.67 The OTP interface in parallel programming mode.

15.2.1 SIGNALS FOR THE PARALLEL PROGRAMMING MODE

In this configuration, the following signals are necessary to program the OTP:

Table 63 Pins for programming mode

OTP PIN	TYPE	EPROM PIN	DESCRIPTION	COMMENTS
V_{PP}	supply	V_{PP}	programming voltage	special pin/logic signal not time critical
V_{DD}	supply	V_{DD}	positive supply	
GND	supply	GND	negative supply	
P0.7 to P0.0	IO	A<14:0>	address	32 kbytes addresses available
		Q<7:0>	data-output	
		I<7:0>	data-input	
		PS<2:0>	security bits input	connected to P0.2 to P0.0 pins
		QS<2:0>	security bits output	
P2.0/LS0	input	–	latch select 0	latch select signals, see Table 64
P2.1/LS1	input	–	latch select 1	
P2.2/PGM	input	–	programming mode	
P2.3/RdStrb	input	CEP/MBPC	read/strobe	read enable clock (CEP) when PGM = 0; strobe for the latches when PGM = 1
P2.4/GBMbpB	input	GB	output enable not/ Mult.BProg Not	read EPROM and set P0 as output; multiple byte programming when PGM = 1
P2.5/WEB	input	WEB	write enable not	programs data if V_{PP} is present
P2.6/SEC	input	SEC	select security bits	see Section 15.10
P2.7/SIG	input	SIG	read signature bytes	see Section 15.9

The control signals GBMbpB, PGM, LS1 and LS0 can be used to select the latches of the interface block and the internal data latches of the OTP. Table 64 shows how the latches are selected.

RdStrb is used to open the selected latch. If PGM is not active the RdSTrb signal is used to start the OTP read cycle.

Table 64 Latch selection

P2.4/GBMbpB	P2.2/PGM	P2.1/LS1	P2.1/LS0	DESCRIPTION
X	0	X	X	no latches selected
1	1	0	0	select test control latch
X	1	0	1	select lower address latch
X	1	1	0	select upper address latch
0	1	1	1	select internal data latch in multi byte programming mode

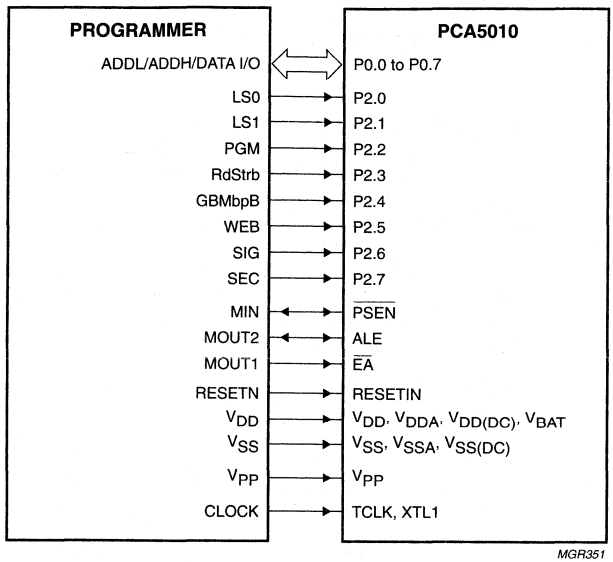


Fig.68 Parallel programming mode.

15.3 Entering the parallel programming mode

The parallel programming mode has been implemented as a general test mode of the PCA5010. This mode can be entered by applying 000 to pins $\overline{PSEN}$, ALE, and $\overline{EA}$ during reset. For the initializing sequence a clock of 76.8 kHz at XTL1 is expected and the supply voltage V_{DD} must be higher then 2.2 V. At the rising edge of $\overline{RESOUT}$ these signals are latched and the code 000 leads to parallel programming mode. The high voltage pin V_{PP} can be either HIGH or V_{DD}.

Since $\overline{PSEN}$ and ALE are output signals of the PCA5010 after reset, a pull-down (strong enough to overdrive the internal 100 µA pull-up of the PCA5010) should be used to drive the outputs LOW. Alternatively the LOW can be driven with a 3-state buffer which is enabled with $\overline{RESOUT}$ = LOW.

The microcontroller fetches instructions from Port 0 in external mode. Data fetching is controlled by $\overline{PSEN}$ and ALE. This is the standard data fetch in external mode. A clock has to be supplied to TCLK while entering the parallel programming mode. Before entering the parallel programming mode, Port 2 should be set to 30H and the microcontroller should be put in Idle mode by setting the bit PCON.0 (address 87H).

The test mode is activated by making $\overline{EA}$ equal to logic 1. The mode entering sequence is given in Table 65.

Before entering the parallel program mode Port 2 can be an output port (dependent on the reset configuration of this port). As soon as the parallel programmed mode is entered Port 2 is an input.

After entering the parallel programming mode this mode has to be initialized. The OTP test latch has to be loaded with code 01H to set the sense amplifiers in verify mode. Before a byte can be programmed a verify has to be performed to check if programming is not blocked by the security (see Section 15.10). The address of this verify cycle is not important and the address latches do not have to be loaded. After this initialization the PCA5010 is ready for programming. Parallel program initialization is shown in Fig.71.

The security check can be replaced by another read action e.g reading the security or signature bytes (see Section 15.9).

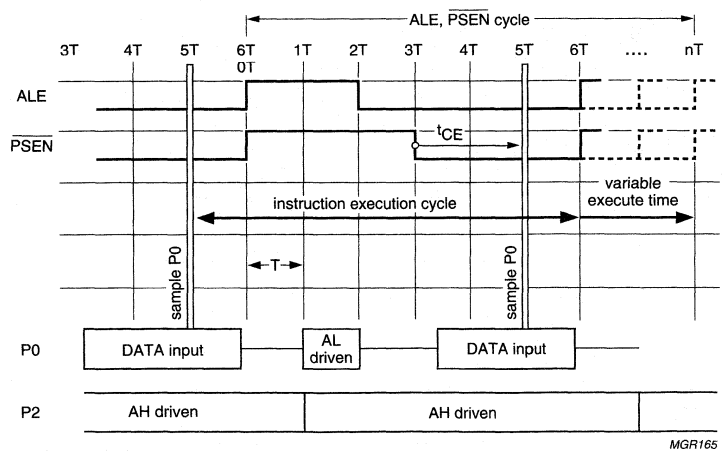
It should be noted that this paragraph is only applicable for the first series. It can be neglected in the future. To prevent problems with the self timed loop it is advised to set the circuit in DC read mode during verify. This is achieved by writing 09H instead of 01H into the OTP test latch.

Table 65 Entering the parallel programming mode; note 1

PINS $\overline{PSEN}$, ALE AND $\overline{EA}$	RESETIN	$\overline{RESOUT}$	PORT 0	DESCRIPTION
000	1	0	xx	reset
000	0	0	xx	259 or more slow clocks at XTL1
000	0	0 → 1	xx	prepare parallel programming mode, enter external access mode, now clocks must be provided on TCLK
zz0	0	1	02	LJMP 3000H
zz0	0	1	30	force P2 to 30H
zz0	0	1	00	
zz0	0	1	00	discard fetch cycle
zz0	0	1	75	MOV PCON, 01H
zz0	0	1	87	make microcontroller idle
zz0	0	1	01	
zz0	0	1	01	discard fetch cycle
zz1	0	1	xx	parallel programming mode active

Note

1. z = pin is output.



T being the half period of the clock signal supplied to TCLK.

The minimum duration of one cycle is 6T. It can be extended by increments of [0 to n]T if the execution of an instruction needs more time (dependant of V_{DD}, T, Temperature, Opcode).

Execution of an op-code goes in parallel with the external access cycle for the next sequential byte. Eventually an already fetched byte is discarded depending on the executed instruction (e.g. any jump or return).

Fig.69 External access timing for programming mode entry.

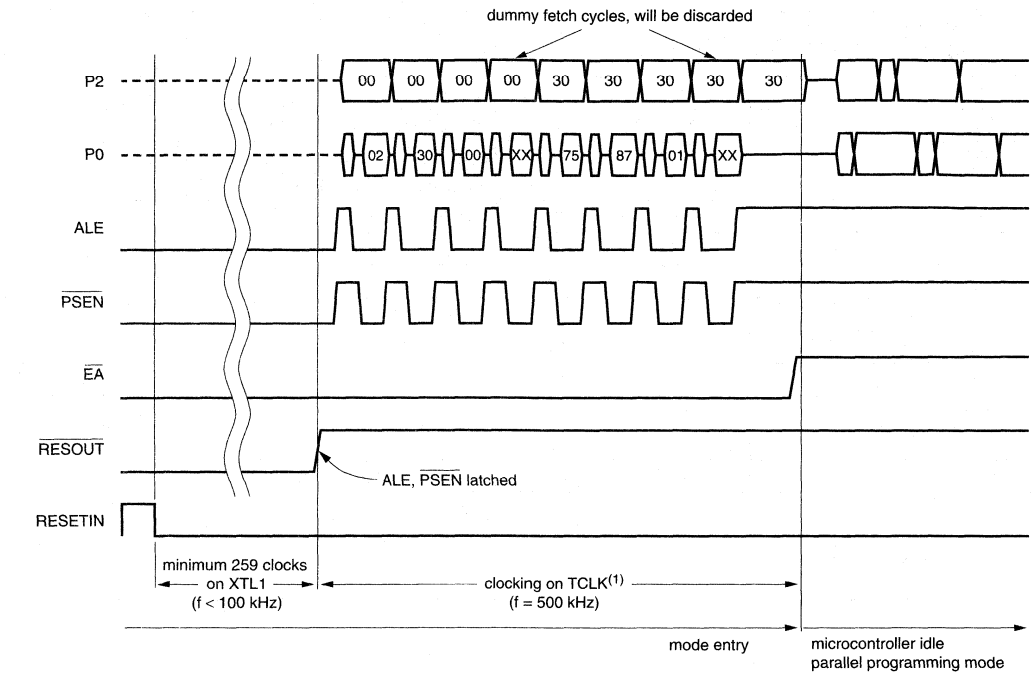


Fig.70 Program mode entry.

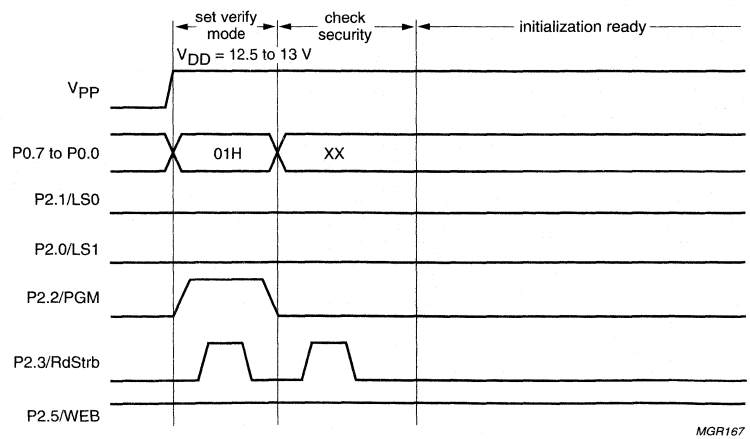


Fig.71 Parallel program mode initialization.

15.4 Address space

The PCA5010 has a 32 kbytes memory and therefore 15 address pins. Applying an address above 32 kbytes (address<15> = 1) leads to the selection of the extra rows. The user should not apply these addresses during programming.

15.5 Single byte programming

Programming and verifying is shown in Fig.72. The upper and lower address byte are loaded one after the other.

The address latch control signals select the proper latch and the RdStrb signal opens the latch (level sensitive). The order of loading the latches is not important. The data is latched if write enable bar becomes active. After programming a byte, this byte can be verified without reloading the addresses. If more bytes are programmed after each other having the same upper address, it is not necessary to reload this upper address.

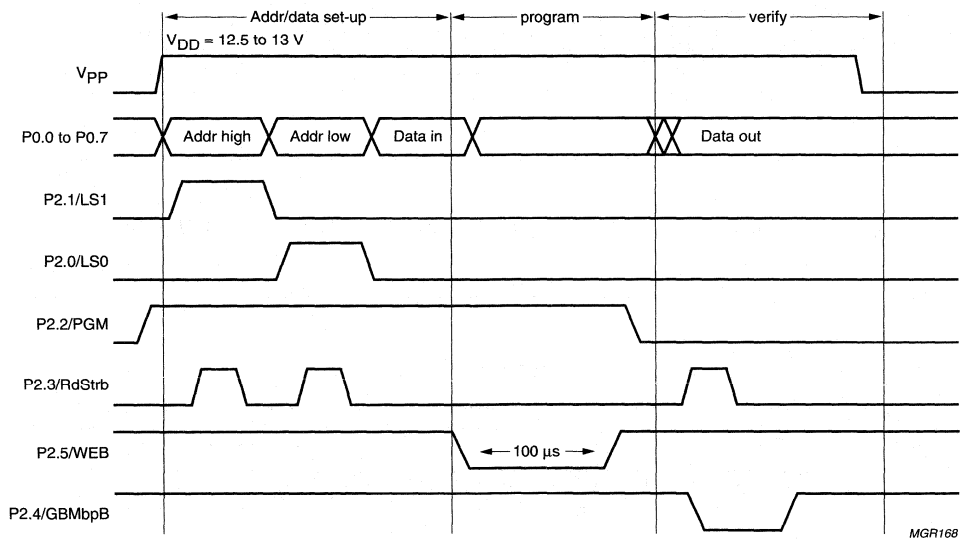


Fig.72 Single byte programming mode.

15.6 Multiple byte programming

A multiple byte programming mode has been implemented to increase programming speed. In this mode four bytes can be programmed in parallel. The addresses of these four bytes have to be equal except for bit 0 and bit 1. Loading the address and data latches is enabled by making PGM HIGH and GBMbpB LOW at the same time. Figure 73 shows the address and data set-up and the program pulse. Loading the upper address is only necessary if it differs from the upper address of the previous quadruple of bytes. In this mode the data latches are controlled by the RdStrb signal (level sensitive). Figure 74 shows the verification in this mode. It should be noted that data 3 is verified before data 0. If this is unwanted the lower address byte of data 0 has to be loaded before verifying data 0 and the lower address byte of data 1 before verifying data 1.

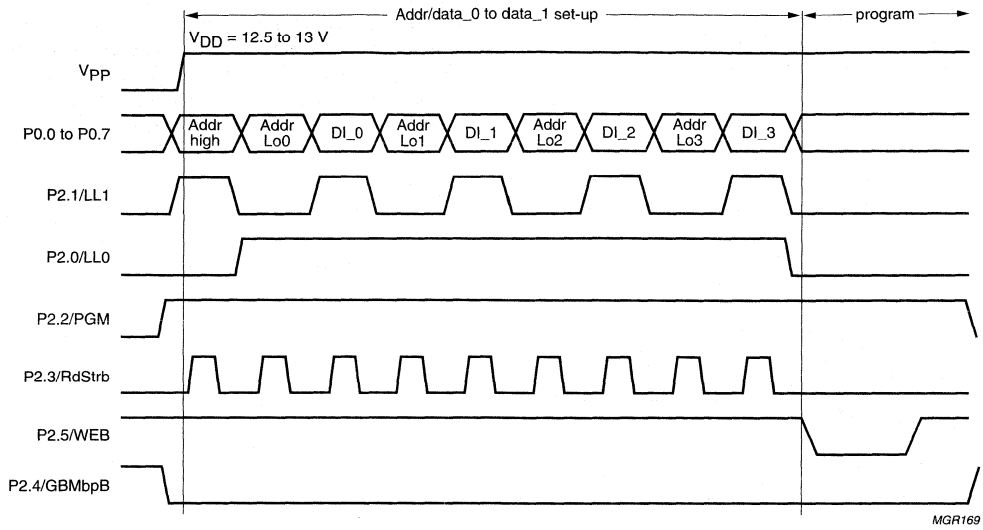


Fig.73 Multiple byte programming mode (address and data load, programming pulse).

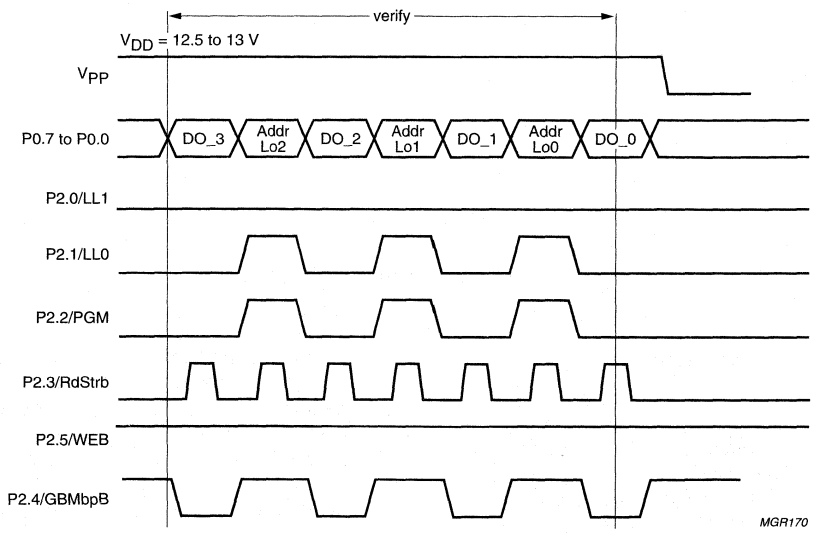


Fig.74 Multiple byte programming mode (verify).

15.7 High voltage timing

The external program voltage V_{PP} has to be HIGH while a program pulse is applied (WEB active). During verify it can be either high or equal to the supply voltage. V_{PP} has to be stable for at least 10 µs before a program pulse can be applied.

After applying a program pulse a recover time of 1 µs is needed to discharge the internal high voltage nodes. During this recover time the memory cannot be accessed for verify.

Due to the above mentioned setup time programming time is reduced if V_{PP} is continuously HIGH during programming and verifying.

15.8 OTP test modes

OTP test modes will be selected from a test control latch which can be loaded in parallel programming over Port 0. The advantage of this is that the test modes of the OTP are independent of the microcontroller. Table 66 shows the OTP test modes coded in 7 bits. When a test mode is loaded the control signals on Port 2 keep their original functionality and can be used to execute the test mode.

Table 66 Definition of test modes

TCL(7 to 0)	TEST MODE
00000000	normal mode (no test active)
XXXXXX01	verify mode (self timed)
XXXXXX10	margin 0 mode
XXXXXX11	margin 1 mode
XXXXX1XX	margin VP mode is active
XXXX1XXX	DC_Read mode is active
X001XXXX	drain stress test mode
X010XXXX	gate stress test mode
X011XXXX	mass programming test mode
X100XXXX	even column test mode
X101XXXX	odd column test mode
X110XXXX	even row test mode
X111XXXX	odd row test mode
1XXXXXXX	OTP interface test

The encoding is such that combinations of test modes are possible, for instance TCB(7 to 0) = 00001100 enables both the margin VP and DC_Read test modes.

The so called vt mode, needed to measure analog cell characteristics, can be entered by making both P2.6/SIG and P2.7/SEC active. During normal programming this mode should not be entered therefore **it is forbidden to make P2.6/SIG and P2.7/SEC HIGH at the same time.**

15.8.1 MASS PROGRAM MODE

The mass program mode can be used to program checker boards. If this mode is active every internal data latch is connected to four bit lines and 128 bits can be programmed in parallel. To write a checker board 0011X0XX has to be loaded in the test register and the circuit has to be set in parallel program mode (P2.2/PGM = 1 and P2.4/GBMbpB = 0). Then data from address 00H is loaded to address 00 03H down to 00 00H. For every even word line (A<6> = 0) a program pulse has to be given at low addresses X0000000 and X0001000. For the odd lines (A<6> = 1) the pulses have to be applied to low address X1000100 and X1001100. In the user address space a checker board can be programmed with 320 × 2 = 640 program pulses.

15.9 Signature bytes

Three signature bytes are available to identify the device. These bytes can be read by doing a verify while the SIG input (Port 2.6) is active. The contents of the signature bytes is given in Table 67. Applying a write pulse while the SIG input is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes are always readable independent on the security.

Table 67 Addresses and contents of the signature bytes

ADDRESS	CONTENTS
00 30H	15H
00 31H	D9H
00 60H	H0h

15.10 Security

To prevent programming or reading of EPROM contents by third parties security can be set by programming the security bits. These bits are located outside the normal memory matrix and have input and output lines separated from the normal OTP I/Os. Three bits are present, but only two are actually used. The third bit can be used for future extensions. Different levels of security can be set by programming one or more bits. The bits are read in parallel at every read cycle and interpreted with the following definition:

- Level 0, bits 000, no security, no restrictions
- Level 1, bits 001, program disabled
- Level 2, bits 011, program and verify disabled.

The third security may be programmed without affecting the functionality. However only the combinations 000, 001, 011 and 111 are possible.

After reset security Level 1 is loaded. To enable programming a read or verify (GB pulse not necessary) is needed to check the actual security level.

The security bits can be programmed the same as normal bits. The bits have to be supplied to the three least significant bits of Port 0.

The SEC bit of Port 2 (bit 7) has to be HIGH during the program cycle. Loading an address is not necessary.

If Port 2.7/SEC is HIGH during verify, the security bits can be read on the three least significant bits of Port 0. After programming 011 to the security bits only the security bits and the signature bytes can be verified and verifying the normal addresses is not possible any more. Verifying a normal address while security Level 2 has been programmed will result in reading 00H.

The programming time for the security bits is 200 μs instead of 100 μs for a normal bit. This extra time can be reached by applying one 200 μs program pulse or by applying two standard pulses.

Although in this OTP an unprogrammed cell is a logic 1 and a programmed cell is a logic 0, a logic 1 has to be programmed to increase the security level. The inversion is performed by the interface block.

Since the security is checked at every read or verify access, verifying is disabled immediately after programming security Level 2. Programming is disabled if a verify or a reset is applied after programming security Level 1 or higher.

16 APPENDIX 3: OS SHEET

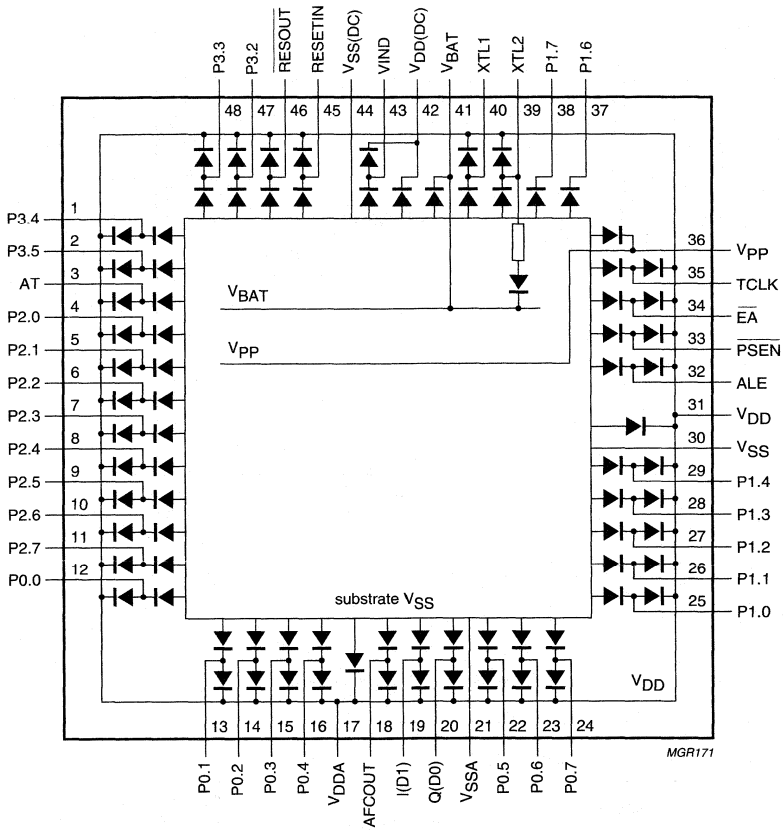


Fig.75 Open/short-circuit diagram for PCA5010.

17 APPENDIX 4: BONDING PAD LOCATIONS

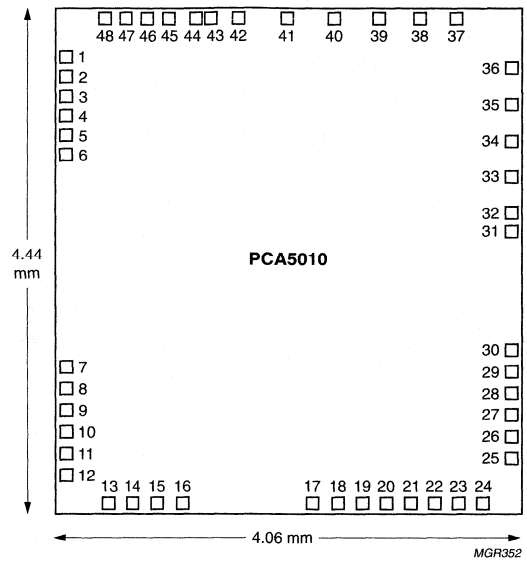


Fig.76 Bonding pad locations.

Table 68 Bonding pad locations (dimensions in μm)

PAD	NAME	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
1	P3.4	91.0	3930.0	87.0
2	P3.5	91.0	3770.0	87.0
3	AT	91.0	3600.0	87.0
4	P2.0	91.0	3430.0	87.0
5	P2.1	91.0	3260.0	87.0
6	P2.2	91.0	3090.0	87.0
7	P2.3	91.0	1240.0	87.0
8	P2.4	91.0	1060.0	87.0
9	P2.5	91.0	880.0	87.0

PAD	NAME	BOND PIN CENTRE x	BOND PIN CENTRE y	PAD SIZE x, y
10	P2.6	91.0	700.0	87.0
11	P2.7	91.0	520.0	87.0
12	P0.0	91.0	340.0	87.0
13	P0.1	420.0	91.0	87.0
14	P0.2	630.0	91.0	87.0
15	P0.3	842.0	91.0	87.0
16	P0.4	1055.0	91.0	87.0
17	V_{DDA}	2170.0	91.0	87.0
18	AFCOUT	2392.5	91.0	87.0
19	I(D1)	2595.0	91.0	87.0
20	Q(D0)	2795.0	91.0	87.0
21	V_{SSA}	2997.5	91.0	87.0
22	P0.5	3195.0	91.0	87.0
23	P0.6	3392.5	91.0	87.0
24	P0.7	3590.0	91.0	87.0
25	P1.0	3827.2	410.0	87.0
26	P1.1	3827.2	620.0	87.0
27	P1.2	3827.2	830.0	87.0
28	P1.3	3827.2	1040.0	87.0
29	P1.4	3827.2	1217.5	87.0
30	V_{SS}	3827.2	1377.5	87.0
31	V_{DD}	3827.2	2417.5	87.0
32	ALE	3827.2	2580.0	87.0
33	$\overline{PSEN}$	3827.2	2890.0	87.0
34	$\overline{EA}$	3827.2	3200.0	87.0
35	TCLK	3827.2	3510.0	87.0
36	V_{PP}	3827.2	3820.0	87.0
37	P1.6	3383.1	4231.5	87.0
38	P1.7	3079.6	4231.5	87.0
39	XTL2	2743.4	4231.5	87.0
40	XTL1	2364.1	4231.5	87.0
41	V_{BAT}	1964.5	4231.5	87.0
42	PowerPads	1550.0	4231.5	84.0
43	PowerPads	1310.0	4231.5	84.0
44	PowerPads	1190.0	4231.5	87.0
45	RESETIN	953.2	4231.5	87.0
46	$\overline{RESOUT}$	766.2	4231.5	87.0
47	P3.2	579.2	4231.5	87.0
48	P3.3	392.2	4231.5	87.0

PCD3316

Caller-ID on Call Waiting (CIDCW) receiver

11 March 1999 **Product specification**

1. General description

The PCD3316 is a low power mixed signal CMOS integrated circuit for receiving physical layer signals like Bellcore's 'CPE[1] Alerting Signal (CAS)' and the signals used in similar services. The device is capable of a very high precision detection of the dual tone (2130 and 2750 Hz) by using a patented digital algorithm. The PCD3316 can be used for on-hook and off-hook Caller-ID (CID), Caller-ID on Call Waiting (CIDCW) and Caller-Name (CNAM) applications.

For timing purposes the PCD3316 can be programmed to generate an interrupt signal to the microcontroller every second or every minute. These timings are derived from an on-chip 32.768 kHz oscillator.

Also incorporated in the device are a Frequency Shift Keying (FSK) receiver/demodulator and a 'Ring or polarity change detector'. The status of the PCD3316, the received FSK data bytes and the ringer period can be read and many options can be selected via the I²C-bus serial interface. Two on-chip oscillators are available. One 3.58 MHz oscillator for all internal functions and a low frequency 32.768 kHz oscillator for the 1 second or 1 minute timing.

In Power-down mode only the polarity comparators and the 32.768 kHz oscillator are active. The CAS detection, the FSK receiver and the 3.58 MHz oscillator can be enabled separately. Detection of a polarity change on the inputs POL0 or POL1, the reception of an FSK data byte, the detection of a CAS tone or a timebase interrupt is signalled to the microcontroller by an interrupt request signal (IRQ). The microcontroller can communicate with the PCD3316 device via the serial interface.

The PCD3316 is designed for use in a microcontroller controlled system. The device is available in a SO16 package.

A demonstration board OM5843 and an application note *AN98071* are available.

1. CPE = Customer Premises Equipment.

2. Features

- Bellcore's 'CPE Alerting Signal (CAS)' and British Telecom's (BT) 'Loop State Tone Alert Signal' detection
- BT's 'Idle State Tone Alert Signal' by means of monitoring the input signal level
- 1200 baud FSK demodulator conform Bell 202 and CCITT V23 standards
- Ring or polarity change detector
- Ring period measurement
- Low battery comparator
- Signal level detector
- On-hook and off-hook applications according to *Bellcore TR-NWT-000030* and *SR-TSV-002476* specifications
- Receive sensitivity of –37.8 dBm (in 600 Ω) for CAS
- 2.5 to 3.6 V supply; low power standby mode
- Selectable 1 second or 1 minute timebase interrupt
- 3.58 MHz and 32.768 kHz crystal oscillators
- SO16 package.

3. Applications

- Analog Display Services Interface (ADSI) phones
- Feature phones and adjunct boxes with Bellcore CID, CIDCW and CNAM systems
- Computer Telephony Integrated (CTI) systems.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCD3316T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5. Block diagram

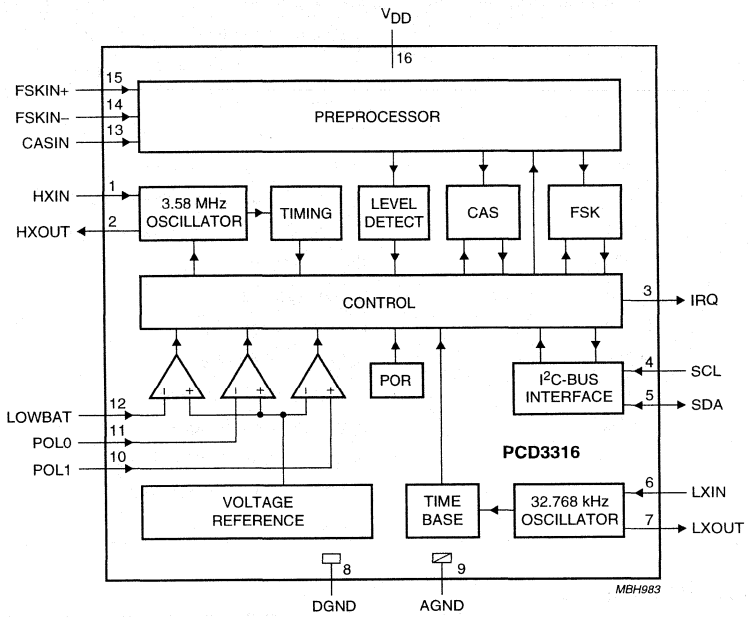


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

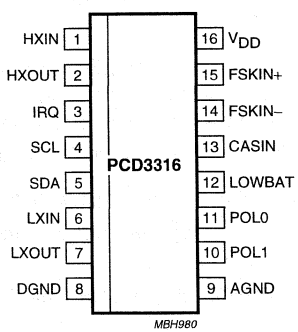


Fig 2. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	I/O	Description
HXIN	1	I	3.58 MHz crystal oscillator input
HXOUT	2	O	3.58 MHz crystal oscillator output
IRQ	3	O	interrupt output; programmable active HIGH or active LOW
SCL	4	I	serial clock line of I^2C-bus
SDA	5	I/O	serial data line of I^2C-bus
LXIN	6	I	32.768 kHz crystal oscillator input
LXOUT	7	O	32.768 kHz crystal oscillator output
DGND	8	–	digital ground
AGND	9	–	analog ground
POL1	10	I	polarity detector input 1
POL0	11	I	polarity detector input 0
LOWBAT	12	I	low battery detector input
CASIN	13	I	input pin for CAS signal
FSKIN–	14	I	negative input for FSK signal
FSKIN+	15	I	positive input for FSK signal
V_{DD}	16	–	supply

7. Functional description

7.1 Preprocessor and analog inputs

The preprocessor for the CAS detection and the FSK receiver incorporates an Analog-to-Digital Converter (ADC) and a digital bandpass filter.

The LOWBAT input of the PCD3316 can be used for low battery detection. The voltage on the LOWBAT pin is compared with an internal voltage reference circuit. When the LOWBAT voltage drops below the reference voltage, the Status register, bit 5 is set to logic 1.

The PCD3316 can be forced in a Power-down state by switching off the 3.58 MHz system clock and the ADC. This is done by setting Mode register 2, bit 7 (CIDMD2.7) to logic 0. To guarantee correct operation the following order of actions must be performed (see also Section 7.8 about interrupts):

1. Switch off CAS and FSK detection (if turned on)
2. Read the interrupt register (thus clearing pending interrupts generated by the CAS and FSK detector)
3. Switch off the 3.58 MHz oscillator by clearing bit 7 of Mode register 2.

The two low power comparators (inputs POL0 and POL1) and the 32.768 kHz clock are always active.

They can be used for ring or line polarity reversal detection. The POL on/off bit (Mode register 1, bit 4) must be set to enable generation of an interrupt when a polarity change occurs. The result of the two comparators can be read in bits 7 and 6 (POL0 and POL1) of the Status register (see Section 7.4). The 3.58 MHz clock is not needed for the generation of a polarity interrupt.

7.2 CAS detection

After a power-on reset or after enabling the CAS detector the internal registers of the CAS detection function are initialized. The initialization takes a maximum of 100 periods of the 3.58 MHz clock.

If the CAS detection is enabled the PCD3316 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected. Interrupts will be blocked when the signal level on the CAS input is below the threshold in the level detector.

7.3 FSK reception

The FSK receiver function can be enabled by setting the FSK on/off bit (Mode register 1, bit 7).

In the FSK transmission specification of BT and Bellcore a channel seizure is transmitted first (sequence of 1010..). After the channel seizure a block of marks and finally the data pattern are sent (see Figure 3). These mark bits are detected by the PCD3316 which sets the FSK-BOM Indication bit (Status register, bit 4). The FSK-BOM Indication bit is reset when the FSK receiver is disabled.

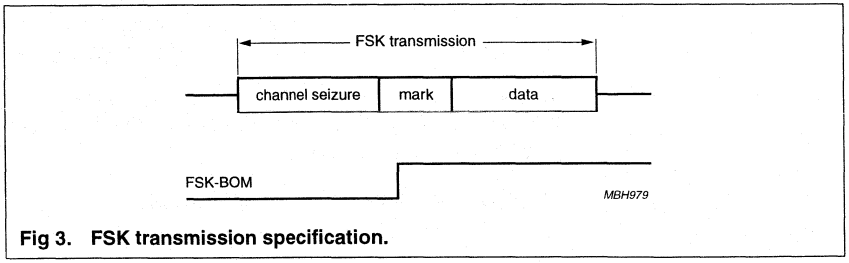


Fig 3. FSK transmission specification.

If the FSK-BOM Indication bit is set, the FSK receiver will generate an interrupt after it has received a complete data word. An FSK data word consists of one start bit (space), followed by eight data bits and one stop bit (mark). Interrupts will therefore not be generated during the channel seizure and during the block of marks. When a valid data word has been received, FSK data is available in the FSK data register.

By clearing the FSK-BOM-mask on/off bit (Mode register 1, bit 6), the FSK receiver will not wait with the generation of interrupts until a Begin Of Mark (BOM) has been detected but will handle the channel seizure as normal data. The block of marks which is a string of logic 1 will still not generate interrupts because there are no start bits.

After the generation of an interrupt the IRQ pin will become active (see Figure 4), and the FSK Interrupt bit is set (Interrupt register, bit 5). The received data is available in the FSK data register.

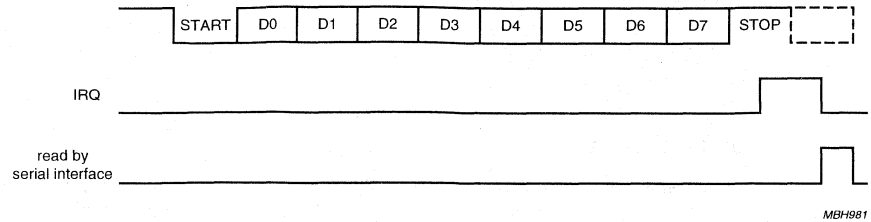


Fig 4. IRQ generation after reading a valid data byte.

The FSK-OVR Error bit (Status register, bit 3) indicates that a previous byte is lost due to an overrun. The FSK-FRM Error bit (Status register, bit 2) indicates an incorrect start- or stop-bit. These frame errors indicate that there are synchronization problems. The on-chip level detector can be used to detect a carrier loss during FSK transmission. FSK data can be rejected when the signal level is below the reference level, this to avoid that noise is interpreted as data (Interrupt register, bit 4 is logic 1).

7.4 Ring or polarity change detector

For ring and polarity change detection two comparators are available in the PCD3316. The reference level of the comparators is set internally by the reference voltage generator. The voltage levels on the two polarity comparator inputs, POL0 and POL1, are compared with the reference voltage V_{ref}. If POL0 < V_{ref} or POL1 > V_{ref}, POL0 and POL1 (Status register, bit 7 and 6) are set respectively and reset if POL0 > V_{ref} and POL1 < V_{ref}. Every time the POL0 status bit changes from logic 1 to logic 0, a POL0 interrupt is generated. Every time the POL1 status bit changes from logic 0 to logic 1, a POL1 interrupt is generated.

The period time of a POL1-POL0-POL1 sequence is available in the Ringer period register. It is preset to 255 on power-on and updated every time a POL1 interrupt is generated. The sequence is:

1. Power-on: Ringer period register = 255
2. First POL1 interrupt: Ringer period register = 255
3. First POL1 interrupt after a POL0 interrupt: Ringer period register = new time
4. First POL1 interrupt after more than $^{255}/_{2048}$ s: Ringer period register = 255.

The period is given in multiples of $^{1}/_{2048}$ s. The maximum value is 255.

The POL1-POL0-POL1 sequence is recognized when one or more POL1 interrupts are generated followed by one or more POL0 interrupts, followed by a POL1 interrupt. The 32.768 kHz clock is needed for the generation of a polarity interrupt.

7.5 Low battery detection

The low battery voltage detection input (pin LOWBAT) is connected to the positive input of a comparator. The negative input is connected to the internal reference voltage. If the voltage on the LOWBAT input pin is less than the reference voltage V_{ref}, the LOW-BAT Indication (Status register, bit 5) is set. If the LOWBAT input rises above V_{ref} again, the LOW-BAT Indication is cleared.

The 32.768 kHz clock signal must be available. The LOW-BAT Indication bit does not generate interrupts, thus the bit should be polled.

7.6 Level detect

When the input signal level on the FSK or the CAS input (the one that is selected) is below a threshold of typically –40 dBm, the Low Level Status bit will be set (Interrupt register, bit 4). The level detector can be used to observe a carrier loss during FSK transmission and to detect the 'Idle State Tone Alert Signal' for British Telecom. The signal power on the input can be monitored by polling the register bit since it will not generate an interrupt. Signal power is measured in a frequency band corresponding to the selected operation mode, FSK (1000 to 2200 Hz) or CAS (2000 to 2800 Hz).

The Low Level Status bit will be updated every 8 ms. When FSK and CAS are both disabled the signal level on the FSK input is measured. The 32.768 kHz clock signal must be available.

7.7 Time base

The 32.768 kHz oscillator is used to generate either a 1 second or a 1 minute interrupt signal. If the TB on/off bit is set (Mode register 2, bit 6) every second or minute an interrupt is generated and MIN Interrupt and/or SEC Interrupt bits (Interrupt register, bit 7 and 6) are set. After reading the Interrupt register the interrupt is cleared.

The SEC/MIN (Mode register 2, bit 5) selects whether every second (SEC/MIN is set) or every minute (SEC/MIN is cleared) an interrupt is generated. All possible selections are shown in Table 3. Resetting bit TB on/off in Mode register 2 (bit 6) will only disable time base interrupts, and the 32.768 kHz oscillator will continue to run.

7.8 Interrupt

The interrupt request output (IRQ) is active HIGH by default. The polarity of the IRQ output can be made active LOW by the INT Polarity HIGH/LOW bit (Mode register 1, bit 3). The IRQ pin is in 3-state when not active, so an external pull-up or pull-down resistor is required. The interrupt cause is indicated by the flags in the Interrupt register. Interrupt flags are set by hardware but must be reset by software. All flags of the Interrupt register are reset when the register is read via I^2C-bus interface.

The IRQ pin is deactivated at the positive edge of SCL which reads the first data bit of the Interrupt register. The IRQ pin will stay inactive for one SCL cycle. IRQ can handle a next interrupt after the next positive edge of SCL.

Table 3: Selection of interrupt modes

Mode register 2 (CIDMD2)		Interrupt register (CIDINT)		Interrupt
TB on/off (CIDMD2.6)	SEC/MIN (CIDMD2.5)	MIN Interrupt (CIDINT.7)	SEC Interrupt (CIDINT.6)	
0	X[1]	0	0	no time base interrupt (time base is reset)
1	0	1	0	every minute an interrupt is generated; no second interrupt
1	1	1	1	every second an interrupt is generated; every minute an interrupt is generated

[1] X = don't care.

7.9 The internal Power-on reset (POR)

The device contains an on-chip Power-on reset circuitry which activates a reset as long as V_{DD} is below a predefined level $V_{POR(H)}$. If V_{DD} exceeds $V_{POR(H)}$, the 3.58 MHz oscillator will start. The PCD3316 is initialized and the internal registers are set to the default value (see Section 7.13). It takes a maximum of 100 cycles of the 3.58 MHz clock to initialize all internal functions. The POR circuitry also ensures, that the chip will be switched off as soon as a falling V_{DD} reaches a predefined level ($V_{POR(L)}$).

7.10 3.58 MHz oscillator circuitry

The 3.58 MHz oscillator is needed for the FSK receiver and the CAS detection. This on-chip Amplitude Controlled Oscillator (ACO) circuitry is a single-stage inverting amplifier biased by an internal feedback resistor R_{fb}. The oscillator circuit is shown in Figure 5. When using a quartz resonator to drive the oscillator, normally no external components are needed.

When using ceramic resonators to drive the oscillator, in some cases external components are needed; refer to the ceramic resonator product specifications. Two different configurations are shown in Figure 6a and Figure 6b.

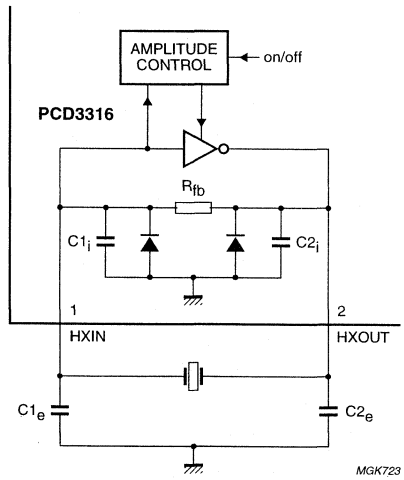
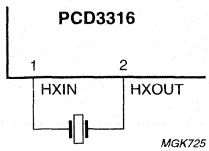


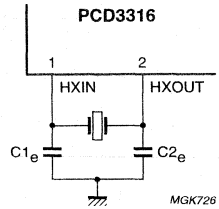
Fig 5. Oscillator.

To drive the device with an external clock source, apply the external clock signal to HXIN, and leave HXOUT to float, as shown in Figure 6c. If the amplitude of the input signal is less than V_{DD} to DGND or a sine wave is applied, capacitive decoupling is needed as shown in Figure 6d.

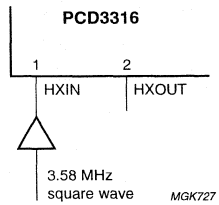
In the Power-down mode (Mode register 2, bit 7 = 0), the oscillator is stopped and HXIN and HXOUT are internally pulled LOW. The current of the whole oscillator is switched off.



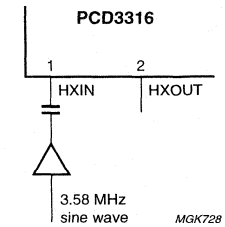
a. Standard oscillator: quartz or PXE.



b. Oscillator: quartz or PXE with external capacitors.

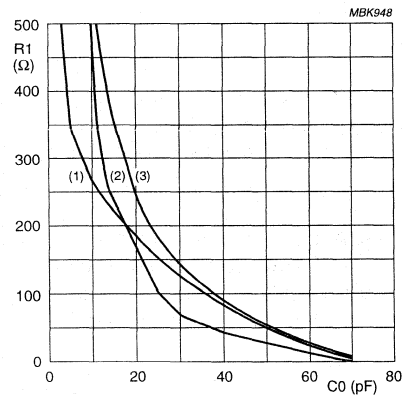


c. External clock: square wave.



d. External clock: sine wave.

Fig 6. 3.58 MHz oscillator configurations.



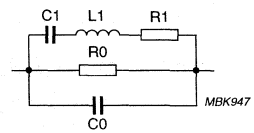
$C1_e$ and $C2_e$ are the external load capacitances (see Figure 6b). Normally, they are not needed due to integrated load capacitances of 10 pF; see curve (2).

(1) $C1_e = C2_e = 22$ pF.

(2) $C1_e = C2_e = 0$ pF.

(3) $C1_e = C2_e = 12$ pF.

a. Resonator requirements for the ACO.



For correct function of the oscillator, the values of R1 and C0 of the chosen resonator (quartz or PXE) must be below the related curve lines shown in Figure 7a. The value of the parallel resistor R0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

b. Resonator equivalent circuit.

Fig 7. Resonator requirements and equivalent circuit.

7.11 32 kHz oscillator

The 32.768 kHz oscillator is enabled permanently and is used to generate either a 1 second or 1 minute interrupt. The 32.768 kHz clock is also used for the 'Ring or polarity change detector', the 'Low battery detection' and the 'Level detect' function.

An external 32.768 kHz signal may be applied to pin LXIN while leaving pin LXOUT not connected.

The 32 kHz oscillator requires an external 32.768 kHz quartz crystal and an external feedback resistor (4.7 MΩ) between the LXIN and LXOUT pins (see Figure 8).

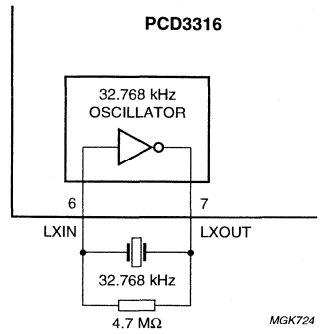


Fig 8. Connections of the 32 kHz oscillator.

7.12 Serial interface

The serial interface of the PCD3316 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I²C-bus and how to use it*, order no. 9398 393 40011 or *I²C Peripherals Data Handbook IC12*.

7.12.1 Characteristics of the I²C-bus

For the I²C-bus configuration see Figure 9. A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are called the 'slaves'. The PCD3316 operates in the slave transmitter/receiver mode only.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

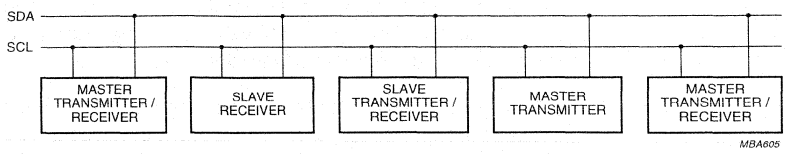


Fig 9. I²C-bus configuration.

7.12.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P); see Figure 10.

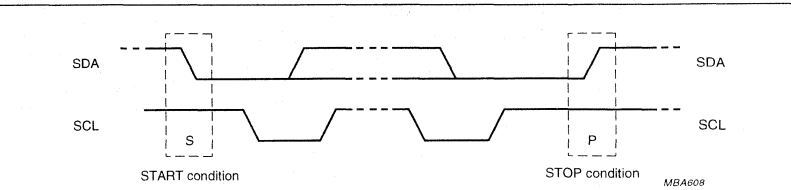


Fig 10. START and STOP conditions for the I²C-bus.

7.12.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 11.

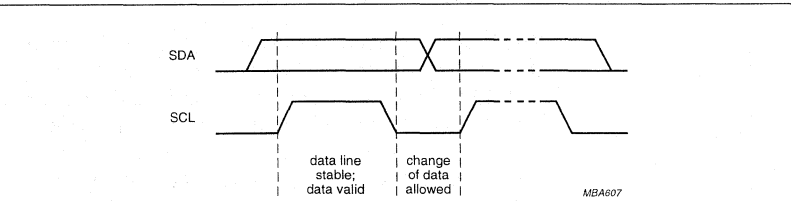


Fig 11. I²C-bus bit transfer.

7.12.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock period immediately after the 8th SCL pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

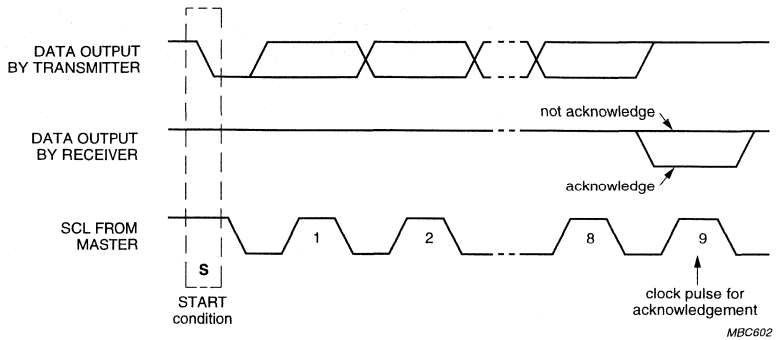


Fig 12. I²C-bus acknowledge.

7.12.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with first byte transmitted after the START procedure. One I²C-bus slave address is reserved for the PCD3316, E0H (1110 0000 for write and 1110 0001 for read).

The I²C-bus protocol is shown in Figure 13. Two different sequences are considered, the write sequence and the read sequence. Both sequences are initiated with a START condition (S) from the I²C-bus master which is followed by the PCD3316 slave address with the read bit cleared. The first byte after the I²C-bus address is interpreted as the address of a PCD3316 register.During the write sequence the register address of the PCD3316 is auto-incremented on each acknowledge. The write sequence is ended with a STOP condition from the master. If the addressed register is read-only or non-existent, nothing will be changed.

For the read sequence the bus master issues a repeated START condition followed by the PCD3316 slave address with the read bit set. Then data is read from previously set address and sent out. When the master responds with an acknowledge the address of the register is auto incremented and the slave will put the data from the next register on the bus. The read sequence is stopped when the master stops giving an acknowledge and generates a STOP condition.

When a non-existing register is addressed the PCD3316 will return FFH. Existing register addresses are shown in Section 7.13. An additional register address (73H) is reserved for test purposes. This address cannot be reached with the auto-increment function of the I²C-bus interface.

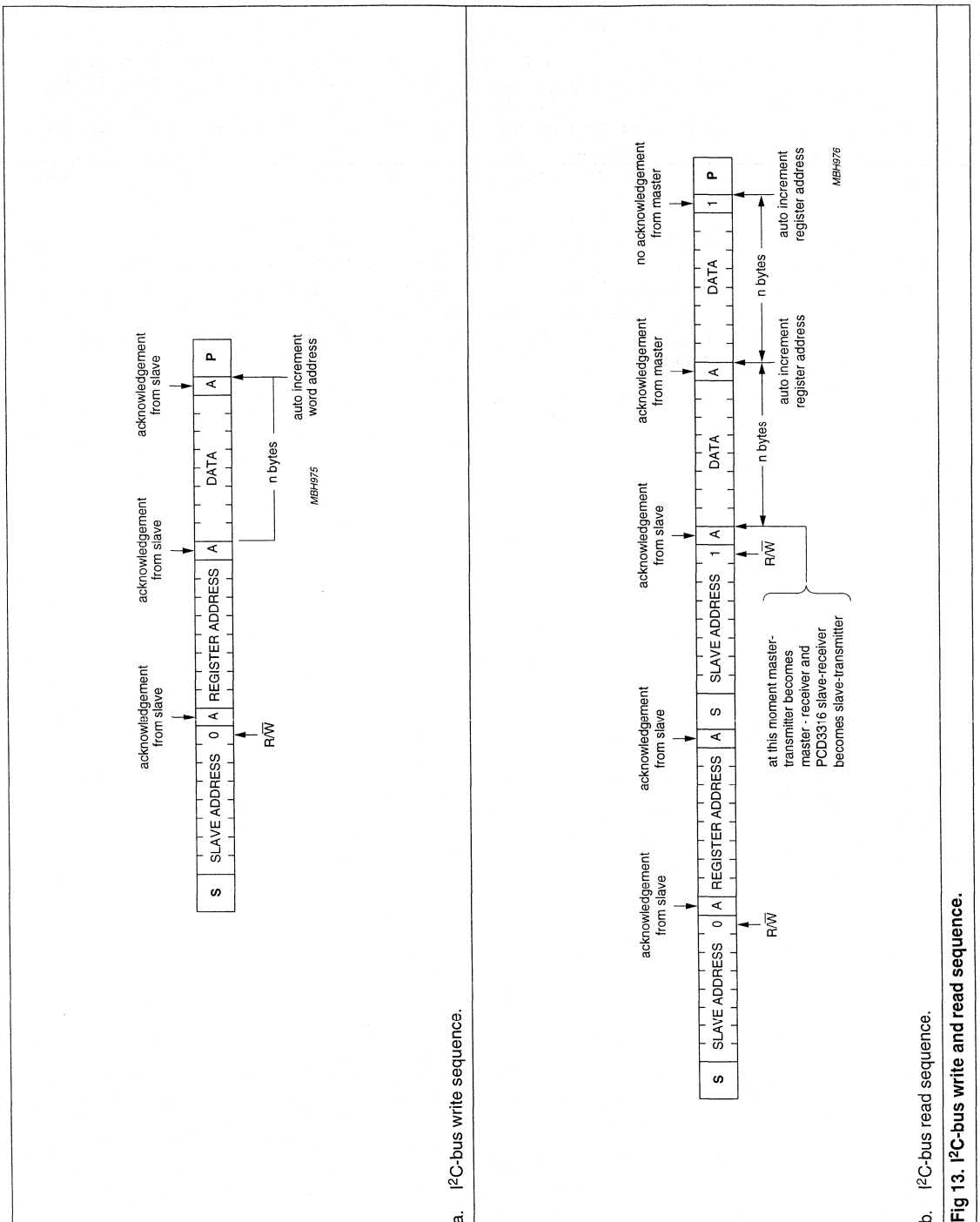


Fig 13. I²C-bus write and read sequence.

7.12.6 I²C-bus bit rate

When a microcontroller is used that implements an I²C-bus in software, the bit rate of the I²C-bus can be critical during reception of FSK. The collection of the interrupt data and FSK-data from the PCD3316 takes 48 bits on the I²C-bus. With an FSK baud rate of 1200 (corresponds to 1200 bits per second) the minimal speed of the I²C-bus should be 5.76 kbits/s. Additional interrupts generated by the time base of the PCD3316 will cause the processor to collect extra information from the PCD3316.

As a consequence, the FSK-data can be overrun in the PCD3316 and one data byte will be lost. In this case, the time base interrupt should be suppressed while FSK is active. This can be done by setting the 'INT-SUP on/off' bit (bit 4 in Mode register 2). The 'TB on/off' bit (bit 6 in Mode register 2) will still be set but the IRQ output will not be activated by the time base interrupt. Any time base interrupt can be detected by the microcontroller when an FSK interrupt is processed by reading the Interrupt register.

7.13 Registers

Table 4: Register overview

Address	Name	Function	Read/Write	Default value
00H	CIDINT	Interrupt register	read only	0000 0000
01H	CIDFSK	FSK data register	read only	–
02H	CIDSTA	Status register	read only	–
03H	CIDRNG	Ringer period register	read only	–
04H	CIDMD1	Mode register 1	read/write	0101 1000
05H	CIDMD2	Mode register 2	read/write	1101 0000

7.13.1 Interrupt register (CIDINT)

Table 5: Interrupt register

Address: 00H; read only.

7	6	5	4	3	2	1	0
MIN Interrupt	SEC Interrupt	FSK Interrupt	Low Level Status	POL1 Interrupt	POL0 Interrupt	CAS Interrupt	–

Table 6: Description of CIDINT bits

Bit	Symbol	Description
CIDINT.7	MIN Interrupt	MIN Interrupt = 0: no interrupt request; MIN Interrupt = 1: one minute interrupt request
CIDINT.6	SEC Interrupt	SEC Interrupt = 0: no interrupt request; SEC Interrupt = 1: one second interrupt request
CIDINT.5	FSK Interrupt	FSK Interrupt = 0: no FSK interrupt or FSK disabled; FSK Interrupt = 1: FSK interrupt, one byte received
CIDINT.4	Low Level Status	Low Level Status = 0: signal level on selected input above power reference (no interrupt); Low Level Status = 1: signal level on selected input below power reference (no interrupt)
CIDINT.3	POL1 Interrupt	POL1 Interrupt = 0: no zero to one changes on POL1 input or polarity interrupt disabled; POL1 Interrupt = 1: a one to zero input change on the POL1 input is detected
CIDINT.2	POL0 Interrupt	POL0 Interrupt = 0: no one to zero changes on POL0 input or polarity interrupt disabled; POL0 Interrupt = 1: a zero to one input change on the POL0 input is detected
CIDINT.1	CAS Interrupt	CAS Interrupt = 0: no CAS signal detected or CAS disabled; CAS Interrupt = 1: CAS signal detected
CIDINT.0	–	reserved bit

7.13.2 FSK data register (CDFSK)

Table 7: Interrupt register

Address: 01H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 8: Description of CDFSK bits

Bit	Symbol	Description
CDFSK.7 to CDFSK.0	D7 to D0	If an FSK interrupt has occurred and no FSK error is detected, the FSK data register contains valid data.

7.13.3 Status register (CIDSTA)

Table 9: Status register

Address: 02H; read only.

7	6	5	4	3	2	1	0
POL1	POL0	LOW-BAT Indication	FSK-BOM Indication	FSK-OVR Error	FSK-FRM Error	–	–

Table 10: Description of CIDSTA bits

Bit	Symbol	Description
CIDSTA.7	POL1	POL1 = 0: voltage on input POL1 < V_{ref}; POL1 = 1: voltage on input POL1 > V_{ref}
CIDSTA.6	POL0	POL0 = 0: voltage on input POL0 > V_{ref}; POL0 = 1: voltage on input POL0 < V_{ref}
CIDSTA.5	LOW-BAT Indication	LOW-BAT Indication = 0: voltage on input LOWBAT > V_{ref}; LOW-BAT Indication = 1: voltage on input LOWBAT < V_{ref}
CIDSTA.4	FSK-BOM Indication	FSK-BOM Indication = 0: begin of mark period not yet detected; FSK-BOM Indication = 1: begin of mark period detected
CIDSTA.3	FSK-OVR Error	FSK-OVR Error = 0: no FSK overrun error; FSK-OVR Error = 1: FSK overrun error, data byte(s) lost
CIDSTA.2	FSK-FRM Error	FSK-FRM Error = 0: no FSK frame error; FSK-FRM Error = 1: FSK frame error, stop bit was wrong
CIDSTA.1 and CIDSTA.0	–	reserved bits

7.13.4 Ringer period register (CIDRNG)

Table 11: Register format

Address: 03H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 12: Description of CIDRNG bits

Bit	Symbol	Description
CIDRNG.7 to CIDRNG.0	D7 to D0	The value held in this byte denotes the time between two positive edges of the POL1 comparator output (between two positive edges of POL1 one positive edge of POL0 must have been detected).

7.13.5 Mode register 1 (CIDMD1)

Table 13: Mode register 1
Address: 04H; read/write.

7	6	5	4	3	2	1	0
FSK on/off	FSK-BOM-mask on/off	CAS on/off	POL on/off	INT polarity HIGH/LOW	–	–	–

Table 14: Description of CIDMD1 bits

Bit	Symbol	Description
CIDMD1.7	FSK on/off	FSK on/off = 0: FSK receiver disabled; FSK on/off = 1: FSK receiver enabled
CIDMD1.6	FSK-BOM-mask on/off	FSK-BOM-mask on/off = 0: FSK interrupts will be generated when a data word was received even before mark period (data from channel seizure); FSK-BOM-mask on/off = 1: FSK interrupts will only be generated after the mark period was detected (no interrupts from channel seizure)
CIDMD1.5	CAS on/off	CAS on/off = 0: CAS detector disabled; CAS on/off = 1: CAS detector enabled
CIDMD1.4	POL on/off	POL on/off = 0: disable interrupts due to polarity change; POL on/off = 1: enable interrupts due to polarity change
CIDMD1.3	INT polarity HIGH/LOW	INT polarity HIGH/LOW = 0: interrupt pin active LOW; INT polarity HIGH/LOW = 1: interrupt pin active HIGH
CIDMD1.2 to CIDMD1.0	–	reserved bits

7.13.6 Mode register 2 (CIDMD2)

Table 15: Mode register 2
Address: 05H; read/write.

7	6	5	4	3	2	1	0
XTAL on/off	TB on/off	SEC/MIN	INT-SUP on/off	–	–	–	–

Table 16: Description of CIDMD2 bits

Bit	Symbol	Description
CIDMD2.7	XTAL on/off	XTAL on/off = 0: disable 3.58 MHz oscillator; XTAL on/off = 1: enable 3.58 MHz oscillator
CIDMD2.6	TB on/off	TB on/off = 0: disable 32.768 kHz timebase; TB on/off = 1: enable 32.768 kHz timebase
CIDMD2.5	SEC/MIN	SEC/MIN = 0: every minute a timebase interrupt; SEC/MIN = 1: every second a timebase interrupt
CIDMD2.4	INT-SUP on/off	INT-SUP on/off = 0: enable SEC/MIN interrupts during FSK reception; INT-SUP on/off = 1: disable SEC/MIN interrupts during FSK reception
CIDMD2.3 to CIDMD2.0	–	reserved bits

8. Limiting values

Table 17: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current at any input		−10	+10	mA
I_O	DC output current at any output		−10	+10	mA
V_I	input voltage on all inputs		−0.5	V_{DD} + 0.5 [1]	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−65	+150	°C

[1] $V_{I(max)}$ = 5.0 V.

9. Characteristics

Table 18: Characteristics

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage		[1]	2.5	3.3	3.6	V
$V_{POR(H)}$	power-on reset HIGH voltage			1.85	2.05	2.25	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		[2]	50	100	150	mV
I_{DD}	supply currents	V_{DD} = 2.5 V					
	Power-down mode		[3]	–	30	70	µA
	operating		[3] [4]	–	2.0	2.3	mA
Low voltage and polarity comparators (pins LOWBAT, POL0 and POL1)							
V_{hys}	hysteresis voltage			–	20	–	mV
I_{LI}	input leakage current		[5]	–	–	1	µA
Internal reference							
V_{ref}	reference voltage level			1.125	1.25	1.375	V
$P_{i(ref)}$	input signal reference power for Low Level Status bit	in 600 Ω load	[6]	−43.8	–	−37.8	dBm
$t_{r(level)}$	input signal to Low Level Status bit rise time	input signal power < $P_{i(ref)}$		–	–	8	ms
$t_{f(level)}$	input signal to Low Level Status bit fall time	input signal power > $P_{i(ref)}$		–	–	8	ms
Logical output (pin IRQ) [7]							
I_{OL}	LOW-level output current	V_{IRQ} = 0.4 V		2	–	–	mA
I_{OH}	HIGH-level output current	V_{IRQ} = V_{DD} − 0.4 V		2	–	–	mA

Table 18: Characteristics...*continued*

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
FSK receiver (pins FSKIN+ and FSKIN−)							
Z_i	input impedance FSKIN+ to FSKIN−			–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance			–	–	200	kΩ
$P_{i(FSKIN)}$	input signal power	in 600 Ω load	[8]	−50	–	0	dBm
S/N_{FSK}	signal-to-noise ratio	200 to 3400 Hz		20	–	–	dB
$\|V_{dif}\|$	differential voltage between mark and space (twist)			–	–	10	dB
$f_{(D)}$	data transmission rate frequency			1180	1200	1212	bits/s
f_s	space frequency			2068	–	2222	Hz
f_m	mark frequency			1188	–	1320	Hz
CAS detector (pin CASIN)							
Z_i	input impedance CASIN to V_{ref}			–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance			–	–	200	kΩ
P_i	input signal power	in 600 Ω load	[8]	−37.8	–	0	dBm
$TH_{ns(CAS)}$	no signal threshold (CAS)	in 600 Ω load		−43.8	–	−37.8	dBm
f_l	low tone frequency			–	2130	–	Hz
f_h	high tone frequency			–	2750	–	Hz
Δf_{max}	maximum frequency deviation		[9]	−0.5	–	+0.5	%
V_{dif}	differential voltage level (twist)		[9]	–	–	6	dB
t_{dt}	dual tone detection time			60	–	–	ms
I^2C-bus interface (pins SCL and SDA)[10]; see Figure 14							
V_{IL}	LOW-level input voltage		[11]	0	–	$0.3V_{DD}$	V
V_{iH}	HIGH-level input voltage		[11]	$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current for pin SDA	$V_{O(SDA)}$ = 0.4 V		2	–	–	mA
C_i	input capacitance for each I/O pin			–	–	10	pF
f_{SCL}	SCL clock frequency			–	–	100	kHz
t_{BUF}	bus free time			4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time			4.7	–	–	µs
$t_{HD;STA}$	START condition hold time			4.0	–	–	µs
t_{LOW}	SCL LOW time			4.7	–	–	µs
t_{HIGH}	SCL HIGH time			4.0	–	–	µs
t_r	maximum SCL and SDA rise time		[12]	–	–	1000	ns
t_f	maximum SCL and SDA fall time		[12]	–	–	300	ns
$t_{SU;DAT}$	data set-up time			250	–	–	ns
$t_{HD;DAT}$	data hold time			0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid time			–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time			4.0	–	–	µs

Table 18: Characteristics...*continued*

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3.58 MHz oscillator (pins HXIN and HXOUT)						
$V_{HXIN(p-p)}$	external clock signal amplitude (peak-to-peak value) on pin HXIN		0.5	–	V_{DD}	V
$Z_{i(HXIN)}$	input impedance on pin HXIN		300	1000	–	kΩ
$C1_i$; $C2_i$	input capacitance on pins HXIN and HXOUT [13]		–	10	–	pF
32 kHz oscillator (pins LXIN and LXOUT)						
g_m	transconductance	$V_{i(p-p)}$ < 50 mV	2	4	10	µS
$C_{i(LXIN)}$	LXIN input capacitance		–	13	–	pF
$C_{o(LXOUT)}$	LXOUT output capacitance		–	10	–	pF

[1] Except for FSK and CAS detection, all circuitry works already when $V_{DD} > V_{POR(H)}$. Since the I²C-bus interface will work (starts to acknowledge), the application can start reading the LOW-BAT Indication bit (Status register, bit 5) to check whether the supply voltage has reached the operating voltage level. A voltage divider network can be connected to pins V_{DD}, LOWBAT and AGND/DGND such that $V_{LOWBAT} = V_{ref}$ if $V_{DD} = V_{DD(min)}$.

[2] The power-on reset LOW level is defined as $V_{POR(L)} = V_{POR(H)} - V_{hys(POR)}$. By design $V_{POR(L)}$ is always lower than $V_{POR(H)}$.

[3] 32 kHz oscillator on (MIN Interrupt, SEC Interrupt, Polarity change, Low battery and Level detect available).

[4] 3.58 MHz oscillator on (device fully operational).

[5] $GND < V_I < V_{DD}$. The leakage currents are generally very small, <1 nA. The value given here, 1 µA, is a maximum that can occur after an Electrostatic Stress on the pin.

[6] When FSK is selected the signal power is measured between 1000 and 2200 Hz. When CAS is selected signal levels are measured between 2000 and 2800 Hz.

[7] The IRQ pin is implemented as a 3-state pin which is only active (either HIGH or LOW) when an interrupt occurs. A pull-up or pull-down has to be connected to define the line when no interrupt is generated.

[8] Verified on sampling basis.

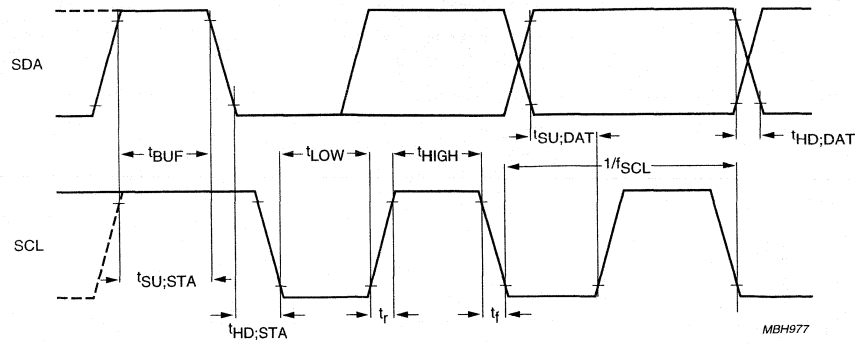
[9] According to Bellcore specification: near end speech level ≤ −7 dBm ASL (ASL = Active Speech Level), referenced to 600 Ω, according to method B of recommendation P.56.

[10] Pins SCL and SDA are equipped with an open-drain output buffer. The pins have no clamp diode to V_{DD}.

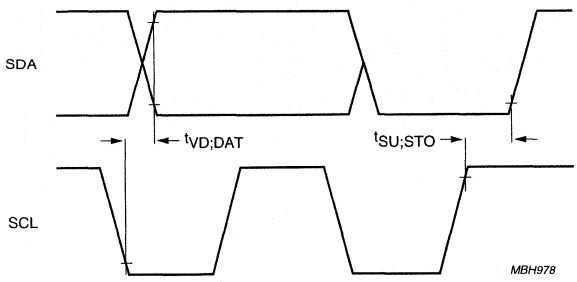
[11] The input threshold voltage of SCL and SDA meet the I²C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1

[12] Maximum capacitive load for each bus line is 400 pF.

[13] $C1_i$ and $C2_i$ are the total internal capacitances (including gate capacitance and leadframe capacitance).



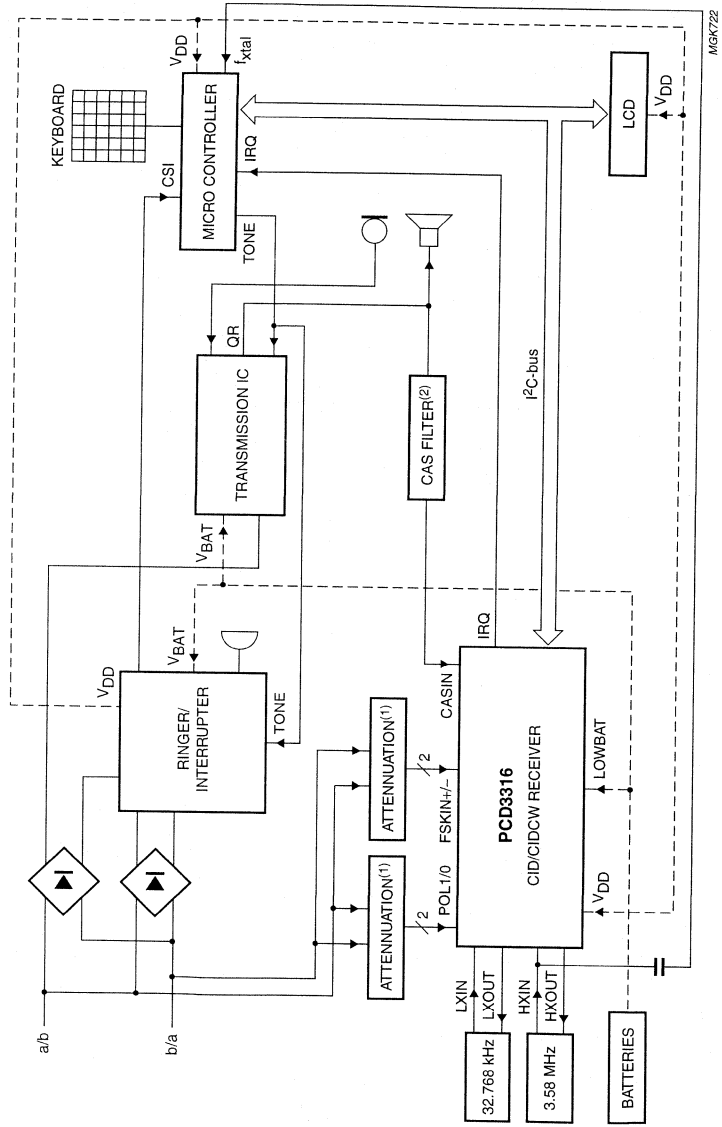
a. Timing diagram 1.



b. Timing diagram 2.

Fig 14. I²C-bus timing.

10. Application information

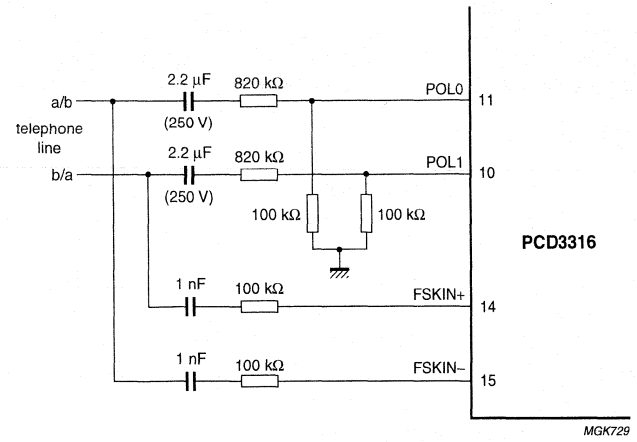


A demo-board (OM5843) of this configuration is available. Please contact your Philips sales office.

(1) See Figure 16a.

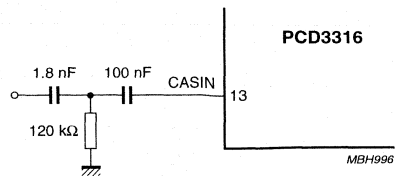
(2) See Figure 16b.

Fig 15. Application diagram for a telephone with CID/CIDCW functionality.



Attenuation networks to connect the polarity and FSK inputs to the telephone line.

a. Attenuation networks.



High-pass filter (cut-off frequency ≈ 1 kHz) to improve performance of CAS detection.

b. High-pass filter.

Fig 16. Application diagrams.

11. Test information

11.1 Application note on Customer Premises Equipment (CPE) testing

Under certain circumstances, some external CIDCW test equipment may generate incorrect pulses after the ringing signal becomes inactive. These pulses may cause the FSK detector of the PCD3316 to respond. Note that this is by no means an incorrect behaviour of the PCD3316 chip, but a correct detection of incorrect test stimuli. However, if not known, it may lead to confusing results during testing of the CPE.

To avoid the issue described above, following work-around can be used:

1. Disable the FSK detection of PCD3316, before and during the ringing signal detection.
2. Switch on the FSK detection only after a certain period, e.g. 100 ms after the ringing signal goes inactive.
3. When the first FSK data is detected, e.g '55H' (possible part of channel seizure), switch off the FSK detection and on again. This will force the FSK detector to resynchronize and detect the normal FSK data correctly. It may be necessary to repeat this sequence a number of times to ensure that the data detected really comes from the channel seizure. Thus, it is recommended to wait for a multiple number of bytes '55H' to be detected to validate a correct channel seizure.

12. Revision history

Rev	Date	CPCN	Description
01	990311	-	**This data sheet supersedes the version of 1998 May 14 (9397 750 03525):** • The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard • Section 1 "General description" on page 1: reference to application note AN98701 added • Section 7.6 "Level detect" on page 7: Added text regarding the frequency band for signal power measurement • Section 7.10 "3.58 MHz oscillator circuitry" on page 8: recommended resonator indication removed • Section 7.13 "Registers" on page 15: new register presentation in this section • Table 14 " Description of CIDMD1 bits" on page 17: Description of bit CIDMD1.6 and CIDMD1.5 adjusted • Application diagram Figure 16a on page 23: diodes removed • Added Section 11.1 "Application note on Customer Premises Equipment (CPE) testing" on page 23.

Contents

Enhanced Pager Decoder for APOC1/POCSAG

PCD5002A

CONTENTS

Enhanced Pager Decoder for APOC1/POCSAG

PCD5002A

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- EEPROM programming requires only 2.0 V supply
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range −25 to +70 °C
- *"CCIR radio paging Code No. 1"* (POCSAG) compatible
- Supports Advanced Pager Operator's Code Phase 1 (APOC1) for extended battery economy
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16 times oversampling) and bit clock recovery
- Advanced ACCESS® synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses Receiver Identity Codes (RICs), each with 4 functions/alert cadences
- Optional automatic call termination when bit error rate is high
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Continuous data decoding upon reception of user programmable sync word (optional)
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF oscillator for battery economy
- Dedicated pin for easy control of superheterodyne receiver
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming (data transfer at up to 100 kbits/s)
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real-time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Advanced display pagers (POCSAG and APOC1)
- Basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5002A is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC1 code. Continuous data decoding upon reception of a dedicated sync word is available for news pager applications.

Data rates supported are 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.0 V, allowing 'over-the-air' programming. I²C-bus compatible.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5002AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

5 LICENSE

Supply of this IC does neither convey nor express an implied license under any patent right to use this in any APOC application.

6 BLOCK DIAGRAM

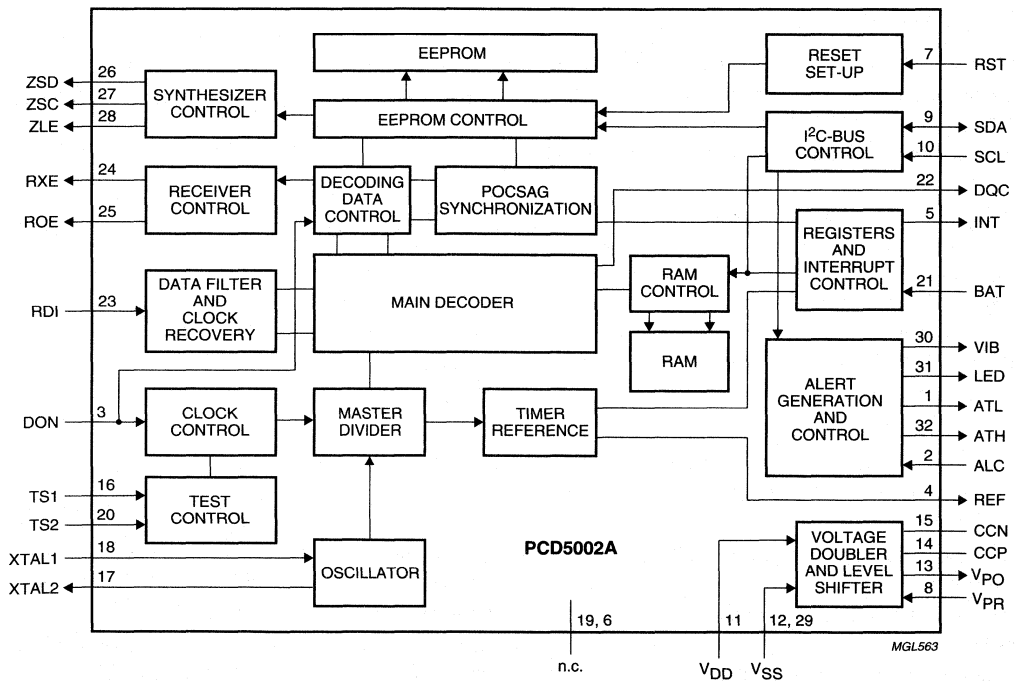


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real-time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)

SYMBOL	PIN	DESCRIPTION
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
DQC	22	demodulator quick charge output
RDI	23	received data input (POCSAG or APOC1)
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

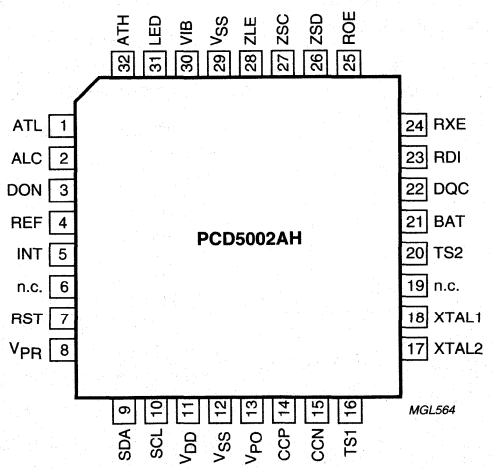


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Introduction

The PCD5002A is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5002A allows for flexible application in a wide variety of radio pager designs.

The PCD5002A is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

The PCD5002A also supports the new Advanced Pager Operator's Code Phase 1 (APOC1). This compatible extension to the POCSAG code improves battery economy by introducing 'cycles' and batch numbering. A cycle consists of 5 or 15 standard POCSAG batches. Each pager will be allocated a batch number in addition to its POCSAG address and it will only search for its address during this batch.

In addition to the standard POCSAG sync word (used also in APOC1) the PCD5002A is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG or APOC1 transmissions via the same radio channel. As an option reception of a UPSW may activate Continuous Data Decoding (CDD).

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5002A offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs) and UPSWs, which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5002A well suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5002A will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5002A can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5002A contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5002A.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5002A such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real-time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption. The APOC1 code uses an extended version of the ACCESS® synchronization algorithm.

Random (and optional) burst error correction techniques are applied to the received data to optimize the call success rate without increasing the falsing rate beyond specified POCSAG levels.

8.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 code-words of 32 bits each. The first code-word is a synchronization code-word with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 code-words each, containing message information. A code-word in a frame can either be an address, message or idle code-word.

Idle code-words also have a fixed pattern and are used to fill empty frames or to separate messages.

Address code-words are identified by an MSB at logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address code-word (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different call types ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished. The call type is determined by two function bits in the address code-word (bits 20 and 21), as shown in Table 1.

Alert-only calls consist only of a single address code-word. Numeric and alphanumeric calls have message code-words following the address. A message causes the frame structure to be temporarily suspended. Message code-words are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message code-words are identified by an MSB at logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each code-word is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32).

This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per code-word.

8.3 The APOC1 paging code

The APOC1 paging code is fully POCSAG compatible and involves the introduction of batch grouping and a Batch Zero Identifier (BZI). This reserved address code-word indicates the start of a 'cycle' of 5 or 15 batches long and is transmitted immediately after a sync word.

Cycle transmission must be coherent i.e. a transmission starting an integer number of cycle periods after the start of the previous one.

Broadcast message data may be included in a transmission. This information may occupy any number of message code-words and immediately follows the batch zero identifier of the first cycle after preamble.
The presence of data is indicated by the function bits in the batch zero identifier: 1,1 indicates 'no broadcast data'. Any other combination indicates a broadcast message.

The PCD5002A can be configured for POCSAG or APOC1 operation via SPF programming. The batch zero identifier is programmable and can be stored in any identifier location in EEPROM.

The POCSAG standard only allows combinations of data formats and function code bits as given in Table 1. However, other (non-standard) combinations will be decoded normally by the PCD5002A.

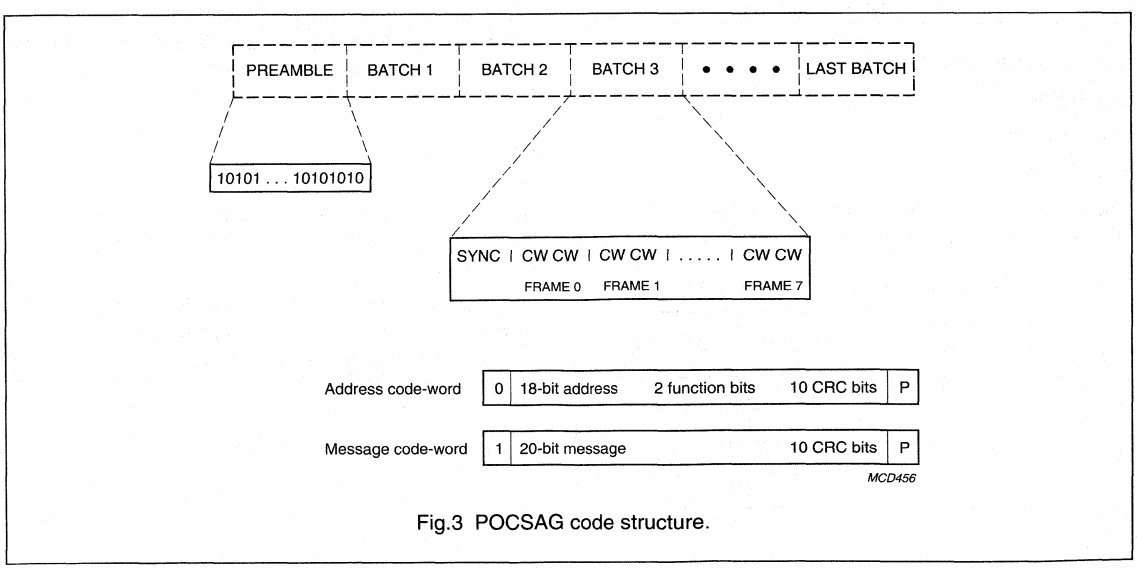


Fig.3 POCSAG code structure.

Table 1 POCSAG recommended call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only 1	–
1	0	alert only 2	–
1	1	alphanumeric	7-bits per ASCII character

8.4 Error correction

In the PCD5002A error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message code-words. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each code-word is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	CORRECTION
Preamble	4 random errors in 31 bits
Synchronization code-word	2 random errors in 32 bits
Address code-word	2 random errors; plus 4-bit burst errors (optional)
Message code-word	2 random errors; plus 4-bit burst errors (optional)

8.5 Operating states

The PCD5002A has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a direct control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

8.6 ON status

In the ON status the decoder pulses the receiver and oscillator enable outputs (RXE and ROE respectively) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call reception.

The data protocol can be POCSAG or APOC1. Continuous data decoding upon reception of a special sync word is also supported. The data protocol is selected by SPF programming.

Reception of a valid paging call is signalled to the microcontroller by an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

8.7 OFF status

In the OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. Using SPF programming the signal periodicity may be selected as;
32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

8.8 Reset

The decoder can be reset by applying a positive pulse on input pin RST. For successful reset at power-on, a HIGH level must be present on the RST pin while the device is powering-up.

This can be applied by the microcontroller, or via a suitable RC power-on reset circuit connected to the RST input. Reset circuit details and conditions during and after a reset are described in Chapter 9.

8.9 Bit rates

The PCD5002A can be configured for data rates of 512, 1200 or 2400 bits/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

8.10 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

8.11 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $\frac{1}{8}$ or $\frac{1}{32}$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

8.12 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address code-word is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next code-word must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{ROE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (using output ROE) before activating the rest of the receiver. This is possible using the UAA2082 receiver which has external biasing for the oscillator circuit.

8.13 POCSAG synchronization strategy

In the ON status the PCD5002A synchronizes to the POCSAG data stream by the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (RXE and ROE respectively) are switched accordingly, with the appropriate establishment times (t_{RXON} and t_{ROON} respectively).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to the ON status, the decoder is in **switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and the sync word. Failure to detect preamble or the sync word will cause the device to switch to the 'carrier off' mode.

When preamble is detected it will cause the device to switch to the **preamble receive** mode, in which a sync word is searched for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within a 1 batch duration the 'carrier off' mode is entered.

Upon detection of a sync word the **data receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message code-word reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch.

When a message extends beyond the end of a batch no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message code-word is found to be uncorrectable, the 'data fail' mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **data fail** mode message reception continues normally for 1 batch duration. When a sync word is detected at the expected position the decoder returns to the 'data receive' mode. If the sync word again fails to appear, then batch synchronization is deemed lost. Call reception is then terminated and the 'fade recovery' mode is entered.

The **fade recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ± 8 bits). This is performed for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble causes switching to the 'preamble receive' mode, while sync word detection causes switching to the 'data receive' mode. When neither is found within a period of 15 batches, the radio signal is considered lost and the 'carrier off' mode is entered.

The purpose of the **carrier off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 code-word in every 18 code-words looking for preamble or sync word.
By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble causes the device to switch to the 'preamble receive' mode, while sync word detection causes the device to switch to the 'data receive' mode.

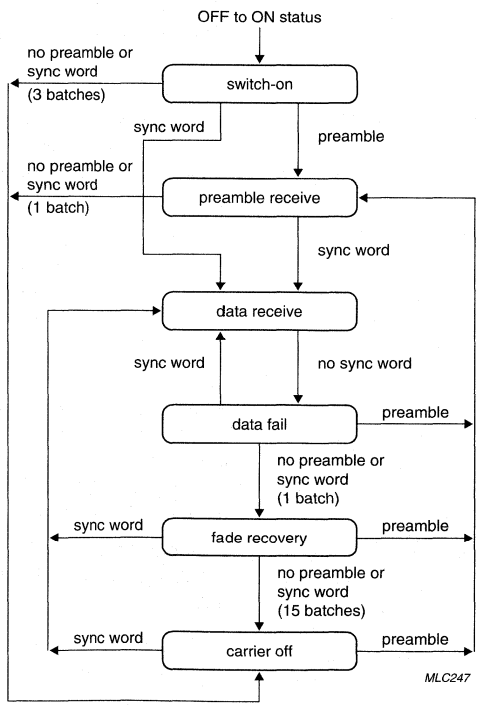


Fig.4 ACCESS® synchronization algorithm for POCSAG.

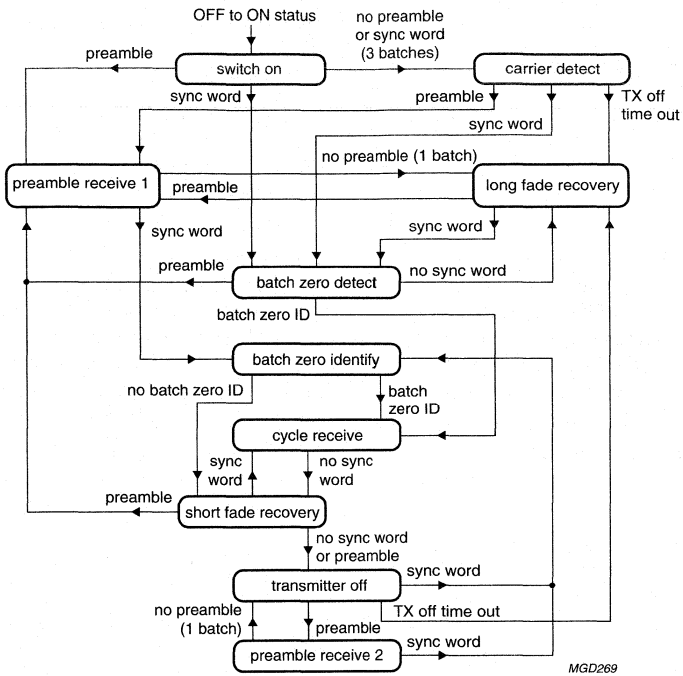


Fig.5 APOC1 synchronization algorithm.

8.14 APOC1 synchronization strategy

The synchronization strategy in APOC1 is an extended version of the ACCESS® scheme and is illustrated in Fig.5. The PCD5002A counts the number of batches in a transmission, starting from the first batch received after preamble. Counter overflow occurs due to the size of a cycle, as determined by SPF programming.

Initially, after switching to the ON status, the decoder will be in the **switch-on** mode. Here the receiver will be enabled for up to 3 batches, testing for preamble and sync word. Detection of preamble causes the device to switch to the 'preamble receive' mode, while any enabled sync word enters the 'batch zero detect' mode. Failure to detect either will cause the device to switch to the 'carrier detect' mode.

In the **preamble receive 1** mode the PCD5002A searches for a sync word, the receiver remaining enabled while preamble is detected. As soon as an enabled sync word is found the 'batch zero identify' mode is started.

If preamble is not found within one batch duration then the 'long fade recovery' mode is entered.

When in **batch zero detect** mode the PCD5002A switches on every batch to maintain synchronization and check for the batch zero identifier. Detection of the batch zero identifier activates the 'cycle receive' mode. When synchronization is lost the 'long fade recovery' mode is entered. 'preamble receive' mode is entered when preamble is detected.

In the **batch zero identify** mode the first code-word immediately after the sync word of the first batch is compared with the programmed batch zero identifier. Failure to detect the batch zero identifier will cause the device to enter the 'short fade recovery' mode.

When this comparison is successful the function bits determine whether any broadcast message will follow. Any function bit combination other than '1,1' will cause the PCD5002A to accept message code-words until terminated by a valid address code-word.

After reception of any broadcast message data the PCD5002A continues to operate in the 'cycle receive' mode.

In the **cycle receive** mode the PCD5002A enables call reception in only one programmed batch per cycle. Sync word detection takes place from 2 bits before to 2 bits after the expected sync word position of this batch. If the sync word is not detected then the position of the current sync word will be maintained and the 'short fade recovery' mode will be entered.

When a valid sync word is found user address code-word detection takes place, as in normal POCSAG code. Any following message code-words are received normally. If a message extends into a subsequent batch containing a batch zero identifier, then the batch zero identifier is detected normally and message reception will continue.

Data reception is suspended after the programmed batch until the same batch position in the next cycle. The exception being when a received call continues into the next batch.

In the **short fade recovery** mode the programmed data receive batch will continue to be checked for user address code-words. In addition the first code-word after the programmed batch is checked for sync word or preamble.

When a valid sync word is detected the 'cycle receive' mode is re-entered, while detection of preamble causes the device to switch to the 'preamble receive' mode. When neither is found then the 'transmitter off' mode is entered.

In the **transmitter off** mode a time-out is set to a pre-programmed duration. This time-out corresponds to the maximum time between subsequent transmissions (preamble to preamble).

The PCD5002A then checks the first batch of every cycle for sync word or preamble. The programmed data receive batch is ignored (unless it is batch 0).

Table 4 Synchronization window tolerance as a function of bit rate

TIME FROM LOSS OF SIGNAL	TOLERANCE		
	512 (bits/s)	1200 (bits/s)	2400 (bits/s)
≤30 s	4 bits	4 bits	4 bits
≤60 s	4 bits	4 bits	8 bits
≤120 s	4 bits	8 bits	16 bits
≤240 s	8 bits	16 bits	32 bits

Synchronization checking is performed over a window ranging from 'n' bits before to 'n' bits after the expected sync word position. The window tolerance 'n' depends on the time since the 'transmitter off' mode was entered and on the selected bit rate (see Table 4).

When a sync word is detected in this widened synchronization window the PCD5002A enters the 'batch zero identify' mode. Time-out expiry before a sync word has been detected causes the device to switch to the 'long fade recovery' mode.

Detection of preamble in the 'transmitter off' mode initiates the **preamble receive 2** mode. Operation in this mode is identical to 'preamble receive mode'. Failure to detect preamble for one batch period will cause the device to switch back to the 'transmitter off' mode. This prevents inadvertent loss of cycle synchronization due to spurious signals resembling preamble.

The **carrier detect** mode is identical to the 'carrier off' mode in standard POCSAG operation. Upon first entry the transmitter off time-out is started. The receiver is enabled to receive one code-word in every 18 code-words to check for sync word and preamble. This check is performed on the last available 32 bits for every received bit.

The 'preamble receive' mode is entered if preamble is detected. If a valid sync word is found the 'batch zero detect' mode is entered. If neither has been detected and the time-out expires, then the 'long fade recovery' mode is entered.

The **long fade recovery** mode is intended to quickly regain synchronization in fading conditions (not caused by the transmitter switching off between transmissions) or when having been out of range, while maintaining acceptable battery economy.

Initially, the receiver is switched off until one cycle duration after the last enabling in the 'transmitter off' mode. The receiver is then enabled for a 2 code-word period in which each contiguous group of 32 bits is tested for **any decodable** POCSAG code-word (including sync word) and preamble. Single-bit error correction is applied.

If a code-word is detected, the receiver enable period is extended by another code-word duration and the above test is repeated. This process continues while valid code-words are received.

Detection of preamble will cause the device to switch to the 'preamble receive' mode, while sync word detection will cause the device to switch to the 'batch zero detect' mode. When neither is detected during the 2 code-word window or any following 32-bit group, the receiver will be disabled.

If valid code-words are detected but no sync word or preamble is detected over a period of 18 code-words, the receiver is also disabled.

Data sampling, as previously described, is repeated one cycle duration after the moment the receiver was last activated.

8.15 Call termination

Call reception is terminated:

- Upon reception of any address code-word (including idle code-word but excluding the batch zero identifier in APOC1 operation) requiring no more than single bit error correction
- Upon reception of a correctable address code-word (error type other than '111'; see Table 11) that matches an enabled RIC
- When a forced call termination command is received from an external controller.
- In 'data fail' mode, when a sync word is not detected at the expected batch position.

The last method permits an external controller to stop call reception, depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter the 'data fail' mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

In the event of the terminating code-word matching an enabled RIC, a concatenated call will be started with the call header replacing the terminator of the previous call.

Following call termination, transfer of the data received since the previous sync word period is initiated by an interrupt to the external controller.

8.16 Enhanced call termination

The PCD5002A provides an enhanced mode of call termination which is enabled by setting SPF byte 3, bit D7. When enabled, the following call termination conditions applies, in addition to those listed in Section 8.15.

- Reception of two consecutive code-words (excluding sync word), each of which are either uncorrectable or an address code-word with more than one bit in error.

8.17 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per code-word. Each stored call consists of a call header, followed by message data blocks and a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 5, 7 and 9.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address code-word.

A **Message Data** block contains the data bits from a message code-word plus the type of error correction performed. No deformatting is performed on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data has a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in 'data fail' mode) and the type of error correction performed on the terminating code-word.

Table 5 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 6 Call header bit identification

BITS (MSB TO LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any code-word of a previous call received in the same batch was uncorrectable.

Table 7 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 8 Message data bit identification

BITS (MSB TO LSB)	IDENTIFICATION
M2 to M21	message code-word data bits
E3 to E1	detected error type; see Table 11
M1	message code-word flag

Table 9 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 10 Call terminator bit identification

BITS (MSB TO LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
E3 to E1	detected error type; see Table 11; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data code-word in the terminating batch was uncorrectable, while in 'data receive' mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in 'data fail' mode.

Table 11 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors; correct code-word	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	–
1	0	1	4-bit burst error and parity error	3 (e.g. 1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable code-word	3 or more

Note

1. POCSAG code allows a maximum of three bit errors to be detected per code-word.

8.18 Error type indication

Table 11 shows how the different types of detected errors are encoded in the call data output format.

8.19 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next code-word.

When the PCD5002A is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Call termination can occur on reception of an address code-word (or even a message code-word if in Enhanced Call Termination Mode) or when a sync word is not detected while in the 'Data Fail' mode ('Short Fade Recovery' in APOC1).

8.20 Continuous data decoding

Apart from transmissions in the POCSAG or APOC1 format, the PCD5002A is also capable of decoding continuous transmissions with the same code-word structure. Any User-Programmable Sync Word (UPSW) may be designated to enable continuous data decoding.

When a Continuous Data Decoding (CDD) sync word is detected at any sync word position, the receiver remains enabled from then on. Status bits D1 and D0 show the CDD mode to be active.

All code-words are decoded and their data fields are stored in SRAM. The usual error information is appended. No distinction is made between address and message code-words: code-word bit 0 is treated as a data bit and is stored in bit M1 of the 3-byte output format.

Code-words received at the expected sync word positions (POCSAG batch size) are matched against standard POCSAG sync word, all enabled UPSWs and preamble.

Data output to an external controller is initiated by an interrupt at the next sync word position, after reception of 16 code-words.

The call header preceding the data has a different structure from normal POCSAG or APOC1 data. The data header format is shown in Table 12.

Continuous data decoding continues until one of the following conditions occur:

- The decoder is switched to the OFF state
- A Forced Call Termination (FCT) command is received via the I^2C-bus
- Preamble is detected at the sync word position
- Standard POCSAG sync word or an enabled non-CDD sync word is detected.

Only a forced call termination command will be indicated in the SRAM data by a call terminator. In the other events continuous data decoding will stop without notification.

Upon forced termination the 'fade recovery' mode is entered. Detection of preamble causes the device to switch to the 'preamble receive' mode. Detection of a standard sync word or any enabled non-continuous UPSW will cause the device to switch to the 'data receive' mode.

Continuous data decoding will continue in the next batch if any enabled CDD sync word is detected or no enabled sync word is detected. It should be noted that the enhanced call termination is ignored in CCD mode.

8.21 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 14).

Table 12 Continuous data header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	X	X	X	C3	C2	C1	0
2	0	C3	C2	C1	C3	C2	C1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 13 Data header bit identification

BITS (MSB TO LSB)	IDENTIFICATION
C3 to C1	identifier number of continuous data decoding sync word
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type (see Table 11); E3 = 0 in a concatenated call header

Table 14 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 25).

8.22 Demodulator quick charge

Two modes of operation are available that determine the period when the DQC output is set

The operating mode is selected by EEPROM programming of SPF byte 03, bit D5:

- **Mode 0 (D5 = 0)**: DQC is active HIGH during the receiver establishment time (t_{RXE}) in all ACCESS and APOC1 modes except data receive and data fail (cycle receive and short fade recovery in APOC1). During switch-on, DQC is active for 1 code-word duration.
- **Mode 1 (D5 = 1)**: DQC is active during sync word detection in all ACCESS and APOC1 modes. During switch-on and preamble receive modes, DQC is active continuously.

The timing of DQC is as follows (see Fig.6):

- **Mode 0**: Set along with RXE output (time t_{RXE} before the first code-word is expected); cleared during the second bit of the code-word following t_{RXE}
- **Mode 1**: Set during the second bit of the sync word; cleared after the last bit of the sync word.

Note: During switch-on, t_{RXE} is not used: RXE and DQC are switched on immediately.

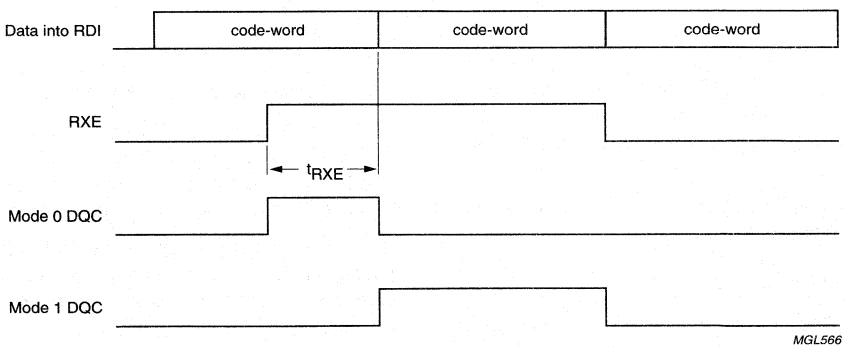


Fig.6 DQC Timing.

8.23 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be exited by means of a reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

8.24 Battery condition input

A logic signal from an external sense circuit, signalling battery condition, can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

8.25 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 1, bit D6), data is transferred to the synthesizer each time the PCD5002A is switched from the OFF to the ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 28).

Data bits on ZSD change on the falling edges of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is illustrated in Fig.7.

The data output timing is synchronous, but has a pause in the bitstream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 15. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is illustrated in Fig.14.

Table 15 Synthesizer programming pause

BIT RATE (bits/s)	t_p (CLOCKS)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

8.26 Serial microcontroller interface

The PCD5002A has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5002A is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a START condition (S: SCL = 1, SDA = ↓) and terminated by a STOP condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the STOP condition can be replaced with a new START condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit A (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is illustrated in Fig.6. Formats for master/slave communication are illustrated in Fig.9.

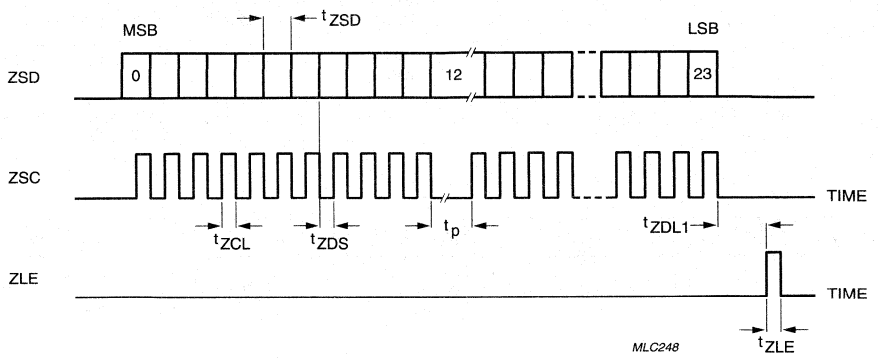


Fig.7 Synthesizer interface timing.

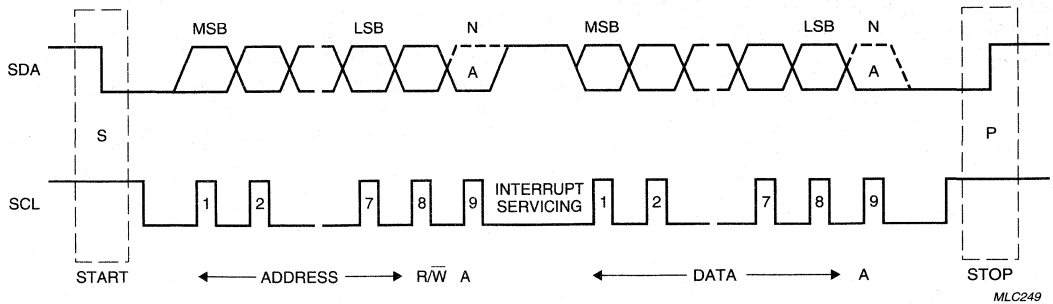
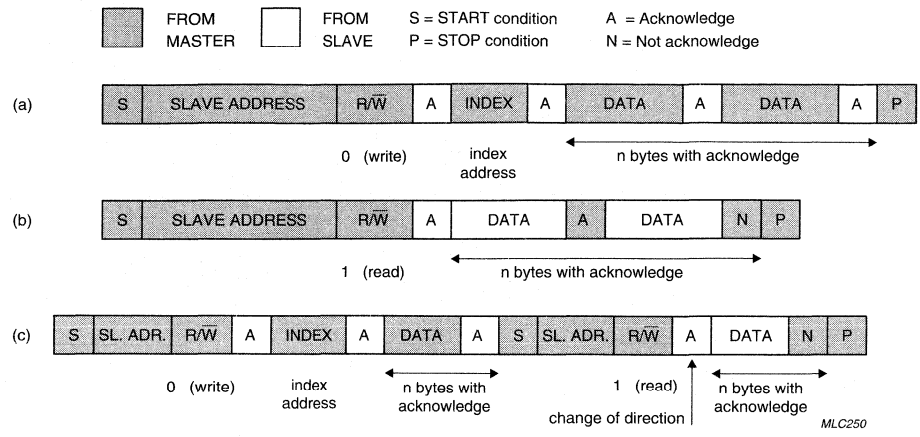


Fig.8 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.9 Message types.

8.27 Decoder I²C-bus access

All internal access to the PCD5002A takes place via the I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 16 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and is organized as a matrix. The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus write message to the PCD5002A must start with its slave address, followed by the index address of the memory element to be accessed. An I²C-bus read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.9.

As a slave the PCD5002A cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 16 Index register

ADDRESS[1]	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real-time clock: seconds	R/$\overline{W}$
02H	real-time clock: $^1/_{100}$ second	R/$\overline{W}$
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/$\overline{W}$
08H	RAM read address pointer	R/$\overline{W}$
09H	RAM data output	R
0AH	EEPROM data input/output	R/$\overline{W}$
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

8.28 External interrupt

The PCD5002A can signal events to an external controller via an interrupt signal at output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event is possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position, if data fail mode (short fade recovery mode in APOC1) is not active.

The interrupt output INT is reset after completion of a status read operation.

8.29 Interrupt masking

In the PCD5002A certain interrupts can be suppressed by masking via the control register. The following interrupts can be masked:

- **Out-of-Range (status bit D5)**: change of state interrupt, masked by setting control register bit D5
- **BAT/RXE monitoring (status bit D6)**: change of state interrupt (source selected by control register bit D2), masked by setting control register bit D6
- **Periodic Timer (status bit D7)**: timer overflow interrupt, masked by setting control register bit D7.

Although no interrupts are generated by these conditions when masked via the control register, the corresponding status bits are updated normally and available via the status register. At reset the control register is cleared, causing all interrupts to be enabled.

8.30 Status/control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 17 and 18 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 17).

Table 17 Status register (00H; read)

BIT(1)	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received (POCSAG or APOC1)
	1 0	continuous decoding data available
	1 1	batch zero data available (APOC1)
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different; data to be read
	1 0	RAM read/write pointers equal; no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 18 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1 and ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5	1	out-of-range interrupt masked
D6	1	BAT/RXE monitor interrupt masked
D7	1	Periodic Timer interrupt masked

8.31 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. An immediate interrupt is then generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

8.32 Out-of-range indication

The out-of-range condition occurs when entering the 'fade recovery' or 'carrier off' mode in POCSAG, or 'transmitter off' or 'carrier detect' mode in APOC1. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE ↓ 0). Every change of state in bit D5 generates an interrupt.

8.33 Real-time clock

The PCD5002A provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period, it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is illustrated in Fig.16.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real-time clock counter runs continuously irrespective of the operating condition of the PCD5002A. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read from or written to via the I²C-bus. The bit allocation of both registers is shown in Tables 19 and 20.

Table 19 Real-time clock; seconds register (01H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written; undetermined when read
D7	X	not used: ignored when written; undetermined when read

Table 20 Real-time clock; $1/100$ second register (02H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	0.01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written; undetermined when read

8.34 Periodic interrupt

A periodic interrupt can be realised with the periodic interrupt counter. This 8-bit counter is incremented every $1/100$ s and produces an interrupt when it reaches the value stored in the periodic interrupt modulus register. The counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the modulus register. Writing a zero will stop interrupt generation immediately and will halt the periodic interrupt counter after 2.55 s.

The modulus register is write-only, the counter register is read only. Both registers have the same index address (05H).

8.35 Received call delay

Call reception (detection of an enabled RIC) causes both the periodic interrupt modulus and the counter register to be reset.

Since the periodic interrupt counter runs for another 2.55 s after a reset, the received call delay (in $^1/_{100}$ s units) can be determined by reading the counter register.

Table 21 Alert set-up register (04H; write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7 and D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00; see Fig.10 (a)
	0 1	POCSAG alert pattern FC = 01; see Fig.10 (b)
	1 0	POCSAG alert pattern FC = 10; see Fig.10 (c)
	1 1	POCSAG alert pattern FC = 11; see Fig.10 (d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address code-word, which designate the POCSAG call type as shown in Table 1.

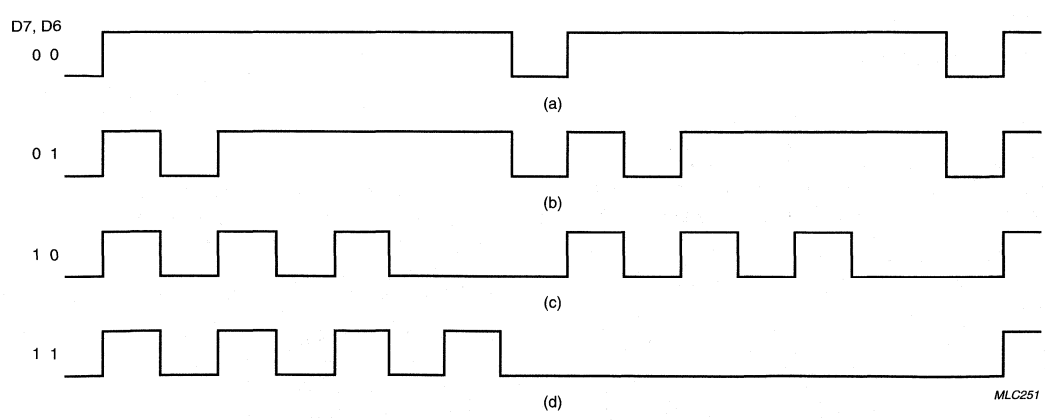


Fig.10 POCSAG alert patterns.

8.36 Alert generation

The PCD5002A is capable of controlling 3 different alert transducers, acoustic beeper (high and low level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open-drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 21.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

8.37 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is initiated an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation within 62.5 ms.

8.38 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 in the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 s (ATL), followed by 12 s at HIGH level (ATL + ATH). When D1 is set, the full 16 s are at HIGH level. An interrupt is generated after the full alert time has elapsed (indicated by bit D4 in the status register).

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advisable to reset the last bit of the previous pattern to prevent unwanted audible level changes.

8.39 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported, LOW level (25 Hz square wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

8.40 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

8.41 Warbled alert

When enabled, by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

8.42 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

8.43 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from its last position. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated in synchronism with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

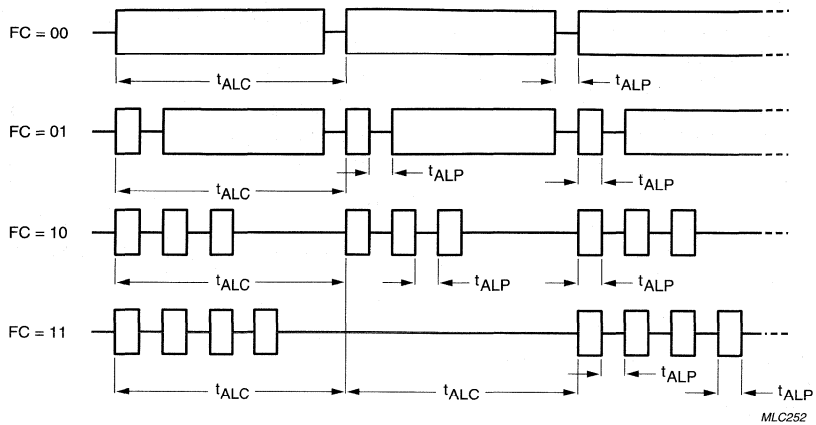


Fig.11 POCSAG alert timing.

8.44 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

8.45 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address code-word (see Table 1). The timing of these alert patterns is shown in Fig.11. After completion of the full 16 s alert period an interrupt is generated by status bit D4.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will be automatically generated at outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address code-word.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

8.46 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per code-word) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0); data is available for reading, if data fail mode (short fade recovery mode in APOC1) is not active
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the code-word following the 'RAM full' interrupt.

8.47 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, because the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH. Bit D7 (MSB) is not used and its value is undefined when read. When a call data byte is written to location 5FH, the write address pointer wraps around to 00H. This does not necessarily imply a RAM full condition.

8.48 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

The RAM read address pointer can be accessed for reading and writing.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written to and undefined when read from.

8.49 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer and can only be read. Each read operation causes an increment of the RAM read address pointer.

8.50 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous. Figure 12 shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes are available for general purpose storage.

8.51 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read from or written to via the EEPROM data I/O register.

The EEPROM address pointer contains two counters for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

8.52 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written to or read from via the EEPROM data I/O register. Each access automatically increments the EEPROM address pointer.

8.53 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advisable to switch to the OFF state before accessing the EEPROM.

The EEPROM cannot be written to unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum programming supply voltage ($V_{DD(prog)}$) is required (2.0 V typ.). The programming supply current ($I_{DD(prog)}$) required during writing is approximately 500 μA.

8.54 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single byte or block reads are permitted.

8.55 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of 7.5 ms (max.) is required to complete the internal programming operation. During this time the external microcontroller may generate an I²C-bus STOP condition. If another I²C-bus transfer is initiated the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in, the control register must be reset.

8.56 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

8.57 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus STOP condition. The EEPROM programming enable bit (D1) in the control register must then be reset.

Any bytes received from the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

8.58 Unused EEPROM locations

A total of 20 EEPROM bytes are available for general purpose storage (see Table 22).

Table 22 Unused EEPROM addresses

ROW	HEX
0	04 and 05[1]
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

8.59 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 23 to 27. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

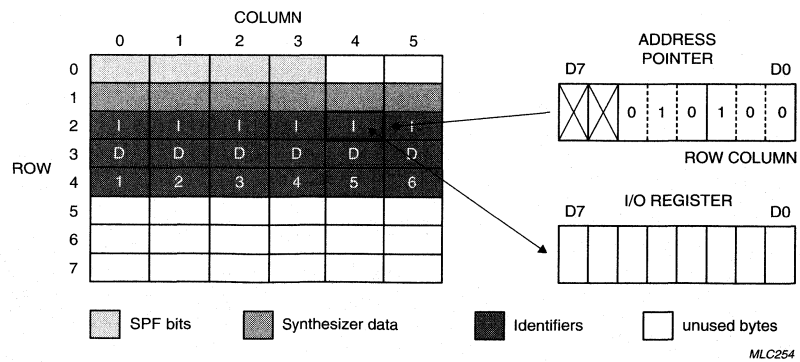


Fig.12 EEPROM organization and access.

Table 23 Special programmed functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	POCSAG decoding enabled
	1	APOC1 decoding enabled
D1	0	cycle length: 5 batches
	1	cycle length: 15 batches
D5 to D2 (MSB D5)	0 to 4	batch number (D1 = 0; MSB is ignored)
	0 to 14	batch number (D1 = 1)
D6	1	continuous data decoding enabled
D7	1	received data inversion enabled

Table 24 Special programmed functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms receiver establishment time (nominal); note 1
	1 0	15 ms receiver establishment time (nominal); note 1
	1 1	30 ms receiver establishment time (nominal); note 1
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms oscillator establishment time (nominal); note 1
	1 0	40 ms oscillator establishment time (nominal); note 1
	1 1	50 ms oscillator establishment time (nominal); note 1
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 25 shows the values for the various bit rates.

Table 25 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 (bits/s)	1024 (bits/s)	1200 (bits/s)	2400 (bits/s)
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5 ms (6 bits)	5 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10 ms (12 bits)	10 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20 ms (24 bits)	20 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40 ms (48 bits)	40 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 26 Special programmed functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real-time clock reference
	0 1	50 Hz square wave
	1 0	2 Hz
	1 1	$1/60$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	0 0	30 s (+0.5 s max.) transmitter off time-out
	0 1	60 s (+ 1 s max.) transmitter off time-out
	1 0	120 s (+ 2 s max.) transmitter off time-out
	1 1	240 s (+ 4 s max.) transmitter off time-out

Table 27 Special programmed functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz acoustic alerter frequency
	1 0	4096 Hz acoustic alerter frequency
	1 1	3200 Hz acoustic alerter frequency
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	0	DQC mode 0
	1	DQC mode 1
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	0	standard call termination
	1	enhanced call termination

8.60 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting with address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 28 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

8.61 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5002A can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW)
- Batch zero identifiers
- Continuous Data Decoding (CDD) sync words.

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Each identifier can be individually enabled. The standard POCSAG sync word is always enabled and has identifier number 7.

The identifier type is determined by bits D2 and D0 of identifier byte 3, as shown in Table 31.

Identifiers 1 and 2 always represent RICs or batch zero identifiers. The last 4 identifiers (numbers 3 to 6) can represent any identifier type.

A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

A batch zero identifier marks the start of a new cycle in the APOC1 protocol. It is only recognized when APOC1 decoding has been enabled (SPF byte 00, bit D0).

Reception of a CDD sync word initiates continuous data decoding. CDD sync words are only recognized when continuous data decoding has been enabled (SPF byte 00, bit 6).

Table 29 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 30.

Table 29 Identifier storage allocation (EEPROM address 10H to 25H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 30 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG code-word (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	batch zero ID/continuous decoding (1 = enabled)

Notes

1. The bit numbering corresponds with the numbering in a POCSAG code-word; bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0. Bits 2 to 19 contain the identifier bit pattern, they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Table 31 Identifier types

BYTE 3; BIT D2	BYTE 3; BIT D0	DESCRIPTION
0	0	user programmable sync word
0	1	continuous data decoding sync word
1	0	normal user address (RIC)
1	1	batch zero identifier

8.62 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller at output V_{PO}. An external ceramic capacitor of 100 nF (typ.) is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

8.63 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5002A.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. If required this could be the on-chip voltage doubler output V_{PO}. When the microcontroller has a separate (regulated) supply it should be connected to V_{PR}.

The level-shifted interface lines are RST, DON, ALC, REF and INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by the standard external pull-up resistors.

8.64 Signal test mode

A special 'signal test' mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5002A.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The 'signal test' mode is activated/deactivated by SPF programming.

9 OPERATING INSTRUCTIONS

9.1 Reset conditions

When the PCD5002A is reset by applying a HIGH level to input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- All interrupts enabled
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high-impedance
- SDA and SCL inputs high-impedance
- Voltage converter disabled.

The programmed functions are activated within t_{RSU} after release of the reset condition (RST LOW). The settings affecting the external operation of the PCD5002A are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

9.2 Power-on reset circuit

During power-up of the PCD5002A a HIGH level of minimum duration t_{RST} = 50 µs must be applied to pin RST. This is to prevent EEPROM corruption which might otherwise occur because of the undefined contents of the control register.

The reset signal can be applied by the external microcontroller or by an RC power-on reset circuit on pin RST (C to V_{PR}, R to V_{SS}). Such an RC-circuit should have a time constant of at least $3t_{RST}$ = 150 µs.

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply) which could be used together with a suitable external capacitor connected to V_{PR} to create a power-on reset signal. However, since this pull-down resistor varies considerably with processing and supply voltage, the resulting time constant is inaccurate.

A more accurate reset duration can be realised with an additional external resistor connected to V_{SS}.

Recommended minimum values in this case are C = 2.2 nF and R = 100 kΩ (see Fig.17).

9.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 s (typ. 800 ms). It is advisable to apply a reset condition, at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 µs.

During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor connected between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

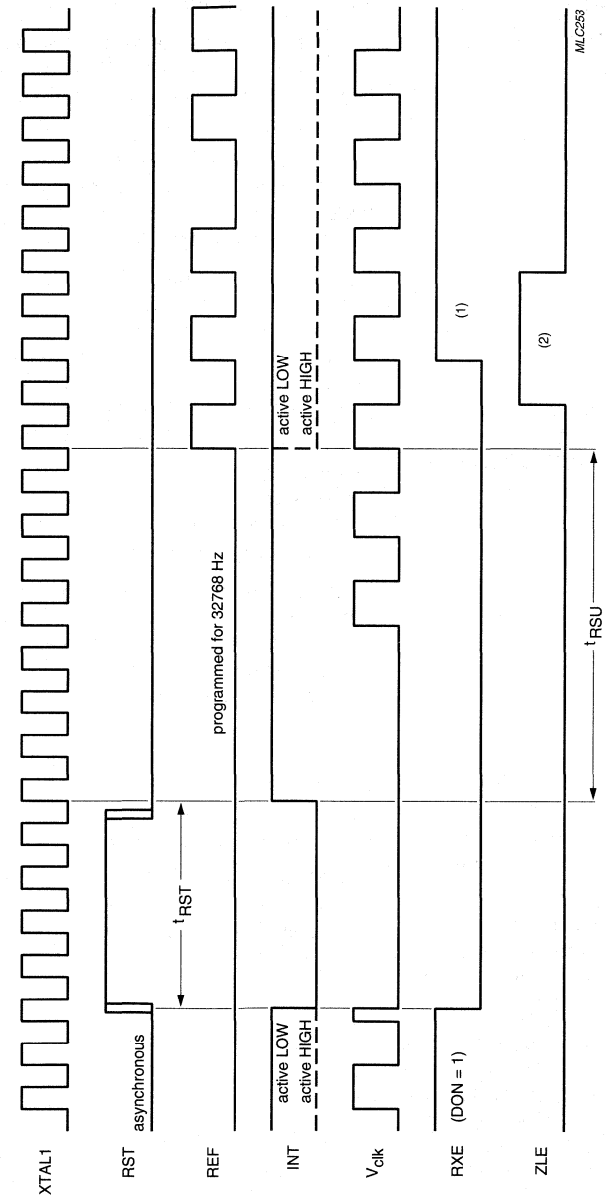
Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is illustrated in Fig.13. The start-up timing including synthesizer programming is illustrated in Fig.14.

9.4 Initial programming

A newly-delivered PCD5002A has EEPROM contents which are undefined. The EEPROM should therefore be programmed, followed by a reset to activate the SPF settings, before any attempt is made to use the device.



(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.13 Reset timing.

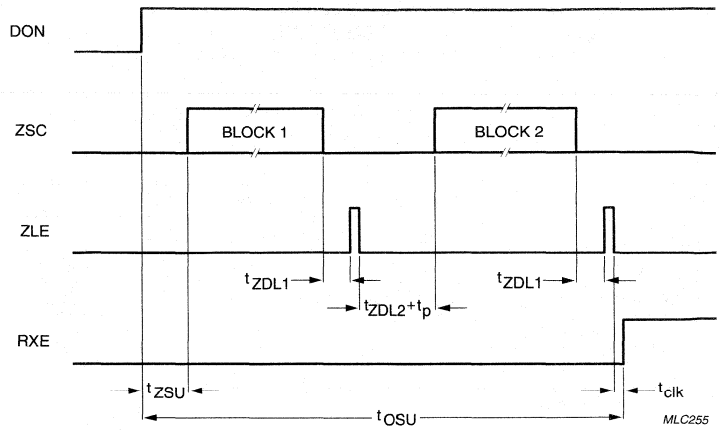


Fig.14 Start-up timing including synthesizer programming.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	input voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		−	250	mW
P_{out}	power dissipation per output		−	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

11 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	voltage converter disabled	1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
$V_{DD(prog)}$	programming supply voltage	voltage converter disabled	2.0	–	6.0	V
		voltage converter enabled	2.0	–	3.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
$I_{DD(prog)}$	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW-level input voltage pins					
	RDI and BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC and RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA and SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage pins					
	RDI and BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC and RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA and SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW-level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH-level input current pins	T_{amb} = 25 °C				
	TS1 and TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI and BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI and BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC and RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW-level output current pins	T_{amb} = 25 °C				
	VIB and LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT and REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC and ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE and DQC	V_{OL} = 0.3 V	80	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH-level output current pins	T_{amb} = 25 °C				
	VIB, LED and DQC	V_{OH} = 0.7 V	−0.6	–	−2.4	mA
	ATH	V_{OH} = 0.7 V	−3.0	–	−11.0	mA
	INT and REF	V_{OH} = 2.4 V	−80	–	–	µA
	ZSD, ZSC and ZLE	V_{OH} = 2.4 V	−60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	−0.5	µA
	ROE and RXE	V_{OH} = 2.4 V	−600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: $f_{ref} = 1/60$ Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 24).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter 10).
3. When ATL (open-drain output) is not activated it is high impedance.

12 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; $V_{PR} = V_{PO}$; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7 V; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2 V; I_{PO} = −250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2 V; V_{PO} = 2.7 V	−400	−650	–	µA
		V_{DD} = 3 V; V_{PO} = 4.5 V	−650	−900	–	µA

13 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent. Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF. Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging) for POCSAG, $\pm 55 \times 10^{-6}$ for APOC1 ('transmitter off' mode).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	UNIT
C_{XO}	output capacitance XTAL2		–	10	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	µS

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits				
		D1 and D0 = 0 0	–	2048	–	Hz
		D1 and D0 = 0 1	–	2731	–	Hz
		D1 and D0 = 1 0	–	3200	–	Hz
		D1 and D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH and LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low-level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high-level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low-level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high-level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real-time clock reference						
f_{ref}	real-time clock reference frequency	SPF byte 02H; bits				
		D3 and D2 = 0 0; note 1	–	32768	–	Hz
		D3 and D2 = 0 1; note 2	–	50	–	Hz
		D3 and D2 = 1 0	–	2	–	Hz
		D3 and D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real-time clock reference pulse duration	all reference frequencies except 50 Hz (square wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE and ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits				
		D1 and D0 = 0 0	–	5	–	ms
		D1 and D0 = 0 1	–	10	–	ms
		D1 and D0 = 1 0	–	15	–	ms
		D1 and D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits				
		D3 and D2 = 0 0	–	20	–	ms
		D3 and D2 = 0 1	–	30	–	ms
		D3 and D2 = 1 0	–	40	–	ms
		D3 and D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{LOW}	SCL clock low period		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH period		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		500	–	–	ns
t_r	SDA and SCL rise time		–	–	1000	ns
t_f	SDA and SCL fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time	see Fig.15	–	–	100	µs
t_{DI1}	data input logic 1 duration	see Fig.15	t_{BIT}	–	∞	
t_{DI0}	data input logic 0 duration	see Fig.15	t_{BIT}	–	∞	
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 0; D4 = 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	code-word duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	code-word duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	code-word duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
APOC1 batch timing						
t_{SB}	cycle duration	SPF byte 00H; bit D2 = 0 (5 batches)	–	2720	–	bits
		SPF byte 00H; bit D2 = 0 (15 batches)	–	8160	–	bits
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 3	1	–	2	bits
f_{ZSC}	output clock frequency	note 4	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 4	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal; 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.16.
2. 50 Hz reference signal: square wave.
3. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
4. Nominal values; pause in 12th data bit (see Table 11).

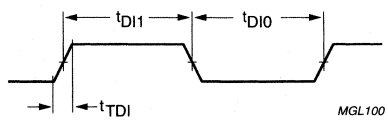


Fig.15 Data input timing.

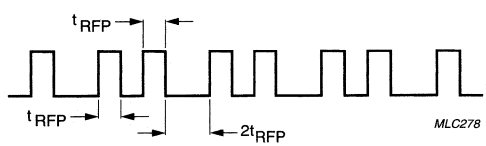


Fig.16 Timing of the 32 768 Hz reference signal.

15 APPLICATION INFORMATION

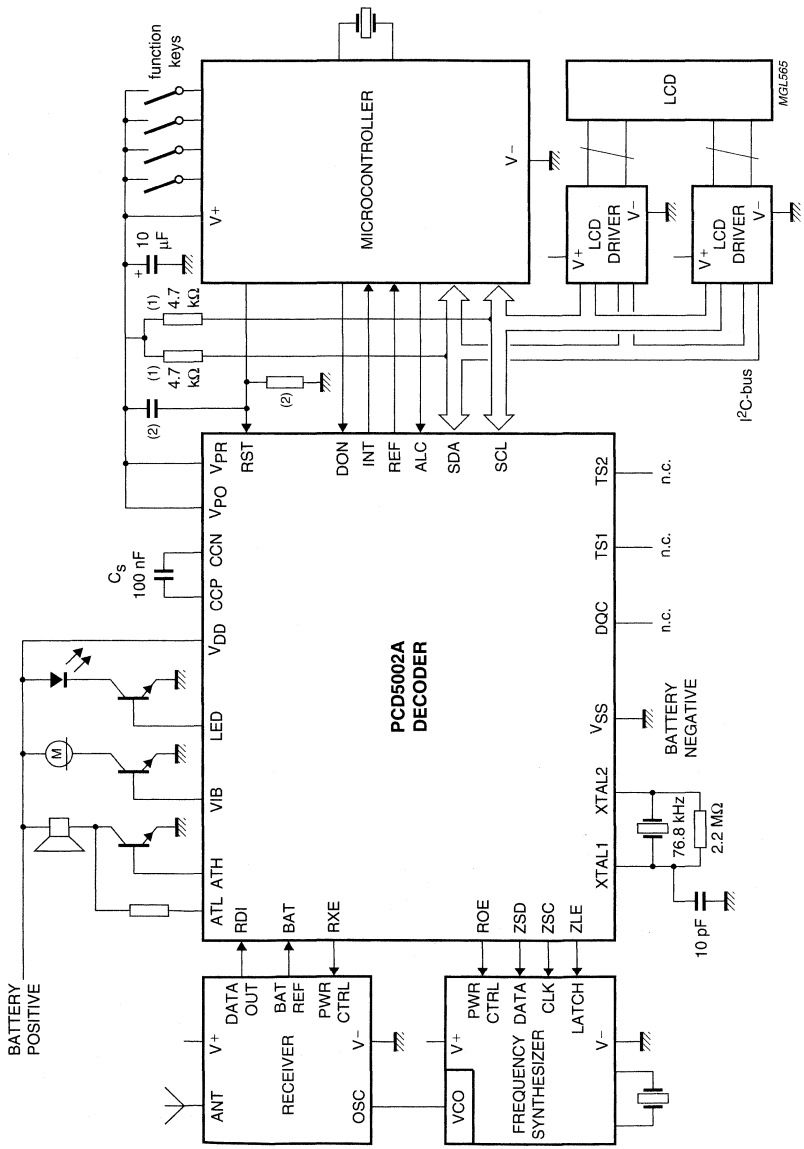


Fig.17 Typical application example (display pager).

(1) Value depends on number of devices attached.
(2) Values should be chosen to give a time constant of at least 150 µs. C = 2.2 nF and R = 100 kΩ are recommended.

CONTENTS

Enhanced Pager Decoder for POCSAG PCD5003A

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- EEPROM programming requires only 2.0 V supply
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range: −25 to +70 °C
- *"CCIR Radio paging Code No. 1"* (POCSAG) compatible
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS® synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses Receiver Identity Codes (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Optional automatic call termination when bit error rate is high
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF-oscillator for battery economy
- Dedicated pin for easy control of superheterodyne receiver
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming (data transfer at up to 400 kbits/s)
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real-time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Display pagers, basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5003A is a very low power POCSAG decoder and pager controller. It supports data rates of 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.0 V, allowing 'over-the-air' programming. The PCD5003A is fast I²C-bus compatible (maximum 400 kbits/s).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5003AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

5 BLOCK DIAGRAM

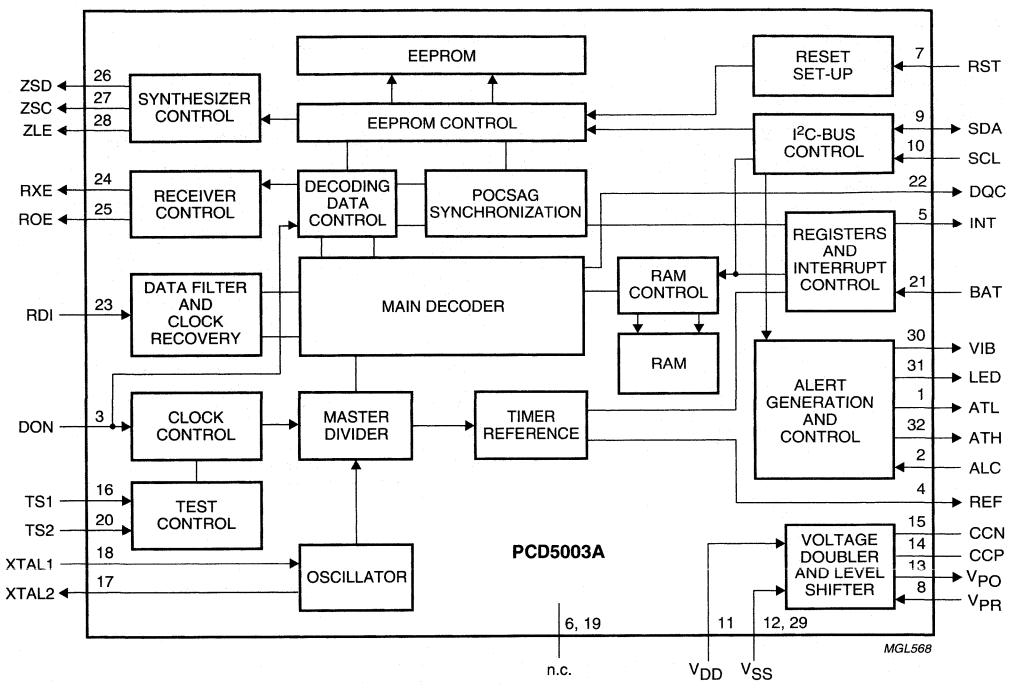


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW-level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real-time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)

SYMBOL	PIN	DESCRIPTION
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
DQC	22	demodulator quick charge output
RDI	23	received POCSAG data input
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH-level output

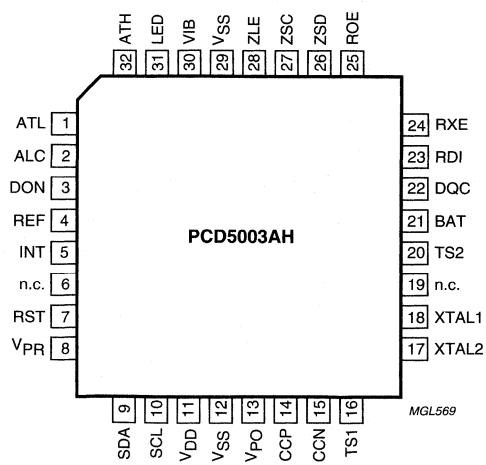


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Introduction

The PCD5003A is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5003A allows for flexible application in a wide variety of radio pager designs.

The PCD5003A is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG sync word the PCD5003A is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5003A offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5003A well suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003A will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5003A can also produce a HIGH-level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5003A contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003A.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5003A such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real-time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) burst error correction techniques are applied to the received data to optimize on call success rate without increasing falsing rate beyond specified POCSAG levels.

7.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 code-words of 32 bits each. The first code-word is a synchronization code-word with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 code-words each, containing message information. A code-word in a frame can either be an address, message or idle code-word.

Idle code-words also have a fixed pattern and are used to fill empty frames or to separate messages.

Address code-words are identified by an MSB of logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address code-word (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different **call types** ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished on each user address. The call type is determined by two function bits in the address code-word (bits 20 and 21), as shown in Table 1.

Alert-only calls only consist of a single address code-word. Numeric and alphanumeric calls have message code-words following the address. A message causes the frame structure to be temporarily suspended. Message code-words are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message code-words are identified by an MSB of logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21). The data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each code-word is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of maximum 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per code-word.

The POCSAG standard recommends the use of combinations of data formats and function bits, as given in Table 1. Other (non-standard) combinations will be received normally by the PCD5003A. Message data is not deformatted.

In the PCD5003A error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message code-words. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each code-word is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

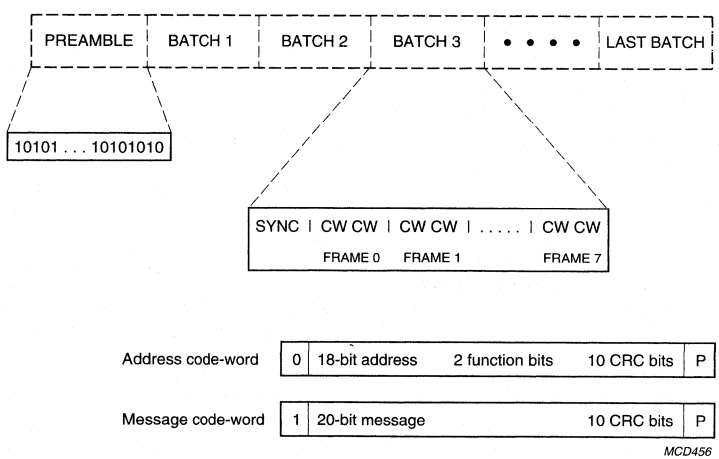


Fig.3 POCSAG code structure.

Table 1 POCSAG recommended call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only 1	–
1	0	alert only 2	–
1	1	alphanumeric	7-bits per ASCII character

7.3 Error correction

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization code-word	2 random errors in 32 bits
Address code-word	2 random errors; plus 4-bit burst errors (optional)
Message code-word	2 random errors; plus 4-bit burst errors (optional)

7.4 Operating states

The PCD5003A has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

7.5 ON status

In ON status the decoder pulses the receiver and oscillator enable outputs (respectively RXE and ROE) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call receipt. Reception of a valid paging call is signalled to the microcontroller by means of an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

7.6 OFF status

In OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. By SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $^1/_{60}$ Hz.

7.7 Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can be connected to this input as well. Conditions during and after a reset are described in Chapter "Operating instructions".

For successful reset at power-on, a HIGH level must be present on the RST pin while the device is powering-up. This can be applied by the microcontroller, or via a suitable RC power-on reset circuit connected to the RST input. Reset circuit details and conditions during and after a reset are described in Chapter 8.

7.8 Bit rates

The PCD5003A can be configured for data rates of 512, 1200 or 2400 bits/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

7.9 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by means of a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

7.10 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by means of a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

7.11 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address code-word is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next code-word must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{RDE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (at output ROE) before activating the rest of the receiver. This is possible with the UAA2082 receiver which has external biasing for the oscillator circuit.

7.12 Synchronization strategy

In ON status the PCD5003A synchronizes to the POCSAG data stream by means of the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization.

The receiver and oscillator enable outputs (respectively RXE and ROE) are switched accordingly, with the appropriate establishment times (respectively t_{RXON} and t_{ROON}).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to ON status, the decoder is in **switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and sync word. Failure to detect preamble or sync word will cause switching to 'carrier off' mode.

Detection of preamble switches to **preamble receive** mode, in which sync word is looked for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within 1 batch duration 'carrier off' mode is entered.

Upon detection of a sync word the **data receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message code-word reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch, no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message code-word is found to be uncorrectable, 'data-fail' mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **data fail** mode message reception continues normally for 1 batch duration. Upon detection of sync word at the expected position the decoder returns to 'data receive' mode. If sync word again fails to appear, batch synchronization is deemed lost. Call reception is then terminated and 'fade recovery' mode is entered.

The **fade recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ±8 bits).

This is done for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble switches to 'preamble receive' mode, while sync word detection switches to 'data receive' mode. When neither is found within a period of 15 batches, the radio signal is considered lost and 'carrier off' mode is entered.

The purpose of **carrier off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 code-word in every 18 code-words looking for preamble or sync word. By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble switches to 'preamble receive' mode, while sync word detection switches to 'data receive' mode.

7.13 Call termination

Call reception is terminated:

- Upon reception of any address code-word (including idle code-word) requiring no more than single bit error correction
- Upon reception of a correctable address code-word (error type other than '111'; see Table 10) that matches an enabled RIC
- When a forced call termination command is received from an external controller.
- In 'data fail' mode, when a sync word is not found at the expected batch position.

The last method permits an external controller to stop call reception depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter 'data fail' mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

In the event of the terminating code-word matching an enabled RIC, a concatenated call will be started with the call header replacing the terminator of the previous call.

Following call termination, transfer of the data received since the previous sync word period is initiated by means of an interrupt to the external controller.

7.14 Enhanced call termination

The PCD5003A provides an enhanced mode of call termination which is enabled by setting SPF byte 3, bit D7. When enabled, the following call termination conditions apply, in addition to those listed in Section 7.15.

- Reception of two consecutive code-words (excluding sync word), each of which are either uncorrectable or an address code-word with more than one bit in error.

7.15 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per code-word. Each stored call consists of a call header, followed by message data blocks and concluded by a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 4, 6 and 8.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address code-word.

A **Message Data** block contains the data bits from a message code-word plus the type of error correction performed. No deformatting is done on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data have a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in 'data fail' mode) and the type of error correction performed on the terminating code-word.

7.16 Sync word indication

The sync word recognized by the PCD5003A is shown in the call header (bits S3 to S1). The decimal value represents the identifier number in the EEPROM of the UPSW in question. A value of 7 indicates the standard POCSAG sync word.

7.17 Error type indication

Table 10 shows how the different types of detected errors are encoded in the call data output format.

A message code-word containing more than a single bit error (bit E3 = 1) may appear as an address code-word (bit M1 = 0) after error correction. In this event the code-word is processed as message data and does not cause call termination.

7.18 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next code-word.

When the PCD5003A is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

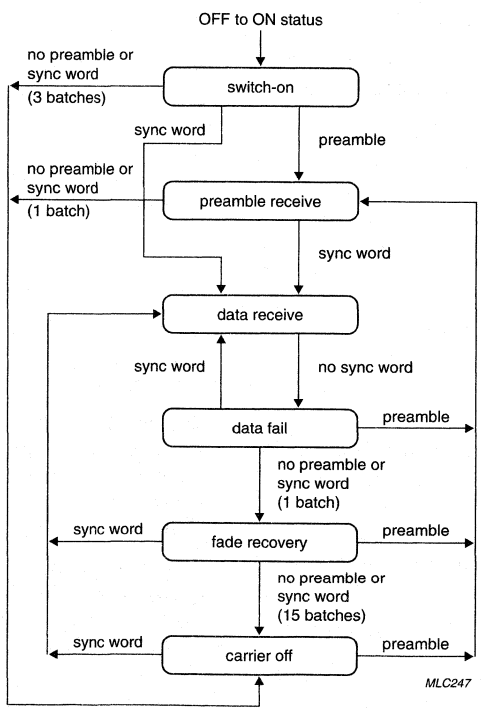


Fig.4 ACCESS® synchronization algorithm.

Table 4 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 5 Call header bit identification

BITS (MSB TO LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any code-word of a previous call received in the same batch was uncorrectable.

Table 6 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 7 Message data bit identification

BITS (MSB TO LSB)	IDENTIFICATION
M2 to M21	message code-word data bits
E3 to E1	detected error type; see Table 10
M1	message code-word flag

Table 8 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 9 Call terminator bit identification

BITS (MSB TO LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
E3 to E1	detected error type; see Table 10; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data code-word in the terminating batch was uncorrectable, while in 'data receive' mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in 'data fail' mode.

Table 10 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors; correct code-word	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	
1	0	1	4-bit burst error and parity error	3 (e.g. 1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable code-word	3 or more

Note

1. POCSAG code allows a maximum of three bit errors to be detected per code-word.

Call termination can occur on reception of an address code-word (or even a message code-word if in enhanced call termination mode) or when a sync word is not detected while in the 'data fail' mode.

7.19 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 11).

7.20 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I^2C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be left by means of a reset or an I^2C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

7.21 Demodulator quick charge

Two modes of operation are available that determine the periods when the DQC is set.

The operating mode is selected by EEPROM programming of SPF byte 3, bit D5:

- **Mode 0 (D5 = 0)**: DQC is active (logic HIGH) during the receiver establishment time t_{RXE} in all ACCESS modes except data receive and data fail. During switch-on, DQC is active for 1 code-word duration.
- **Mode 1 (D5 = 1)**: DQC is active during sync word detection in all ACCESS modes. During switch-on and preamble receive modes, DQC is active continuously.

The timing of DQC is as follows: (see Fig.5).

- **Mode 0**: Set along with RXE output (time t_{RXE} before the first code-word is expected); cleared during the second bit of the code-word following t_{RXE}.
- **Mode 1**: Set during the second bit of the sync word; cleared after the last bit of the sync word.

Note: During switch-on, t_{RXE} is not used: RXE and DQC are switched on immediately.

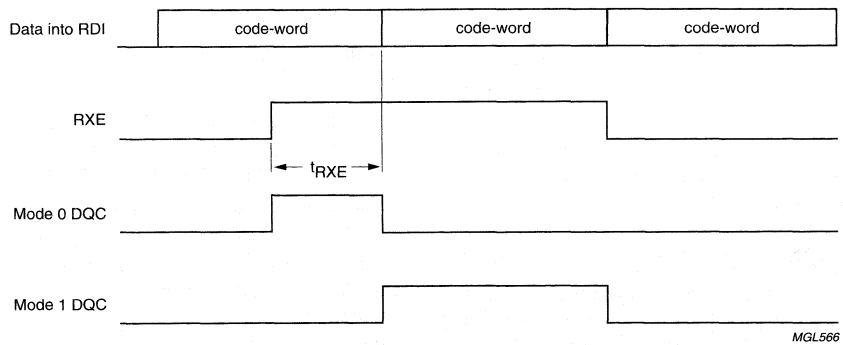


Fig.5 Example of DQC timing.

7.22 Battery condition input

A logic signal from an external sense circuit signalling battery condition can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH-level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 11 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 22).

7.23 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5003A is switched from OFF to ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 25).

Data bits on ZSD change on the falling flanks of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is given in Fig.6.

The data output timing is synchronous, but has a pause in the bit stream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 12. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is given in Fig.13.

Table 12 Synthesizer programming pause

BIT RATE (bit/s)	t_p (CLOCKS)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

7.24 Serial microcontroller interface

The PCD5003A has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5003A is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111). Together with the R/$\overline{W}$ bit the first byte of an I²C-bus message then becomes 4EH (write) or 4FH (read).

Data transmission requires 2 lines: SDA (serial data) and SCL (serial clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a START condition (S: SCL = 1, SDA = ↓) and terminated by a STOP condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the STOP condition can be replaced with a new START condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit ACK (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is shown in Fig.7. Formats for master/slave communication are shown in Fig.8.

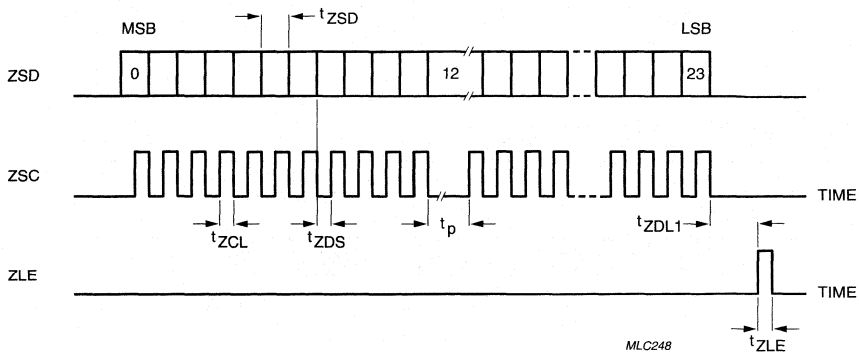


Fig.6 Synthesizer interface timing.

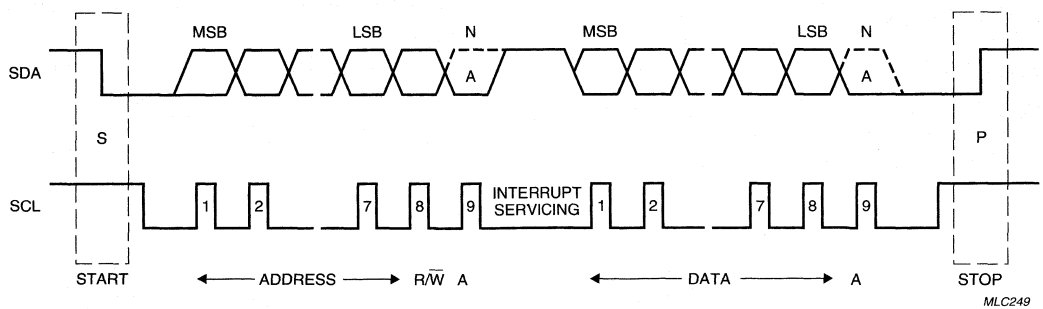
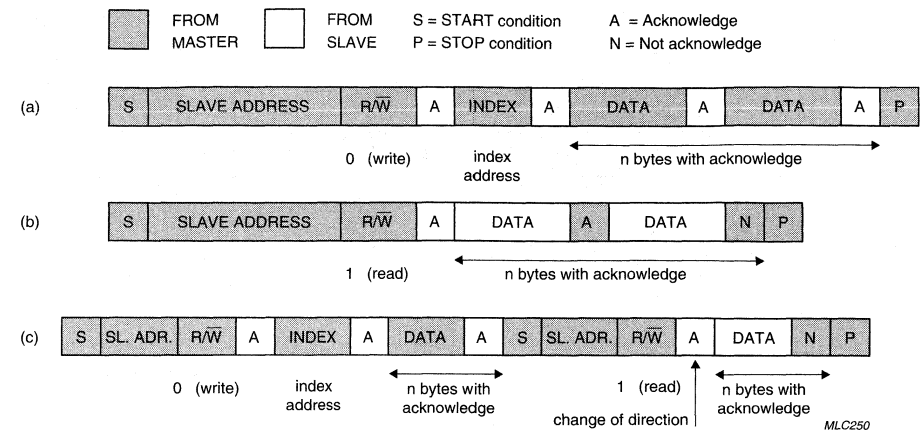


Fig.7 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.8 Message types.

7.25 Decoder I²C-bus access

All internal access to the PCD5003A takes place via the I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 13 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and organized as a matrix. The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus write message to the PCD5003A must start with its slave address, followed by the index address of the memory element to be accessed. An I²C-bus read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.8.

As a slave the PCD5003A cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 13 Index register

ADDRESS[1]	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real-time clock: seconds	R/W
02H	real-time clock: $^1/_{100}$ second	R/W
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/W
08H	RAM read address pointer	R/W
09H	RAM data output	R
0AH	EEPROM data input/output	R/W
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

7.26 External interrupt

The PCD5003A can signal events to an external controller via an interrupt signal on output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position, if data fail mode (short fade recovery mode in APOC1) is not active.

The interrupt output INT is reset after completion of a status read operation.

7.27 Interrupt Masking

In the PCD5003A certain interrupts can be suppressed by masking via the control register. This feature prevents unnecessary wake-up actions of the microcontroller causing battery life reduction.

The following interrupts can be masked:

- **Out-of-Range (status bit D5)**: change of state interrupt, masked by setting control register bit D5
- **BAT/RXE monitoring (status bit D6)**: change of state interrupt (source selected by control register bit D2), masked by setting control register bit D6
- **Periodic Timer (status bit D7)**: timer overflow interrupt, masked by setting control register bit D7.

Although no interrupts are generated by these conditions when masked via the control register, the corresponding status bits are normally updated and available via the status register. At reset the control register is cleared, causing all interrupts to be enabled.

7.28 Status/control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 14 and 15 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 14).

Status bit D0 is set when call reception is started by detection of an enabled RIC (user address). This does not generate an interrupt.

Table 14 Status register (00H; read)

BIT(1)	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received
	1 0	reserved for future use
	1 1	reserved for future use
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different: data to be read
	1 0	RAM read/write pointers equal: no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 15 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5	1	out-of-range interrupt masked
D6	1	BAT/RXE monitor interrupt masked
D7	1	periodic timer interrupt masked

7.29 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. Next, an immediate interrupt is generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

7.30 Out-of-range Indication

The out-of-range condition occurs when entering fade recovery or 'carrier off' mode. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE ↓ 0). Every change of state in bit D5 generates an interrupt.

7.31 Real-time clock

The PCD5003A provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period: it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is shown in Fig.15.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real-time clock counter runs continuously irrespective of the operating condition of the PCD5003A. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read or written via the I^2C-bus. The bit allocation of both registers is shown in Tables 16 and 17.

Table 16 Real-time clock; seconds register (01H; read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written; undetermined when read
D7	X	not used: ignored when written; undetermined when read

Table 17 Real-time clock; $1/100$ second register (02H; read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	0.01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written; undetermined when read

7.32 Periodic interrupt

A periodic interrupt can be realised with the periodic interrupt counter. This 8-bit counter is incremented every $1/100$ second and produces an interrupt when it reaches the value stored in the periodic interrupt modulus register. The counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the modulus register. Writing a zero will stop interrupt generation immediately and will halt the periodic interrupt counter after 2.55 seconds.

The modulus register is write-only, the counter register can only be read. Both registers have the same index address (05H).

7.33 Received call delay

Call reception causes both the periodic interrupt modulus and the counter register to be reset.

Since the periodic interrupt counter runs for another 2.55 seconds after a reset, the received call delay (in $^1/_{100}$ second units) can be determined by reading the counter register.

Table 18 Alert set-up register (04H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7, D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.9(a)
	0 1	POCSAG alert pattern FC = 01, see Fig.9(b)
	1 0	POCSAG alert pattern FC = 10, see Fig.9(c)
	1 1	POCSAG alert pattern FC = 11, see Fig.9(d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address code-word, which designate the POCSAG call type as shown in Table 1.

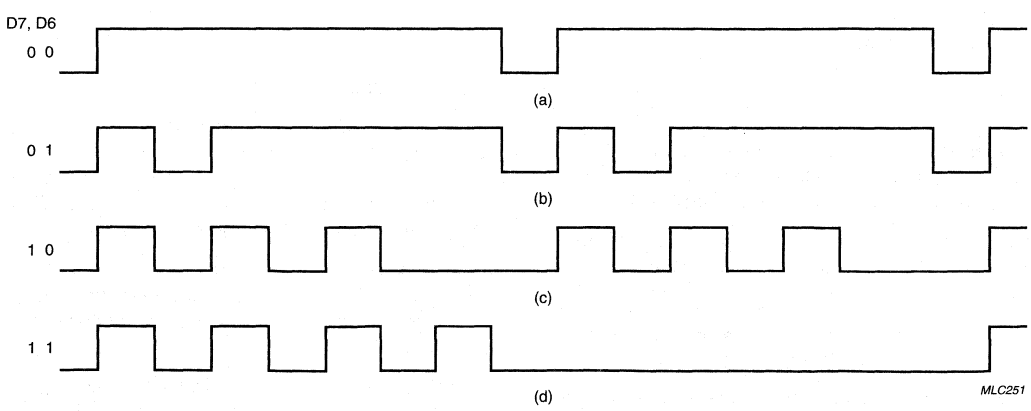


Fig.9 POCSAG alert patterns.

7.34 Alert generation

The PCD5003A is capable of controlling 3 different alert transducers: acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 18.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

Automatic generation via all alert outputs of the POCSAG alert pattern matching the received call type can be enabled by SPF programming (SPF byte 3, bit D2).

7.35 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is started an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation.

7.36 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 of the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 seconds (ATL), followed by 12 seconds at HIGH level (ATL + ATH). When D1 is set, the full 16 seconds are at HIGH level. An interrupt is generated upon expiry of the full alert time.

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advised to reset the last bit of the previous pattern to prevent unwanted audible level changes.

7.37 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported: LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

7.38 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

7.39 Warbled alert

When enabled by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

7.40 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

7.41 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from the position it was left at. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated synchronous with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

7.42 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

7.43 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address code-word (see Table 1). The timing of these alert patterns is shown in Fig.10.

When enabled by SPF programming (SPF byte 3, bit D2) standard POCSAG alerts will automatically be generated on outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address code-word.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

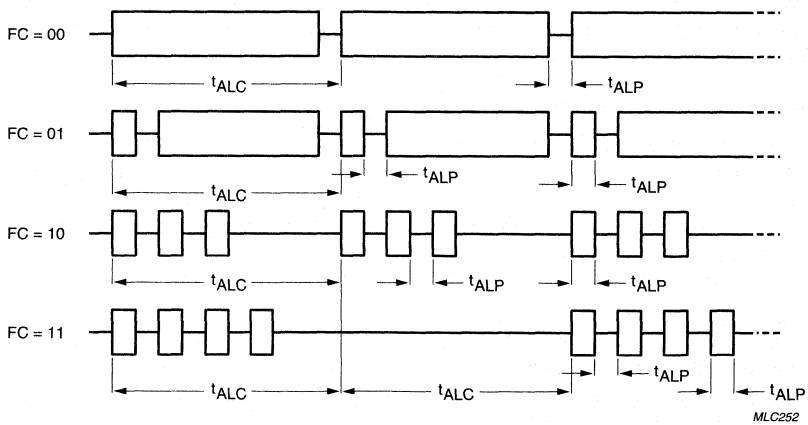


Fig.10 POCSAG alert timing.

7.44 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per code-word) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I²C-bus interface. The RAM is accessed indirectly by means of a read address pointer and a data output register. A write address pointer indicates the first byte after the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0): data is available for reading, if data fail mode (short fade recovery mode in APOC1) is not active
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the code-word following the 'RAM full' interrupt.

7.45 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, as the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH.

Bit D7 (MSB) is not used and its value is undefined when read.

7.46 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

It can be accessed for writing as well as reading.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H.

Bit D7 (MSB) is not used; it is ignored when written and undefined when read.

7.47 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer. It can only be read, each read operation causing an increment of the RAM read address pointer.

7.48 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous as can be seen in Fig.11, which shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes is available for general purpose storage.

7.49 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read or written via the EEPROM data I/O register.

The EEPROM address pointer contains two counters, for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

7.50 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written or read via the EEPROM Data I/O register. Each access automatically increments the EEPROM address pointer.

7.51 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advised to switch to OFF state before accessing the EEPROM.

The EEPROM cannot be written unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum programming supply voltage $V_{DD(prog)}$ is required (2.0 V typ.). The programming supply current ($I_{DD(prog)}$) needed during writing will be ≈ 500 μA.

Any modified SPF settings (bytes 0 to 3) only take effect after a decoder reset. Modified identifiers are active immediately.

7.52 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single-byte or block reads are permitted.

7.53 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of maximum 7.5 ms is required to complete the programming operation internally. During this time the external microcontroller may generate an I²C-bus stop condition. If another I²C-bus transfer is started the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in the control register must be reset.

7.54 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

7.55 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus stop condition. Next, the EEPROM programming enable bit (D1) in the control register must be reset.

Any bytes received of the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

7.56 Unused EEPROM locations

A total of 20 EEPROM bytes is available for general purpose storage (see Table 19).

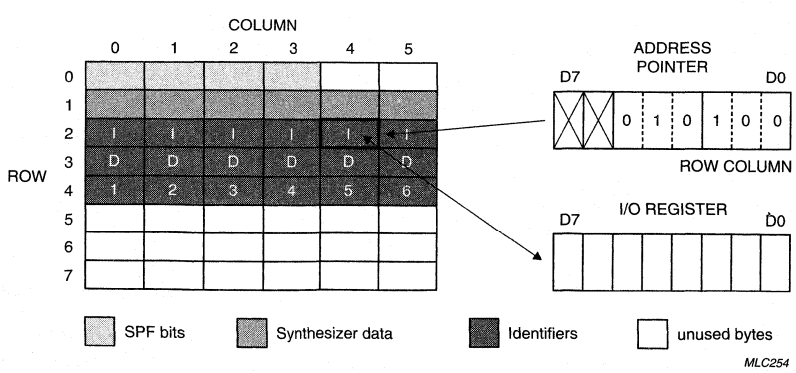


Fig.11 EEPROM organization and access.

Table 19 Unused EEPROM addresses

ROW	HEX
0	04 and 05[1]
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

7.57 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 20 to 24. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

The contents of SPF (bytes 0 to 3) are read into the associated logic only when the decoder is reset (HIGH level in input RST).

Table 20 Special programmed functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	reserved for future use; logic 0 when read
D1	X	reserved for future use
D2	X	reserved for future use
D3	X	reserved for future use
D4	X	reserved for future use
D5	X	reserved for future use
D6	X	reserved for future use; logic 0 when read
D7	1	received data inversion enabled

Table 21 Special programmed functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms receiver establishment time (nominal); note 1
	1 0	15 ms receiver establishment time (nominal); note 1
	1 1	30 ms receiver establishment time (nominal); note 1
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms oscillator establishment time (nominal); note 1
	1 0	40 ms oscillator establishment time (nominal); note 1
	1 1	50 ms oscillator establishment time (nominal); note 1
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (data is output via ZSD, ZSC and ZLE at decoder switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 22 shows the values for the various bit rates.

Table 22 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 BITS/s	1024 BITS/s	1200 BITS/s	2400 BITS/s
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5.0 ms (6 bits)	5.0 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10.0 ms (12 bits)	10.0 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20.0 ms (24 bits)	20.0 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40.0 ms (48 bits)	40.0 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 23 Special programmed functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real-time clock reference
	0 1	50 Hz square wave
	1 0	2 Hz
	1 1	$^1/_{60}$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	X X	reserved for future use

Table 24 Special programmed functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz acoustic alerter frequency
	1 0	4096 Hz acoustic alerter frequency
	1 1	3200 Hz acoustic alerter frequency
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	0	DQC mode 0
	1	DQC mode 1
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	0	standard call termination
	1	enhanced call termination

7.58 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting from address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

7.59 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5003A can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW).

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Only the last 4 identifiers (numbers 3 to 6) can be programmed as a UPSW. Identifiers 1 and 2 always represent RICs. A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

The standard POCSAG sync word is always enabled and has identifier number 7.

Table 26 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 27.

Table 25 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

Table 26 Identifier storage allocation (EEPROM address 10H to 25H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 27 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG code-word (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	reserved for future use, logic 0 when read

Notes

1. The bit numbering corresponds with the numbering in a POCSAG code-word: bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0; bits 2 to 19 contain the identifier bit pattern; they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB : FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

7.60 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller on output V_{PO}. An external ceramic capacitor of typical 100 nF is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

7.61 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5003A.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. This could be the on-chip voltage doubler output V_{PO} if required. When the microcontroller has a separate (regulated) supply this separate supply voltage should be connected to V_{PR}.

The level-shifted interface lines are: RST, DON, ALC, REF and INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by means of the standard external pull-up resistors.

7.62 Signal test mode

A special 'signal test' mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5003A.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The 'signal test' mode is activated/deactivated by SPF programming.

8 OPERATING INSTRUCTIONS

8.1 Reset conditions

When the PCD5003A is reset by applying a HIGH-level on input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- All interrupts enabled
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high impedance
- SDA, SCL inputs high impedance
- Voltage converter disabled.

Within t_{RSU} after release of the reset condition (RST LOW) the programmed functions are activated. The settings affecting the external operation of the PCD5003A are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

8.2 Power-on reset circuit

During power-up of the PCD5003A a HIGH level of minimum duration t_{RST} = 50 µs must be applied to pin RST. This is to prevent EEPROM corruption which might otherwise occur because of the undefined contents of the control register.

The reset signal can be applied by the external microcontroller or by an RC power-on reset circuit on pin RST (C to V_{PR}, R to V_{SS}). Such an RC-circuit should have a time constant of at least $3t_{RST}$ = 150 µs.

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply) which could be used together with a suitable external capacitor connected to V_{PR} to create a power-on reset signal. However, since this pull-down resistor varies considerably with processing and supply voltage, the resulting time constant is inaccurate.

A more accurate reset duration can be realised with an additional external resistor connected to V_{SS}. Recommended minimum values in this case are C = 2.2 nF and R = 100 kΩ (see Fig.16).

8.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 second (typ. 800 ms). It is advised to apply a reset condition at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 µs.

During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

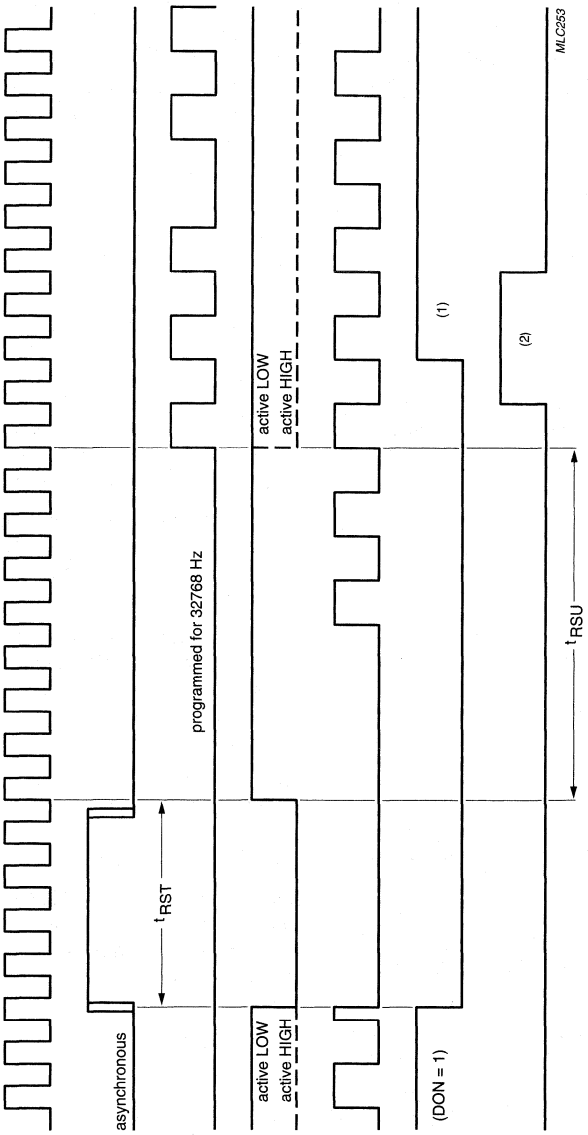
Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is shown in Fig.12. The start-up timing including synthesizer programming is given in Fig.13.

8.4 Initial programming

A newly-delivered PCD5002A has EEPROM contents which are undefined. The EEPROM should therefore be programmed, followed by a reset to activate the SPF settings, before any attempt is made to use the device.



(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.12 Reset timing.

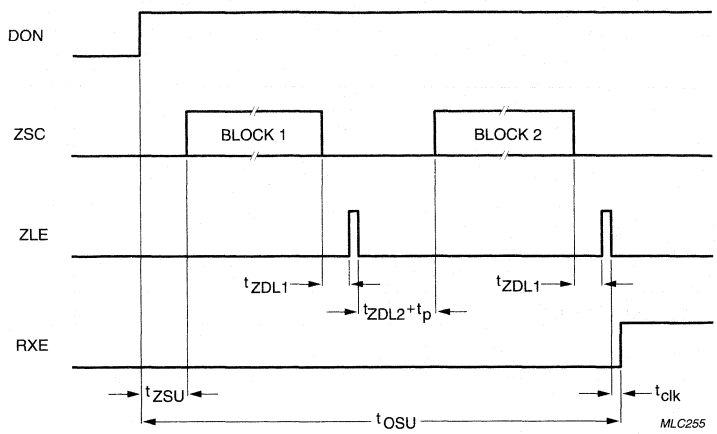


Fig.13 Start-up timing including synthesizer programming.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		–	250	mW
P_{out}	power dissipation per output		–	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

10 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	voltage converter disabled	1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
$V_{DD(prog)}$	programming supply voltage	voltage converter disabled	2.0	–	6.0	V
		voltage converter enabled	2.0	–	3.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	DON = V_{DD}; note 1	–	50.0	80.0	µA
$I_{DD(prog)}$	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW-level input voltage					
	RDI and BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC and RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA and SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage					
	RDI and BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC and RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA and SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW-level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH-level input current	T_{amb} = 25 °C				
	TS1 and TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI and BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI and BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC and RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW-level output current	T_{amb} = 25 °C				
	VIB and LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT and REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC and ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE and DQC	V_{OL} = 0.3 V	80	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB and LED	V_{OH} = 0.7 V	−0.6	–	−2.4	mA
	ATH	V_{OH} = 0.7 V	−3.0	–	−11.0	mA
	INT and REF	V_{OH} = 2.4 V	−80	–	–	µA
	ZSD, ZSC and ZLE	V_{OH} = 2.4 V	−60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	−0.5	µA
	ROE, RXE and DQC	V_{OH} = 2.4 V	−600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: f_{ref} = 1/60 Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 21).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter 9).
3. When ATL (open-drain output) is not activated it is high impedance.

11 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = V_{PO}; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7 V; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2.0 V; I_{PO} = −250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2.0 V; V_{PO} = 2.7 V	−400	−650	–	µA
		V_{DD} = 3.0 V; V_{PO} = 4.5 V	−650	−900	–	µA

12 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent. Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF. Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	UNIT
C_{XO}	output capacitance XTAL2		–	10	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	µS

13 EEPROM CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	UNIT
N_{EW}	erase/write cycles		1000	10000	
t_{DR}	data retention time	T_{amb} = 70 °C; note 1	10	–	years

Note

1. Retention cannot be guaranteed for naked dies (PCD5003AU/10).

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH and LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low-level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high-level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low -level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high-level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real-time clock reference						
f_{ref}	real-time clock reference frequency	SPF byte 02H; bits				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real-time clock reference pulse duration	all reference frequencies except 50 Hz (square wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE, ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I^2C-bus interface						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SDA, SCL rise time		–	–	300	ns
t_f	SDA, SCL fall time		note 3	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		0.6	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time	see Fig.14	–	–	100	µs
t_{DI1}	data input logic 1 duration	see Fig.14	t_{BIT}	–	∞	
t_{DI0}	data input logic 0 duration	see Fig.14	t_{BIT}	–	∞	
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 0 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	code-word duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	code-word duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	code-word duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 4	1	–	2	bits
f_{ZSC}	output clock frequency	note 5	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 5	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal: 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.15.
2. 50 Hz reference signal: square-wave.
3. The fall time may be faster than prescribed in the I^2C-bus specification for very low load capacitance values. To increase the fall time external capacitance is required.
4. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
5. Nominal values; pause in 12th data bit (see Table 12).

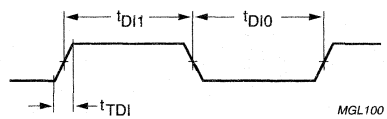


Fig.14 Data input timing.

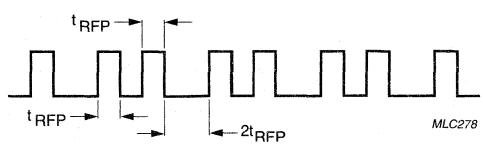
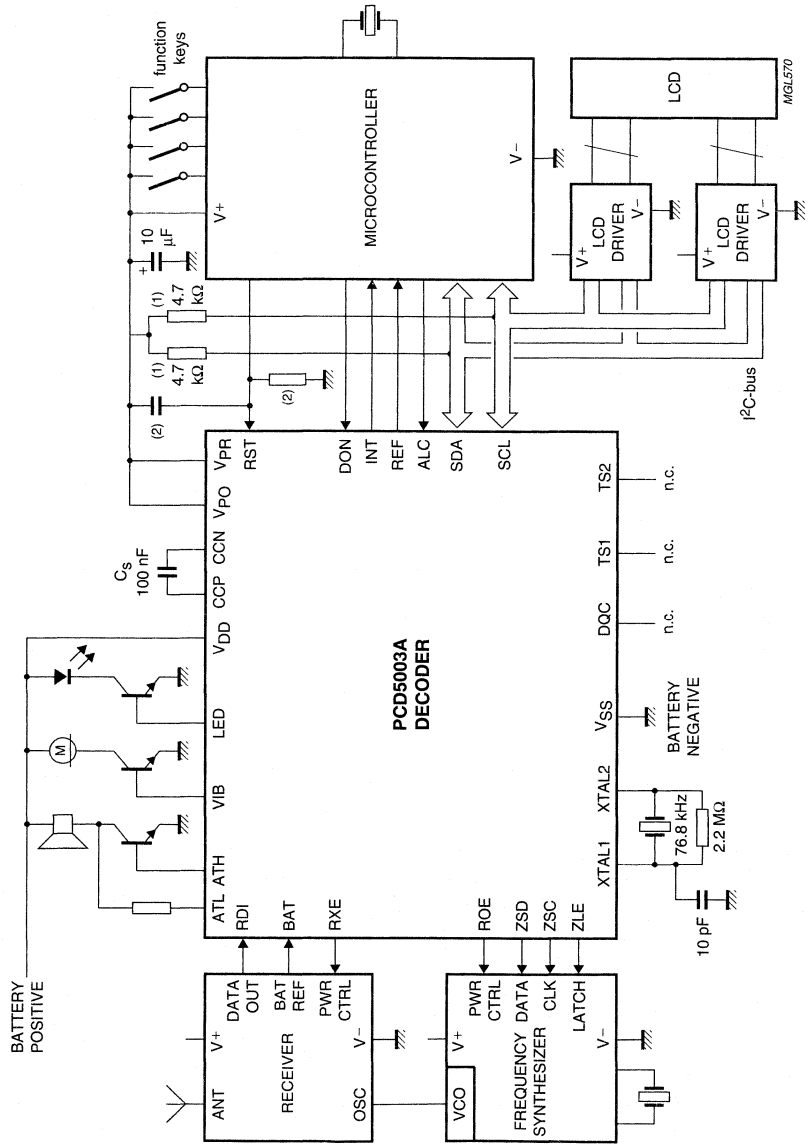


Fig.15 Timing of the 32768 Hz reference signal.

15 APPLICATION INFORMATION



(1) Value depends on number of devices attached.
(2) Values should be chosen to give a time constant of at least 150 µs. C = 2.2 nF and R = 100 kΩ are recommended.

Fig.16 Typical application example (display pager).

CONTENTS

FLEX™ Pager Decoder PCD5008

1 FEATURES

- FLEX™ paging protocol signal processor
- 16 programmable user address words
- 16 fixed temporary addresses
- 1600, 3200 and 6400 bits/s decoding
- Any-phase or single-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low current power-down mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX™ fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- Low cost LQFP32 plastic package
- Operates using a 76.8 kHz crystal
- Very low power consumption
- Operates at low supply voltage.

2 APPLICATIONS

- Numeric FLEX™ pagers
- Alphanumeric FLEX™ pagers
- Remote metering
- Car security systems
- Personal digital assistants.

3 GENERAL DESCRIPTION

This data sheet describes the operation of the PCD5008 integrated paging decoder. It is fully compatible with the Motorola FLEXchip™ IC.

The PCD5008, also referred to as the decoder, simplifies implementation of a FLEX™ paging device, by being able to interface with several off-the-shelf paging receivers and host microcontrollers/processors. Its primary function is to process information received and demodulated from a FLEX™ radio paging channel, select messages addressed to the paging device and communicate the message information to the host.

Motorola FLEXstack™ software, installed on the product host processor, communicates with the PCD5008 and interprets the codewords that are passed to the host.

The PCD5008 operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when no message is being received.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	2.2	3.6	V
I_{DD}	supply current	see Sections 10 and 12	–	6.4	–	µA
T_{amb}	operating ambient temperature		–25	+25	+70	°C
f_{EXTAL}	external clock frequency		–	76.8	–	kHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5008H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

6 BLOCK DIAGRAM

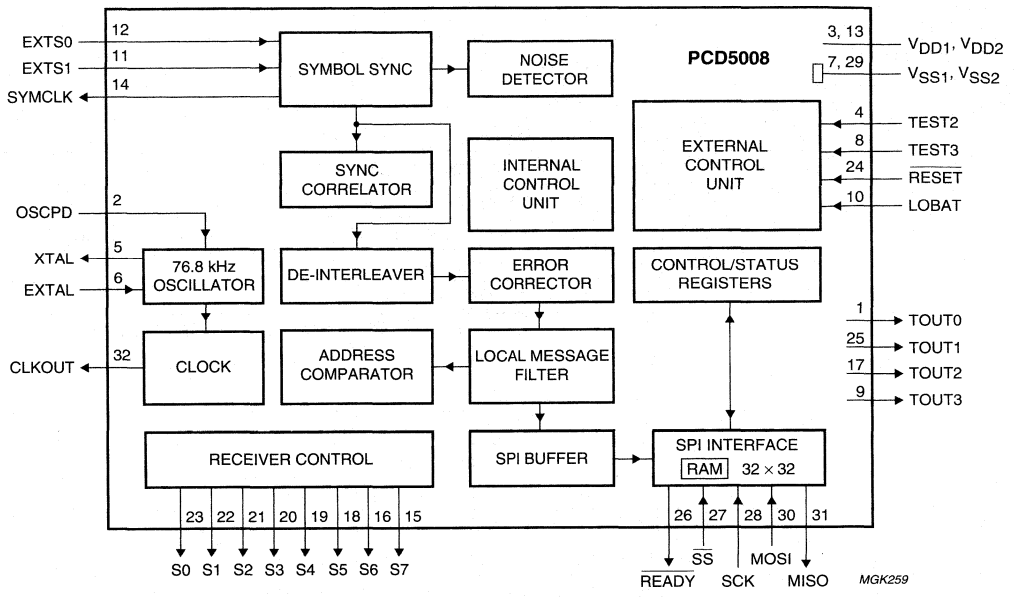


Fig.1 Functional block diagram for PCD5008 pager decoder.

7 PINNING

SYMBOL	PIN	I/O	PAD COORDINATE X/Y; note 1	DESCRIPTION
TOUT0	1	O	−1405/1088	3-state test output; note 2
OSCPD	2	I	−1405/816	internal oscillator power-down; connected to V_{SS} when using the internal oscillator, connected to V_{DD} when using an external source
V_{DD1}	3	−	−1405/563	supply voltage
TEST2	4	I	−1405/306	manufacturing test mode input pin; has to be connected to V_{SS}
XTAL	5	O	−1405/76	76.8 kHz crystal oscillator output
EXTAL	6	I	−1405/−404	76.8 kHz crystal oscillator input or external clock input
V_{SS1}	7	−	−1405/−648	ground supply
TEST3	8	I	−1405/−1104	manufacturing test mode input pin; has to be connected to V_{SS}
TOUT3	9	O	−1125/−1400	3-state test output; note 2
LOBAT	10	I	−863/−1400	low battery voltage detect input
EXTS1	11	I	−633/−1400	most significant bit (MSB) of the symbol currently being decoded
EXTS0	12	I	−398/−1400	least significant bit (LSB) of the symbol currently being decoded
V_{DD2}	13	−	134/−1400	supply voltage
SYMCLK	14	O	569/−1400	recovered symbol clock output
S7	15	O	829/−1400	receiver control output port, 3-state
S6	16	O	1084/−1400	receiver control output port, 3-state
TOUT2	17	O	1405/−1093	3-state test output; note 2
S5	18	O	1405/−718	receiver control output port, 3-state
S4	19	O	1405/−398	receiver control output port, 3-state
S3	20	O	1405/−93	receiver control output port, 3-state
S2	21	O	1405/202	receiver control output port, 3-state
S1	22	O	1405/502	receiver control output port, 3-state
S0	23	O	1405/812	receiver control output port, 3-state
$\overline{\text{RESET}}$	24	I	1405/1114	active LOW reset input
TOUT1	25	O	1051/1400	3-state test output; note 2
$\overline{\text{READY}}$	26	O	721/1400	output driven LOW when the PCD5008 is ready for an SPI packet
$\overline{\text{SS}}$	27	I	404/1400	slave select input for SPI communications
SCK	28	I	149/1400	serial clock input for SPI communications
V_{SS2}	29	−	−100/1400	ground supply
MOSI	30	I	−516/1400	data input for SPI communications
MISO	31	O	−789/1400	data output for SPI communications, 3-state
CLKOUT	32	O	−1084/1400	38.4 kHz clock output (derived from 76.8 kHz oscillator)

Notes

1. The pad coordinates are given in μm relating to the centre of the chip and are used in case of naked die delivery.
2. These test outputs may be either left unconnected or connected to V_{SS} in the application.

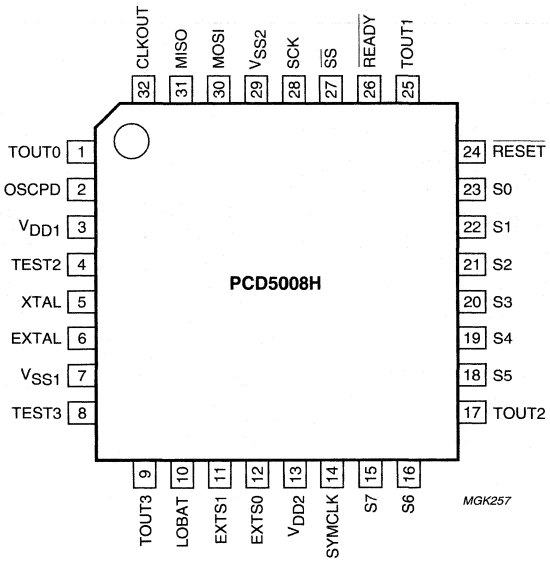


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The PCD5008 simplifies implementation of a FLEX™ paging device by interfacing with off-the-shelf components such as a paging receiver and a microcontroller or microprocessor (called a host). The PCD5008 is fully compatible with FLEXstack™ software which provides a complete, platform independent, software driver for the PCD5008.

The PCD5008 fully supports all non-roaming aspects of the FLEX™ protocol (version G1.8), and can operate in either single-phase or any-phase mode. The PCD5008 supports FLEX™ dynamic grouping, allowing up to 16 temporary addresses to be enabled simultaneously. It is also capable of retrieving real time information from a FLEX™ channel.

The PCD5008 connects to any receiver capable of providing a 2-bit digital signal. The PCD5008 operates the paging receiver in an efficient power consumption mode. The PCD5008 has 8 receiver control lines used for warming up, operating and shutting down a receiver in stages.

The PCD5008 has the ability to detect a battery-low signal from an external detector during the receiver control sequences.

The PCD5008 carries out the following functions:

- Synchronises to a FLEX™ data stream
- Processes received, demodulated information
- Performs de-interleaving and error correction
- Selects calls addressed to the paging device using up to 16 programmable addresses
- Communicates the message information to the host.

The PCD5008 interfaces to a host through a serial peripheral interface (SPI). The host can then interpret the message information in an appropriate manner (numeric, alphanumeric, binary, etc.). This function is provided by the FLEXstack™ software.

The PCD5008 enables the host to operate in a low power mode when no message information for the paging device is being received. It has a 38.4 kHz clock output capable of driving other devices, and has a 1-minute timer that offers low-power support for a real-time clock function on the host. The host can use receiver control lines which are not required by the receiver as expansion ports to control other peripheral devices.

8.2 Clocking, reset and start-up

8.2.1 OSCILLATOR

The PCD5008 uses an inverting crystal oscillator. The clock signal for the internal circuitry is derived via an amplifier from the oscillator input pin EXTAL. Alternatively, an external clock signal can be fed in at input pin EXTAL. In this case the internal oscillator can be disabled by pulling the OSCPD input pin HIGH.This reduces current consumption and routes EXTAL directly to the internal clock signal. When using a crystal, an external feedback resistor and the load capacitances need to be connected to pins EXTAL and XTAL (Fig.18). See Section 12 for the recommended crystal parameters and the specification of the oscillator transconductance to guarantee correct start-up.

8.2.2 RESET AND START-UP CONDITIONS

The PCD5008 is reset by pulling the $\overline{\text{RESET}}$ input LOW. After releasing the $\overline{\text{RESET}}$ by pulling it HIGH, the PCD5008 counts 76800 clock cycles (typically 1 second) before pulling $\overline{\text{READY}}$ LOW to indicate that the decoder is ready for configuration via the SPI.

See Fig.3 and Section 11 for the PCD5008 timing specifications when power is applied.

See Fig.4 and Section 11 for the PCD5008 timing specifications when it is reset.

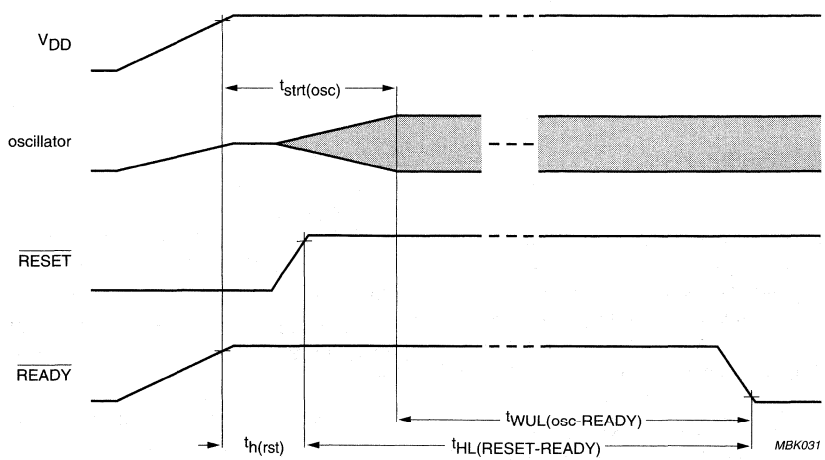


Fig.3 Start-up timing.

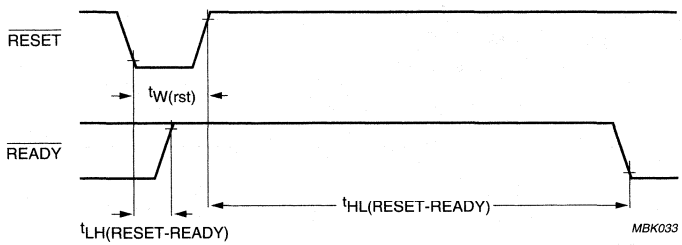


Fig.4 Reset timing.

8.3 Serial peripheral interface (SPI)

8.3.1 General

All data communication between the PCD5008 and the host is done via the SPI using 32-bit data packets at data rates up to 1 Mbits/s. SPI transfers are full-duplex and can be initiated by either the host which acts as the SPI master providing the data clock for packet transfer, or the PCD5008 as an SPI slave.

The host can send packets to configure or control the PCD5008 or a checksum packet to validate SPI communication (Section 8.4.2). The PCD5008 buffers data packets, relating to received data, into a 32 packet transmit buffer. The PCD5008 can send either a status packet, a part ID packet, or packets from the transmit buffer. In the event of a buffer overflow, the PCD5008 stops decoding and clears the transmit buffer.

8.3.2 SPI interconnect

Connection on the PCD5008 consists of a $\overline{\text{READY}}$ pin and 4 SPI pins ($\overline{\text{SS}}$, SCK, MOSI and MISO):

$\overline{\text{READY}}$: output signal; indicates that data is available from the PCD5008

$\overline{\text{SS}}$: SPI select; used as PCD5008 chip select

SCK: serial clock; output from the host used for clocking data

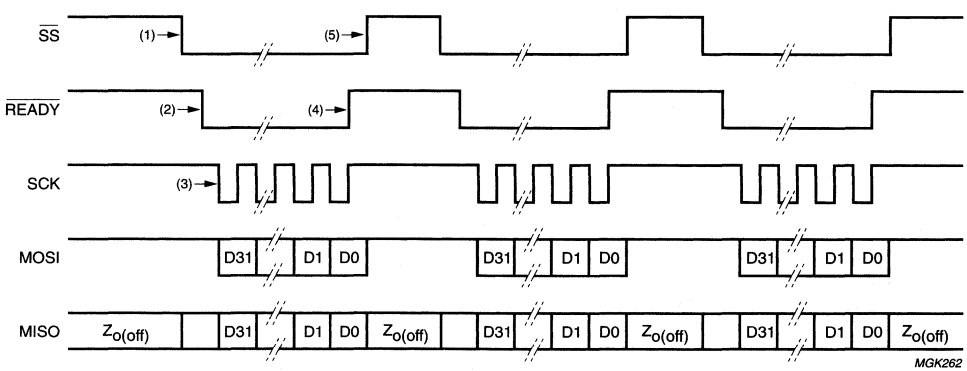
MOSI: master output slave input; data output from the host

MISO: master input slave output; data output from the PCD5008.

8.3.3 SPI TRANSFER INITIATED BY THE HOST

The following steps occur when the host initiates an SPI packet transfer, see Fig.5 for event timings:

1. The host selects the PCD5008 by driving the $\overline{SS}$ pin LOW.
2. The PCD5008 indicates that it is ready to start the SPI transfer by driving the $\overline{READY}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host waits until the $\overline{READY}$ line is pulled HIGH, then de-selects the PCD5008 SPI by driving the $\overline{SS}$ pin HIGH.
6. The first 5 steps are repeated for each additional packet.



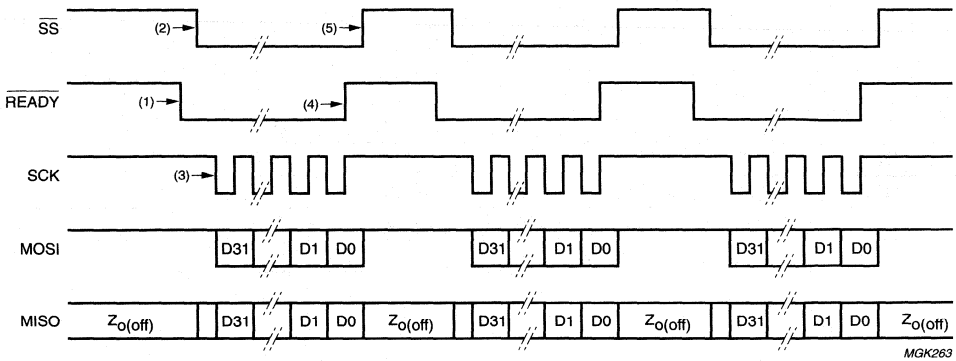
Numbers within parenthesis refer to sequence numbers, see Section 8.3.3.

Fig.5 Typical multiple SPI transfers initiated by the host.

8.3.4 SPI TRANSFER INITIATED BY THE DECODER

The following steps occur when the PCD5008 initiates an SPI packet transfer, see Fig.6 for event timings:

1. The PCD5008 initiates the SPI transfer by driving the $\overline{READY}$ pin LOW.
2. If the PCD5008 is not already selected, the host selects the PCD5008 SPI by driving the $\overline{SS}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host may then either de-select the SPI interface of the PCD5008 (Fig.7) by driving the $\overline{SS}$ pin HIGH or maintain $\overline{SS}$ LOW to continue sending packets to the PCD5008.



Numbers within parenthesis refer to sequence numbers, see Section 8.3.4.

Fig.6 Typical multiple SPI transfers initiated by the PCD5008.

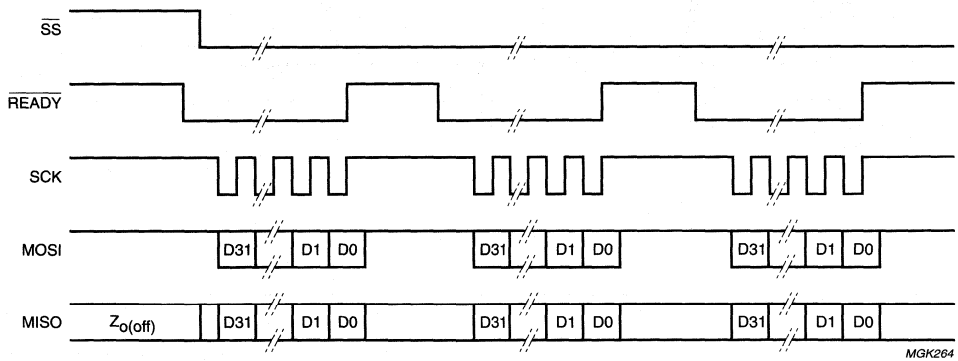


Fig.7 Multiple SPI transfers initiated by the PCD5008 with $\overline{SS}$ maintained LOW.

8.3.5 SPI PACKET FORMAT

SPI data packets consist of an 8-bit ID (byte 3), followed by 24 bits of information (byte 2 to byte 0). See Table 1, note that bit 7 of byte 3 is the first bit on the bus.

8.3.6 SPI TIMING

See Fig.8 and Chapter 11 for the timing specifications of the SPI.

Table 1 Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	D31	D30	D29	D28	D27	D26	D25	D24
2	D23	D22	D21	D20	D19	D18	D17	D16
1	D15	D14	D13	D12	D11	D10	D9	D8
0	D7	D6	D5	D4	D3	D2	D1	D0

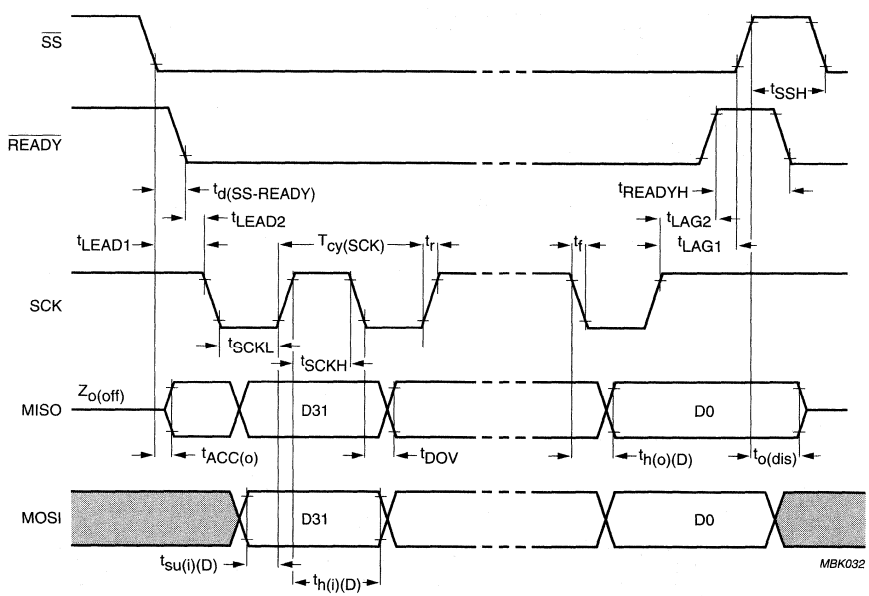


Fig.8 SPI timing.

8.3.7 HOST-TO-DECODER PACKETS OVERVIEW

This section summarises the packets which can be sent from the host to the decoder.

Table 2 Host-to-decoder packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	checksum	8.4.6
01	configuration	8.4.4
02	control	8.4.7
03	all frame mode	8.8.3
04 to 0E	reserved (host should never send)	–
0F	receiver line control	8.5.7
10	receiver control configuration (off setting)	8.5.4
11	receiver control configuration (warm-up 1 setting)	8.5.5.3
12	receiver control configuration (warm-up 2 setting)	8.5.5.3
13	receiver control configuration (warm-up 3 setting)	8.5.5.3
14	receiver control configuration (warm-up 4 setting)	8.5.5.3
15	receiver control configuration (warm-up 5 setting)	8.5.5.3
16	receiver control configuration (3200 sps sync setting)	8.5.6.2
17	receiver control configuration (1600 sps sync setting)	8.5.6.2
18	receiver control configuration (3200 sps data setting)	8.5.6.2
19	receiver control configuration (1600 sps data setting)	8.5.6.2
1A	receiver control configuration (shut-down 1 setting)	8.5.8.1
1B	receiver control configuration (shut-down 2 setting)	8.5.8.1
1C to 1F	special (ignored by decoder)	–
20	frame assignment (frames 112 to 127)	8.6.7
21	frame assignment (frames 96 to 111)	8.6.7
22	frame assignment (frames 80 to 95)	8.6.7
23	frame assignment (frames 64 to 79)	8.6.7
24	frame assignment (frames 48 to 63)	8.6.7
25	frame assignment (frames 32 to 47)	8.6.7
26	frame assignment (frames 16 to 31)	8.6.7
27	frame assignment (frames 0 to 15)	8.6.7
28 to 77	reserved (host should never send)	–
78	user address enable	8.6.6
79 to 7F	reserved (host should never send)	–
80	user address assignment (user address 0)	8.6.6
81	user address assignment (user address 1)	8.6.6
82	user address assignment (user address 2)	8.6.6
83	user address assignment (user address 3)	8.6.6
84	user address assignment (user address 4)	8.6.6
85	user address assignment (user address 5)	8.6.6

PACKET		
ID (HEX)	**TYPE**	**SECTION**
86	user address assignment (user address 6)	8.6.6
87	user address assignment (user address 7)	8.6.6
88	user address assignment (user address 8)	8.6.6
89	user address assignment (user address 9)	8.6.6
8A	user address assignment (user address 10)	8.6.6
8B	user address assignment (user address 11)	8.6.6
8C	user address assignment (user address 12)	8.6.6
8D	user address assignment (user address 13)	8.6.6
8E	user address assignment (user address 14)	8.6.6
8F	user address assignment (user address 15)	8.6.6
90 to FF	reserved (host should never send)	–

8.3.8 DECODER-TO-HOST PACKETS OVERVIEW

This section summarises the packets which can be sent from the PCD5008 to the host (Table 3).

Table 3 Decoder-to-host packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	block information word	8.7.9
01	address	8.7.2
02 to 57	vector or message (ID is word number in frame)	8.7.3, 8.7.8
58 to 7E	reserved	–
7F	status	8.4.9
80 to FE	reserved	–
FF	part ID	8.4.5

8.4 Configuration and synchronisation

8.4.1 GENERAL

After a reset, all configuration data has to be (re)loaded into the PCD5008 by the host using the SPI. PCD5008 features which do not change during operation are configured using the configuration packet (Section 8.4.4), the receiver control packets (Section 8.5) and the address configuration packets (Section 8.6). PCD5008 features which can be changed during operation are configured using the control packet. The checksum packet ensures proper communication between the host and the PCD5008.

8.4.2 SPI SECURITY ALGORITHM

The PCD5008 provides a security algorithm to verify correct SPI operation (Figs 9 and 10). The PCD5008 maintains a checksum register equal to the result of XORing the 24 data bits of every packet it receives, except the checksum packet 00H and special packets 1CH to 1FH. When the PCD5008 is reset, the internal checksum register is initialized to the 24 bit part ID defined in the part ID packet.

Immediately following a reset and whenever the host sends a packet other than a checksum packet, the SPI output of status and data (SPI transmit) is disabled. The PCD5008 then initiates SPI transfers continuously, sending the part ID packet (Section 8.4.5). Note that when SPI transmit is disabled all decoding and timing functions are unaffected. The SPI transmit can be enabled by sending a checksum packet for which the checksum value matches the checksum register.

Any checksum packets sent when the SPI transmit is enabled, are ignored by the PCD5008 irrespective of the value of the checksum packet data bits. Thus when the PCD5008 initiates an SPI transfer and the host has no data to send, the host should send the checksum packet so as not to disable the SPI transmit. The data in the checksum packet could be a null packet (32 bit stream of all zeros).

Sending a packet other than the checksum packet when the SPI transmit is enabled causes the SPI transmit to be disabled until a checksum packet is sent with the correct value. Thus when the host re-configures the PCD5008 after a reset, the SPI transmit is disabled until the host sends a checksum packet at the end of the configuration data, with the checksum value equal to the result of XORing together the data bits of each of the configuring packets and the data bits of the part ID packet.

If the SPI transmit is enabled and there is data in the transmit buffer, the PCD5008 initiates an SPI transfer sending a packet from its transmit buffer. The PCD5008 sends the status packet (which is not buffered) when the host initiates an SPI transfer and the transmit buffer is empty.

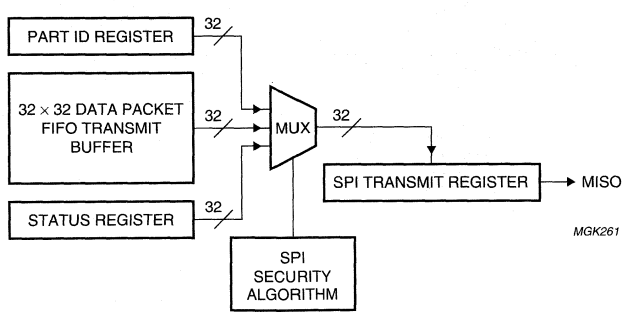


Fig.9 SPI transmit functional block diagram.

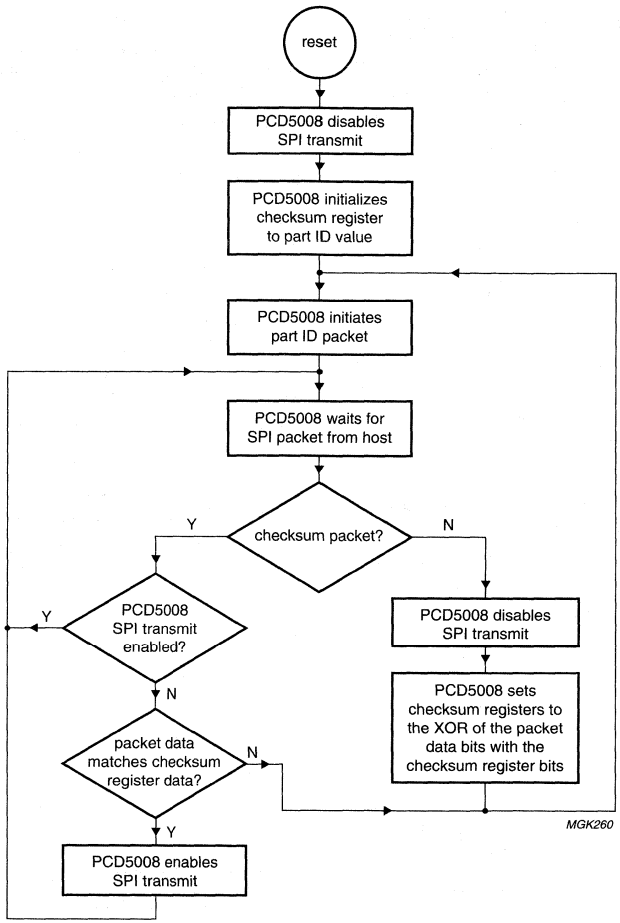


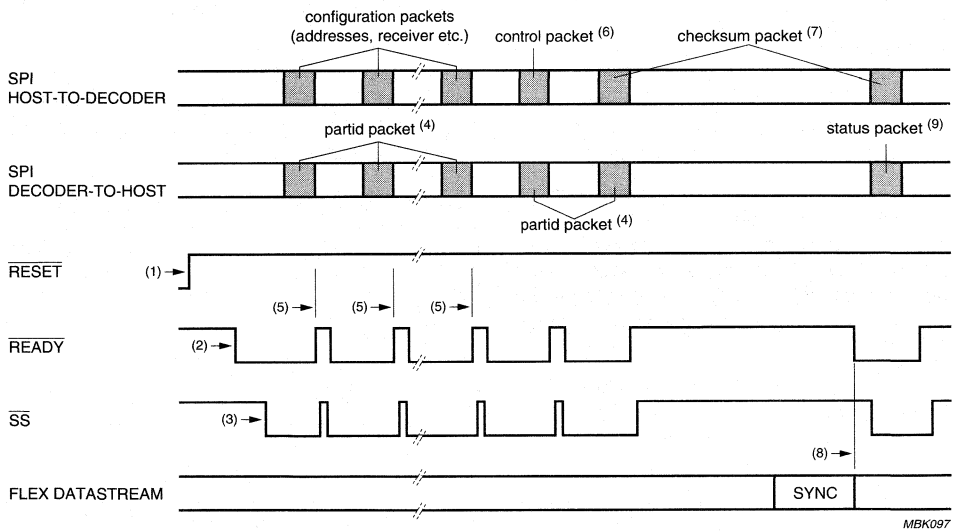
Fig.10 SPI security algorithm.

8.4.3 CONFIGURATION SEQUENCE

A typical configuration and synchronisation sequence would be as follows, see Fig.11 for event timings:

1. The PCD5008 is reset by the host.
2. After 1 second the PCD5008 interrupts the host to read the part ID by pulling the $\overline{\text{READY}}$ line LOW.
3. The host pulls $\overline{\text{SS}}$ LOW at the start of each SPI transfer and clocks out the part ID data.
4. The host configures the following aspects of PCD5008 operation:
   a) General configuration (Section 8.4.4)
   b) Receiver operation (Section 8.5)
   c) FLEX™ CAPCODE configuration (Section 8.6).

   The PCD5008 writes a part ID packet in response to each incoming packet.
5. At the end of each packet the PCD5008 pulls the $\overline{\text{READY}}$ line HIGH, and then LOW again to indicate that packet processing is complete.
6. The host writes a control packet to enable FLEX™ decoding in the PCD5008 (Section 8.4.7).
7. The host writes a checksum packet to enable SPI data output by the PCD5008 (Section 8.4.2).
8. On recognising a SYNC word, the PCD5008 synchronises to the channel.
9. The PCD5008 initiates an SPI transfer writing the status packet, indicating that it is now in synchronous mode.



Numbers within parenthesis refer to sequence numbers, see Section 8.4.3.

Fig.11 Typical configuration and synchronisation sequence.

8.4.4 CONFIGURATION PACKET (ID = 01H)

The configuration packet defines a number of different configuration options for the PCD5008. The PCD5008 ignores this packet when decoding is enabled, i.e. the ON bit in the control packet is set (Table 11).

OFD: oscillator frequency difference (Tables 4 and 5). These bits represent the maximum frequency difference between the 76.8 kHz oscillator (accounting for ageing, temperature variation, manufacturing tolerance etc.) and the worst case transmitter bit rate (specified in FLEX™ as ±25 parts per million (ppm), see Section 15.3.1). For example, if the transmitter tolerance is ±25 ppm and the 76.8 kHz oscillator tolerance is ±140 ppm, the transmitter-oscillator frequency difference is ±165 ppm and OFD should be cleared (300 ppm max.). Value after reset = 0. Note that configuring a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios.

SME: synchronous mode enable (Table 5). When this bit is set, a status packet is sent automatically whenever the synchronous mode update (SMU) bit in the status packet is set. This happens whenever a change occurs in the synchronous mode (SM) status bit, which indicates that the decoder is synchronized to a FLEX™ data stream. The host can use the SM bit in the status packet as an in-range/out-of-range indication. Value after reset = 0.

MOT: maximum off time (Table 5). When this bit is set, the PCD5008 assumes that there can be up to 1 minute between transmitted frames on the paging system. When this bit is clear, the PCD5008 assumes that there can be up to 4 minutes between transmitted frames on the paging system. This setting is determined by the service provider. Value after reset = 0.

COD: clock output disable (Table 5). When this bit is clear, a 38.4 kHz signal is output on the CLKOUT pin. When this bit is set, the CLKOUT pin is driven HIGH. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4 kHz period. Also note that when the clock output is enabled, the CLKOUT pin always outputs the 38.4 kHz signal even when the PCD5008 is in reset. Value after reset = 0.

MTE: minute timer enable (Table 5). When this bit is set, a status packet is sent at one minute intervals with the minute time-out (MT) bit in the status packet set. When this bit is clear, the internal 1-minute timer stops counting. See Section 8.4.8 for details of 1-minute timer operation. Value after reset = 0.

LBP: low battery polarity (Table 5). This bit defines the polarity of the PCD5008's LOBAT pin: When this bit is set, a HIGH at input LOBAT represents a low battery condition. The LB bit in the status packet is initialized to the inverse (i.e. inactive) value of the LBP bit when the PCD5008 is turned on (by setting the ON bit in the control packet). When the PCD5008 is turned on, the first low battery update in the status packet is sent to the host when a low battery condition is detected on the LOBAT pin. Value after reset = 0.

SP: signal polarity (Tables 5, 6 and 7). These bits set the polarity of EXTS1 and EXTS0 input signals. The polarity of the EXTS1 and EXTS0 bits is determined by the receiver design. Value after reset = 0.

Table 4 Maximum oscillator frequency difference

OFD_1	OFD_0	FREQUENCY DIFFERENCE (ppm)
0	0	±300
0	1	±150
1	0	±75
1	1	±0

Table 5 Configuration packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	OFD_1	OFD_0
1	0	0	0	0	0	0	SP_1	SP_0
0	SME	MOT	COD	MTE	LBP	0	0	0

Table 6 Input signal polarity

SP_1	SP_0	SIGNAL POLARITY	
		EXTS1	EXTS0
0	0	normal	normal
0	1	normal	inverted
1	0	inverted	normal
1	1	inverted	inverted

Table 7 FLEX™ 4 level FSK modulation selection

EXTS1	EXTS0	FSK MODULATION AT SP = 0,0 (Hz)
1	0	+4800
1	1	+1600
0	1	−1600
0	0	−4800

8.4.5 PART ID PACKET (ID = FFH)

The part ID packet is output by the PCD5008 SPI whenever the SPI transmit is disabled due to the checksum feature.

MDL: model (Table 8). The PCD5008 model value is 0.

CID: compatibility ID (Table 8). This value describes other parts with the same model number, which are compatible with this part. The PCD5008 compatibility value is 1. Devices which implement a superset of PCD5008 functionality have MDL cleared and CID_0 set.

REV: revision (Table 8). This identifies the manufacturing version of the PCD5008. For the PCD5008 the value is 6. Compatible parts have values in the range 0 to 5.

8.4.6 CHECKSUM PACKET (ID = 00H)

See Table 9 for checksum packet bit assignment.

CV: checksum value (24 bits), see Section 8.4.2.

Table 8 Part ID packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	1	1	1	1	1	1	1
2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

Table 9 Checksum packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

8.4.7 CONTROL PACKET (ID = 02H)

The control packet defines a number of different control bits for the PCD5008.

FF: force frame 0 to 7 (Table 11). When set, each of these bits forces the PCD5008 to decode one of the FLEX™ frames 0 to 7 irrespective of the system collapse value (for details of collapse values see Section 8.6.2). For example, if the system collapse causes the PCD5008 to decode frames 0, 32, 64 and 96, setting FF_2 causes the PCD5008 to also decode FLEX™ frame 2. This may be used to acquire transmitted time information. Value after reset = 0.

SPM: single phase mode (Table 11). When this bit is set, the PCD5008 decodes only one of the transmitted phases. When this bit is clear, the PCD5008 decodes all transmitted phases. This value is determined by the CAPCODE (Section 8.6). A change to this bit while the PCD5008 is on does not take effect until the next block 0 of a frame. Value after reset = 0.

PS: phase select (Tables 10 and 11). When the SPM bit is set, these bits define which phase the PCD5008 shall decode. This value is determined by the CAPCODE (Section 8.6). A change to these bits, while the PCD5008 is on, does not take effect until the next block 0 of a frame. Value after reset = 0.

Table 10 Phase selection (PS bits)

PS_1	PS_0	DECODED PHASE (BASED ON FLEX™ DATA RATE)		
		1600 bits/s	3200 bits/s	6400 bits/s
0	0	A	A	A
0	1	A	A	B
1	0	A	C	C
1	1	A	C	D

SBI: send block information words (BIW) 2 to 4 (Table 11). When this bit is set, BIWs with time and date information and BIWs received in error are sent to the host, (Section 8.7.9). Value after reset = 0.

MTC: minute timer clear (Table 11). Setting this bit causes the 1-minute timer to restart from 0 (Section 8.4.8).

ON: turn on decoder (Table 11). When this bit is set, the PCD5008 decodes FLEX™ signals. If this bit is cleared, signal processing stops. However, to assure proper operation, the PCD5008 requires that it be set into asynchronous mode when turned off. To achieve that the following sequence must be used:

1. Send control packet with ON bit clear (decoder off)
2. Send control packet with ON bit set (decoder on)
3. Send control packet with ON bit clear (decoder off).

Timing between these steps is specified below and is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet.

- The minimum time between steps 1 and 2 is the greater of 2 ms or the programmed shut-down time.
  The programmed shut-down time is the sum of all of the times programmed in the used receiver shut-down settings packets.
- There is no maximum time between steps 1 and 2
- The minimum time between steps 2 and 3 is 2 ms
- The maximum time between steps 2 and 3 is the programmed warm-up time minus 2 ms.
  The programmed warm-up time is the sum of all the times programmed in the used receiver warm-up settings packets.

8.4.8 OPERATING THE 1-MINUTE TIMER

The PCD5008 provides a 1-minute timer which allows the host to implement a time-of-day function while maintaining low-power operation. The 1-minute timer is enabled using the MTE bit in the configuration packet (Section 8.4.4). When the 1-minute timer is enabled, a status packet is sent at 1-minute intervals with the MT bit set (Section 8.4.9). When the MTE bit is clear, the internal 1-minute timer stops counting. When the host sends a control packet with MTC bit set, the 1-minute timer restarts from 0. This allows accurate setting of a time-of-day function.

Table 11 Control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	0
2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
1	0	SPM	PS_1	PS_0	0	0	0	0
0	0	SBI	0	MTC	0	0	0	ON

8.4.9 STATUS PACKET (ID = 7FH)

The status packet contains various types of information that the host may require and is sent to the host:

- Whenever the PCD5008 is polled and has no other data to send
- On events for which the PCD5008 is configured to send the status packet (Sections 8.4.4 and 8.4.7). In this case, the PCD5008 prompts the host to read a status packet for the following conditions:
  - SMU bit in the status packet and the SME bit in the configuration packet are set
  - MT bit in the status packet and the MTE bit in the configuration packet are set
  - EOF bit in the status packet is set
  - LBU bit in the status packet is set
  - BOE bit in the status packet is set.

FIV: frame information valid (Table 12). This bit is set, when a valid frame information word has been received since becoming synchronous to the system and the f and c fields contain valid values. If this bit is clear, no valid frame information words have been received since the PCD5008 became synchronous to the system. This value changes from 0 to 1 at the end of block 0 (Fig.17) of the frame in which the first frame information word was properly received. It is cleared when the PCD5008 goes into asynchronous mode (see SM bit below). This bit is initialized to 0 when the PCD5008 is reset and when the PCD5008 is turned off by clearing the ON bit in the control packet.

f: current frame number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

c: current system cycle number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: synchronous mode (Table 12). This bit is set, when the PCD5008 is synchronous to the system.
The PCD5008 sets this bit when the first synchronization words are received. It clears this bit when synchronisation to the FLEX™ signal is lost. This bit is initialized to 0 when the PCD5008 is reset and when it is turned off by clearing the ON bit in the control packet.

SMU: synchronous mode update (Table 12). This bit is set if the SM bit has been updated in this packet. After the PCD5008 has been turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search period (meaning the receiver is active during this time) expires (SM stays 0), after the PCD5008 is turned on. The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial search period expires. After the initial synchronous mode update, the SMU bit is set whenever the PCD5008 switches from/to synchronous mode. The bit is cleared when read. Changes in the SM bit due to turning off the PCD5008 does not set the SMU bit. This bit is initialized to 0 when the PCD5008 is reset.

LB: low battery (Table 12). Set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the receiver control packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the configuration packet, when the PCD5008 is turned on, by setting the ON bit in the control packet.

LBU: low battery update (Table 12). This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. The bit is cleared when read. The host controls when the LOBAT pin is read via the receiver control packets. Changes in the LB bit due to turning on the PCD5008 do not cause the LBU bit to be set. This bit is initialized to 0 when the PCD5008 is reset.

MT: minute time-out (Table 12). Set if one minute has elapsed. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

EOF: end of frame (Table 12). Set when the PCD5008 is in all frame mode (AFM) (Section 8.8.3), and the end of the frame has been reached. The PCD5008 is in the AFM if the AFM enable counter is non-zero, if any temporary address enabled (TAE) counter is non-zero (Section 8.8.3) or if the FAF bit in the AFM packet is set. The bit is cleared when read and initialized to 0 when the PCD5008 is reset.

BOE: buffer overflow error (Table 12). Set when information has been lost owing to slow host response time. When the PCD5008 detects that its SPI transmit buffer has overflowed, it clears the transmit buffer, turns off decoding by clearing the ON bit in the control packet, and sets this bit. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

x: unused bits (Table 12). The value of these bits is not guaranteed.

8.5 Receiver control interface

8.5.1 General

The PCD5008 has 8 programmable receiver control lines, S0 to S7. The host can program via SPI packets what setting is applied to the receiver control lines, the duration of warm-up and shut-down stages and the polling of the LOBAT pin. This programmability allows the PCD5008 to interface with many off-the-shelf receiver ICs. Note that these packets are ignored when sent while decoding is enabled (ON bit is set in the control packet).

8.5.2 Low battery detection

The PCD5008 can be configured to poll the LOBAT pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the PCD5008 activates the next setting on the receiver control lines. The PCD5008 sends a status packet whenever the value differs from the previous time that the LOBAT pin was polled.

8.5.3 Receiver settings at reset

The receiver control ports are 3-state outputs which are set to high impedance when the PCD5008 is reset, until the corresponding FRS bit in the receiver line control packet is set or the PCD5008 is turned on for the first time after a reset (by setting the ON bit in the control packet). This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the PCD5008.

8.5.4 Receiver off state (ID = 10H)

The receiver off state is configured by the receiver off setting packet (Table 13), which defines the settings to be applied when the PCD5008 decides to switch the receiver off.

LBC: low battery check (Table 13). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving the receiver off state. Value after reset = 0.

CLS: control line setting (Table 13). This is the value to be output on the receiver control lines for the receiver off state. Value after reset = 0.

ST: step time (Table 13). This sets the duration of the warm-up off time. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 159.375 ms (ST = FFH). Value after reset = 01H.

Table 12 Status packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	1	1	1
2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	SM	LB	x	x	c_3	c_2	c_1	c_0
0	SMU	LBU	x	MT	x	EOF	x	BOE

Table 13 Receiver off setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	0	0	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.5 RECEIVER WARM-UP SEQUENCES

8.5.5.1 Normal receiver warm-up sequence

The PCD5008 allows for up to 6 steps associated with warming up the receiver. When the PCD5008 turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS1 and EXTS0 input pins.

1. The PCD5008 leaves the receiver control lines in the off state for the programmed warm-up off time.
2. The first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting.
3. Subsequent warm-up settings are applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found.
4. At the end of the last used warm-up setting, the 1600 symbols per second (sps) sync setting or the 3200 sps sync setting is applied to the receiver control lines depending on the PCD5008 current state.

The PCD5008 must be configured such that the sum of all of the used warm-up times and the warm-up off time does not exceed 160 ms.

If it exceeds 160 ms, the PCD5008 executes the receiver shut-down sequence 160 ms after the start of the warm-up off time. If the sum of all of the used warm-up times and the warm-up off times is less than 160 ms, the receiver remains in the 1600 sps sync setting or the 3200 sps sync setting from the end of the last used warm-up setting until valid signals are expected (160 ms after the start of the warm-up off time). Figure 12 shows the receiver warm-up sequence while decoding, when all warm-up settings are enabled.

8.5.5.2 First receiver warm-up sequence

When the PCD5008 is turned on by setting the ON bit in the control packet, the receiver warm-up sequence differs from the sequence described in Section 8.5.5.1. After the ON bit is set no receiver warm-up off time is applied, instead the PCD5008 immediately begins to apply the receiver warm-up settings. When a disabled warm-up setting is found, the decoder applies 3200 sps sync setting to the receiver control lines. The decoder then expects valid signals after the 3200 sps sync warm-up time. Figure 13 shows the receiver warm-up sequence when the PCD5008 is first turned on and when all warm-up settings are enabled.

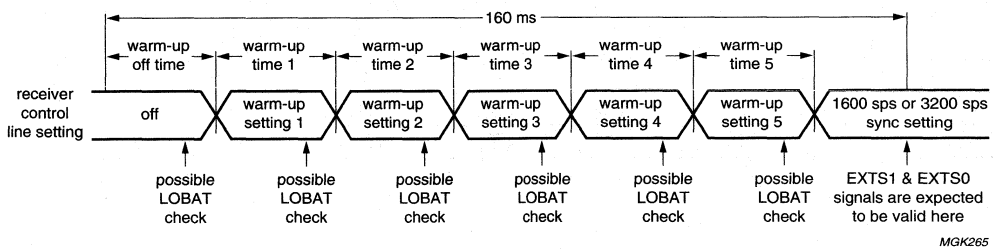


Fig.12 Receiver warm-up sequence while decoding.

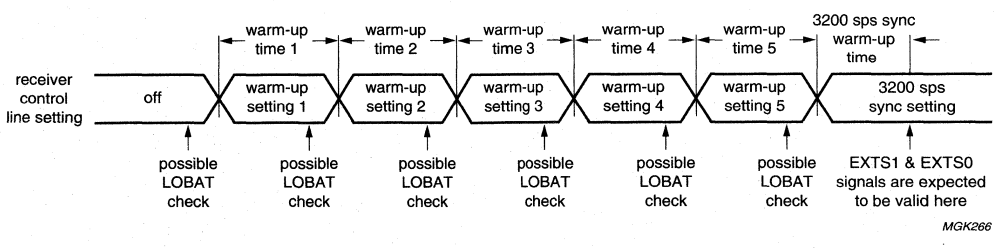


Fig.13 First receiver warm-up sequence after turning decoding on.

8.5.5.3 Receiver warm-up setting packets (ID = 11H to 15H)

CLS: control line setting (Table 15). This is the value to be output on the receiver control lines (S0 to S7) for this receiver warm-up state. Value after reset = 0.

SE: step enable (Table 15). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver warm-up sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 15). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver warm-up state. Value after reset = 0.

ST: step time (Table 15). This sets the duration time for receiver warm-up until the next receiver state. The setting is in 625 µs steps and valid values are:

625 µs (ST = 01H) to 79.375 ms (ST = 7FH).

Value after reset = 01H.

s: setting number, see Tables 14 and 15 for the s names and values and location in the receiver warm-up packet.

Table 14 Receiver warm-up setting numbers

s_3	s_2	s_1	s_0	SETTING NAME
0	0	0	1	warm-up 1
0	0	1	0	warm-up 2
0	0	1	1	warm-up 3
0	1	0	0	warm-up 4
0	1	0	1	warm-up 5

Table 15 Receiver warm-up setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.6 ACTIVE RECEIVER STATES

8.5.6.1 General

In addition to the warm-up and shut-down states, the PCD5008 has four active receiver states. When these settings are applied to the receiver control lines, the PCD5008 is decoding the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the FLEX™ data stream. Because of this, there is no time setting associated with these settings (with the exception of the 3200 sps sync setting).

The four settings are as follows:

1600 sps sync setting: applied when the PCD5008 searches for a 1600 sps signal.

3200 sps sync setting: applied when the PCD5008 searches for a 3200 sps signal.

1600 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync word in the sync 2 section of a 1600 sps frame.

3200 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync word in the sync 2 section of a 3200 sps frame.

Figure 14 shows some examples of how these settings are used in the PCD5008.

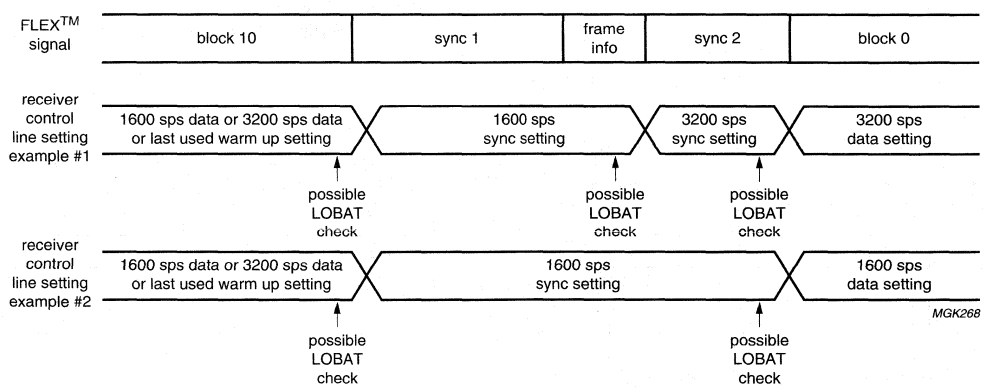


Fig.14 Examples of receiver control transitions.

8.5.6.2 Receiver on setting packets (ID = 16H to 19H)

LBC: low battery check (Table 17). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver sync setting state. Value after reset = 0.

CLS: control line setting (Table 17). This is the value to be output on the receiver control lines for this receiver sync setting state. Value after reset = 0.

ST: step time (Table 17). This sets the waiting time, before expecting good signals at EXTS1 and EXTS0 at the end of the warm-up sequence, after turning decoding on. The setting is in steps of 625 µs. Valid values are: 625 µs (ST = 01H) to 79.375 ms (ST = 7FH). Value after reset = 01H.

LBC: low battery check (Table 18). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver on state. Value after reset = 0.

CLS: control line setting (Table 18). This is the value to be output on the receiver control lines (S0 to S7) for this receiver on state. Value after reset = 0.

s: setting number, see Tables 16 and 18 for the s names and values and location in the receiver on setting packet.

Table 16 s names and values

s_3	s_2	s_1	s_0	SETTING NAME
0	1	1	1	1600 sps sync
1	0	0	0	3200 sps data
1	0	0	1	1600 sps data

8.5.7 FORCING RECEIVER LINES (ID = 0FH)

This packet (Table 19) enables host control over the receiver control line (S0 to S7) settings in all modes except reset. In reset, the receiver control lines are high impedance.

FRS: force receiver setting (Table 19). Setting a bit causes the associated CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line. Clearing a bit returns control of the corresponding receiver control line to the PCD5008. Value after reset = 0.

CLS: control line setting (Table 19). This bit setting is applied to the corresponding receiver control line if the associated FRS bit is set in this packet. Value after reset = 0.

Table 17 3200 sps sync setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	1	1	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

Table 18 Receiver on setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	0	0	0	0	0	0

Table 19 Receiver line control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	1	1	1	1
2	0	0	0	0	0	0	0	0
1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

8.5.8 Receiver shut-down sequence

The PCD5008 allows up to 3 steps associated with shutting down the receiver. When the PCD5008 decides to turn off the receiver, the first shut-down setting, if enabled, is applied to the receiver control lines for the corresponding shut-down time. At the end of the last used shut-down time, the receiver off setting is applied to the receiver control lines. If the first shut-down setting is not enabled, the PCD5008 switches directly from the receiver on to the receiver off setting.

Figure 15 shows the receiver shut-down sequence when all shut-down settings are enabled. If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the control packet), the PCD5008 immediately executes the receiver shut-down sequence. If the PCD5008 is executing the shut-down sequence when turned on (with the ON bit in the control packet set) the PCD5008 completes the shut-down sequence before starting the warm-up sequence.

8.5.8.1 Receiver shut-down setting packets (ID = 1A to 1BH)

SE: step enable (Table 21). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver shut-down sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 21). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver shut-down state. Value after reset = 0.

CLS: control line setting (Table 21). This is the value to be output on the receiver control lines (S0 to S7) for this receiver shut-down state. Value after reset = 0.

ST: step time (Table 21). This sets the duration time for receiver shut-down, until the next receiver state. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 39.375 ms (ST = 3FH). Value after reset = 01H.

s: setting number, see Tables 20 and 21 for the s names and values and location in the receiver shut-down packet.

Table 20 s names and values

s	SETTING NAME
0	shut-down 1
1	shut-down 2

Table 21 Receiver shut-down stages

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	1	0	1	s
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

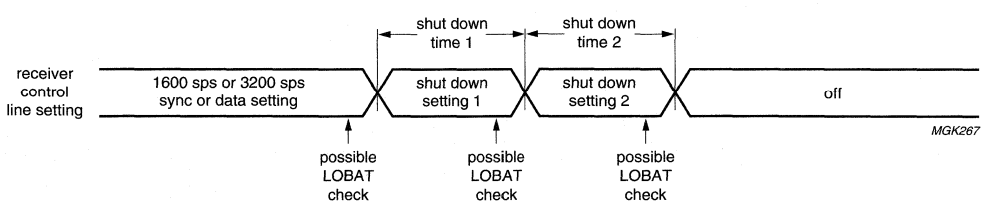


Fig.15 Receiver shut-down sequence.

8.6 Configuration of the FLEX™ CAPCODE

8.6.1 GENERAL

A CAPCODE specifies a decoder address, the collapse value of the address and whether single-phase, any-phase or all-phase address. The PCD5008 supports single-phase and any-phase operation. The FLEX™ protocol provides a standard mechanism to derive phase and frame in which an address should be transmitted. If this mechanism is not used, a CAPCODE also specifies the phase and frame assigned to the address.

8.6.2 CAPCODE FORMAT

The FLEX™ CAPCODE consist of a series of decimal and alphabetic fields, see Fig.16 for the field definitions.

When the FLEX™ standard pager collapse value of 4 (battery cycle of 16 frames) is used, the pager collapse field can be omitted.

The collapse value is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX™ channel. For a given collapse value b, the decoding device looks in every 2^b frames. Thus an address with an assigned base frame of 3 and a collapse value of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e. frames 3, 35, 67 and 99).

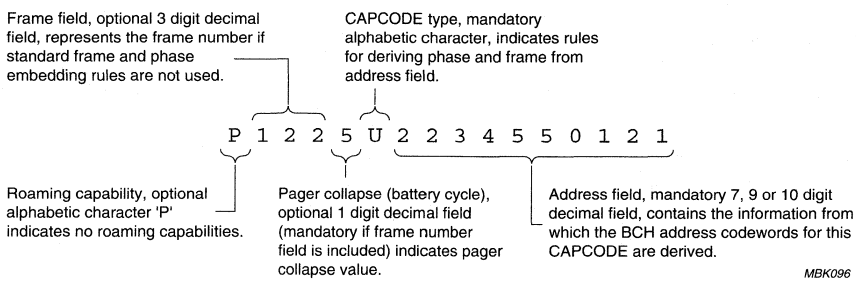


Fig.16 CAPCODE format.

8.6.3 CAPCODE RANGES

A CAPCODE represents user addresses ranging from 1 to 5370810366. A short CAPCODE can have address values below 2031615 and are represented in the data stream by a single address codeword. Some short addresses have been reserved for special purposes: information service addresses, network addresses, temporary (group) addresses and operator messaging addresses.

A long CAPCODE represents addresses situated above 2101248 subdivided into categories (uncoordinated, global, country) to allow different allocation schemes to coexist.

Table 22 defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table 22 CAPCODE assignment table

CAPCODE ADDRESS VALUE		DESCRIPTION
from	to	
0000000000		illegal
0000000001	0001933312	short addresses
0001933313	0001998848	illegal
0001998849	0002009087	reserved for future use
0002009088	0002025471	Information service addresses
0002025472	0002029567	network addresses
0002029568	0002029583	temporary addresses
0002029584	0002029599	operator messaging addresses
0002029600	0002031614	reserved for future use
0002031615	0002101248	invalid, not used
0002101249	0102101250	long address set 1-2 uncoordinated
0102101251	0402101250	long address set 1-2 country; note 1
0402101251	1075843072	long address set 1-2 global; note 2
1075843073	2149584896	long address set 1-3 global; note 2
2149584897	3223326720	long address set 1-4 global; note 2
3223326721	3923326750	long address set 2-3 country; note 1
3923326751	4280000000	long address set 2-3 reserved
4280000001	4285000000	long address set 2-3 information service, global; notes 2 and 3
4285000001	4290000000	long address set 2-3 information service, country; notes 1 and 3
4290000001	4291000000	long address set 2-3 information service, world-wide; notes 3 and 4
4291000001	4297068542	reserved for future use

Notes

1. Country: the addresses are coordinated within each country and with countries along borders.
2. Global: address is coordinated to be unique world-wide.
3. Information service: currently, the rules governing the use of these addresses are not defined.
4. World-wide: 1000 addresses are assigned to each country for world-wide use.

8.6.4 ADDRESS CALCULATION

Address codeword values generally do not coincide with (part of) the user address as specified in the CAPCODE. To find the address codewords corresponding to a user address a conversion has to be done (Table 24). The type of conversion depends on the CAPCODE range in which the user address is located. Note that addresses are transmitted LSB first (differently to POCSAG).

Short addresses, are transmitted in a single address codeword where as long addresses are transmitted in two consecutive address codewords. The first codeword of a long address contains the lower part of the address, the second codeword the upper part. By combining two long address codewords from different banks 6 long address ranges are created: 1 to 2, 1 to 3, 1 to 4, 2 to 3, 2 to 4 and 3 to 4. Ranges 2 to 4 and 3 to 4 are as yet undefined and reserved.

Table 24 describes how to calculate the 21 bit address codeword which is transmitted over the air.

Table 23 Address word range definitions

TYPE	HEX VALUE
Idle word (illegal address)	000000
Long address 1	000001 to 008000
Short address	008001 to 1E0000
Long address 3	1E0001 to 1E8000
Long address 4	1E8001 to 1F0000
Short address (reserved)	1F0001 to 1F27FF
Information service address	1F2800 to 1F67FF
Network address	1F6800 to 1F77FF
Temporary address	1F7800 to 1F780F
Operator messaging address	1F7810 to 1F781F
Short address (reserved)	1F7820 to 1F7FFE
Long address 2	1F7FFF to 1FFFFE
Idle word (illegal address)	1FFFFF

Table 24 Address word calculation

TYPE	LOWER ADDRESS CODEWORD; notes 1, 2 and 3	UPPER ADDRESS CODEWORD; notes 1, 3 and 4
Short address	CAPCODE + 8000	note 5
Long address, range 1 to 2; note 6	1 + ((CAPCODE – 1F9001) MOD 8000)	1FFFFF – ((CAPCODE – 1F9001) DIV 8000)
Long address, ranges 1 to 3 and 1 to 4	1 + ((CAPCODE – 1F9001) MOD 8000)	1D8000 + ((CAPCODE – 1F9001) DIV 8000)
Long address, range 2 to 3	1F7FFF + ((CAPCODE – 1F8FFF) MOD 8000)	1C8000 + ((CAPCODE – 1F8FFF) DIV 8000)

Notes

1. All numbers are in hexadecimal format.
2. The MOD operator gives the remainder of an integer division.
3. CAPCODE refers to the value of the address field in a FLEX™ CAPCODE.
4. The DIV operator is the integer division.
5. A short address consists of a single codeword.
6. The upper codeword range in bank 2 is used from the highest address downwards, i.e. the lowest value of the CAPCODE produces a codeword value of 1FFFFEH.

8.6.5 PHASE AND FRAME CALCULATION

The method for specifying the phase and base frame of a pager is specified in the CAPCODE type:

- The phase, base frame are extracted by standard rules from the user address field in the CAPCODE (CAPCODE types A to L).
- The phase is indicated by the CAPCODE type (Table 25) and the base frame is specified in the frame field of the CAPCODE (CAPCODE types U to Z).

For easy allocation of (up to 4) consecutive CAPCODEs having the same phase and frame, an offset in the range 0 to 3 is subtracted from the user address for the purposes of phase and frame extraction. The offset is determined by the CAPCODE type.

The standard rules for extracting phase and base frame from the user address are (phase numbers 0 to 3 correspond to phases A to D):

Phase number = ((Address – Offset) DIV 4) MOD 4

Frame = ((Address – Offset) DIV 16) MOD 128

where DIV is the integer division and MOD is the remainder of an integer division.

For a CAPCODE which does not use the standard rules for extracting phase and base frame (CAPCODE types U to Z) the 3-digit frame field 000 to 127 and a single digit decimal pager collapse 0 to 5 can precede the CAPCODE type. When these fields are not included, the paging device or the subscriber database must be accessed to determine the assigned frame and collapse value.

Table 25 Frame and phase extraction for different CAPCODE types

CAPCODE TYPE	PAGER TYPE	FRAME/PHASE EXTRACTION
A	single-phase	standard rules; Offset: 0
B	single-phase	standard rules; Offset: 1
C	single-phase	standard rules; Offset: 2
D	single-phase	standard rules; Offset: 3
E	any-phase	standard rules; Offset: 0
F	any-phase	standard rules; Offset: 1
G	any-phase	standard rules; Offset: 2
H	any-phase	standard rules; Offset: 3
I	all-phase; note 1	standard rules; Offset: 0
J	all-phase; note 1	standard rules; Offset: 1
K	all-phase; note 1	standard rules; Offset: 2
L	all-phase; note 1	standard rules; Offset: 3
U	single-phase	no frame extraction rules, phase-A
V	single-phase	no frame extraction rules, phase-B
W	single-phase	no frame extraction rules, phase-C
X	single-phase	no frame extraction rules, phase-D
Y	any-phase	no frame extraction rules, any-phase
Z	all-phase; note 1	no frame extraction rules, all-phase

Note

1. All-phase decoding is not defined in FLEX™ G1.8 and, therefore, is not supported by the PCD5008.

8.6.6 CONFIGURATION OF USER ADDRESSES (ID = 78H, 80H TO 8FH)

The PCD5008 has 16 user address locations which can be programmed as long or short, and configured as priority and/or tone-only. After a reset all address locations are disabled. Short addresses occupy a single location, long addresses occupy two locations. The first word of a long address must be in an even address location and the second word must be in the address index immediately following the first word. Address location containing long addresses of the 2-3 and 2-4 set (Section 8.6.3) must follow any address locations programmed as long addresses of the 1-2, 1-3 and 1-4 set.

User addresses are programmed using the address assignment packets, and are enabled and disabled using the address enable packet. To allow easy reprogramming of user addresses without disrupting normal operation, the host can send address assignment packets while the PCD5008 is on. In this case, the host must disable the user address location(s) by clearing the corresponding user address enable (UAE) bit in the UAE packet before changing any of the bits in the corresponding address assignment packet.

a: address location (Table 26). This specifies which address location is being configured. A zero in this field corresponds to address index zero (AI = 0) in the address packet received from the PCD5008 when an address is detected (Section 8.7.2).

LA: long address (Table 26). When this bit is set, the address is configured as a long address. Both words of a long address must have this bit set.

TOA: tone-only address (Table 26). When this bit is set, the PCD5008 considers this address a tone-only address and does not decode a vector word when the address is received. Both words of a long, tone only address must have this bit set.

A: address word (Table 26). This is the 21 bit value of the address word (A20 = MSB). Valid FLEX™ messaging addresses must be used. For the conversion from a CAPCODE (Section 8.6.4).

UAE: user address enable (Table 27). When a bit is set, the corresponding user address location is enabled. When it is cleared, the corresponding user address location is disabled. UAE_0 corresponds to the user address location configured using a packet ID of 80H and UAE_{15} corresponds to the user address location configured using a packet ID of 8FH. In some instances, if an invalid FLEX™ messaging address is programmed, it is not detected even when the address is enabled. Value after reset = 0.

Table 26 Address assignment packet bit assignments (ID = 80H to 8FH)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	0	0	0	a_3	a_2	a_1	a_0
2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Table 27 Address enable packet bit assignments (ID = 78H)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	0	0	0
2	0	0	0	0	0	0	0	0
1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_9	UAE_8
0	UAE_7	UAE_6	UAE_5	UAE_4	UAE_3	UAE_2	UAE_1	UAE_0

8.6.7 CONFIGURATION OF ASSIGNED FRAMES AND PAGER COLLAPSE (ID = 20H TO 27H)

The assigned frame and collapse value determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The PCD5008 must be configured explicitly to receive all required frames by setting the associated assigned frame (AF) bits. For each enabled CAPCODE these are the base frame and the associated frames implied by the pager collapse value. For example if the PCD5008 has one enabled address and it is assigned to base frame 3 with a collapse value of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99 and 115 should be set and the AF bits for all other frames should be cleared. There are 8 frame assignment packets each capable of assigning a range of 16 consecutive frame numbers.

f: frame range, see Table 29 for location in the frame assignment packet and Table 28 for the AFs and values. The value determines which 16 frames out of a range of 128 correspond to the 16 AF bits in the packet. At least one of these bits must have been set when the PCD5008 is turned on by setting the ON bit in the control packet. Value after reset = 0.

AF: assigned frame (Table 29). If a bit is set, the PCD5008 decodes the associated FLEX™ frame and scans its contents for enabled addresses. Value after reset = 0.

Table 28 Frame assignment ranges

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	frame 127	frame 112
0	0	1	frame 111	frame 96
0	1	0	frame 95	frame 80
0	1	1	frame 79	frame 64
1	0	0	frame 63	frame 48
1	0	1	frame 47	frame 32
1	1	0	frame 31	frame 16
1	1	1	frame 15	frame 0

8.6.8 CONFIGURATION OF ASSIGNED PHASE

The assigned phase is required only for single-phase devices. It determines the phase (A, B, C, or D) in which the messages are received. For details of phase calculation see Section 8.6.5. For details of programming the assigned phase see Section 8.4.7.

Table 29 Frame assignment packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

8.7 Call data packets

8.7.1 GENERAL

The PCD5008 sends data extracted from the FLEX™ signal to the host in SPI packets using the following packet types:

- BIW packets which contain data transmitted in BIWs
- Address packets which indicate that a call has been detected and give additional information about call attributes
- Vector packets which indicate the call type and indicate which message word numbers (WN) are associated with the call
- Message packets which contain the information contained within the message codewords of a call.

For more information about the function of these packets within the FLEX™ datastream see Section 8.8.

8.7.2 ADDRESS PACKET (ID = 01H)

Information from address codewords in received calls is sent to the host in address packets. If less than 3 bit errors are detected in a received address word and it matches an enabled address assigned to the PCD5008, the address packet is sent to the host processor. The address packet contains the call address, the location in the datastream of the associated vector, and other miscellaneous call data.

PA: priority address (Table 30). This bit is set if the address was received as a priority address.

p: phase (Table 30). This is the phase on which the address was detected (0 = A, 1 = B, 2 = C and 3 = D).

LA: long address (Table 30). This bit is set if the address was programmed in the PCD5008 as a LA.

AI: address index (Table 30). This index identifies which address was detected. Valid values are 00H to 0FH, corresponding to the 16 programmable address words and 80H to 8FH, corresponding to the 16 temporary addresses (Section 8.8.4). For long addresses, the address packet is only sent once with AI referring to the second word of the address.

TOA: tone-only address (Table 30). Set this bit if the address was programmed in the PCD5008 as a tone-only address. No vector word is sent for tone-only addresses.

WN: word number of vector (2 to 87 decimal) (Table 30). The location of the vector within this frame for the detected address. This value is invalid for this packet if the TOA bit is set.

x: unused bits (Table 30). The value of these bits is not guaranteed.

8.7.3 VECTOR PACKETS (ID = 02H TO 57H)

Information from vector codewords in received calls is sent to the host in vector packets. For any address packet sent to the host (except tone-only addresses), a corresponding vector packet is always sent.

The ID of the vector packet is the word number where the vector word was received in the frame. The host must associate vector packets with a call by searching for an address packet previously received on the same phase and with WN bits which match the ID of the vector packet.

The vector type of a vector packet indicates the format of a call as one of:

- Numeric (3 types)
- Short message/tone-only
- Hex/binary
- Alphanumeric
- Secure message
- Short instruction.

The numeric, hex/binary, alphanumeric, and secure message vector packets indicate the location and number of message word packets in the message field. If more than two bit errors are detected in the vector word (via BCH calculations, parity calculations, check character calculations, or value validation) the e bit is set and the message words are not sent.

Table 30 Address packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	PA	p_1	p_0	LA	x	x	x	x
1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

8.7.4 NUMERIC VECTOR PACKET

WN: word number of vector (2 to 87 decimal) (Table 31). WN describes the location of the vector word in the frame.

e: error (Table 31). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 31). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

K: first check bits of the message checksum (Table 31 and Section 8.8.6).

n: number of message words in the message (Table 31), including the second vector word for long addresses, (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.

b: word number of message start in the message field (3 to 87 decimal) (Table 31). For long addresses, the word number indicates the location of the second message word.

x: unused bits (Table 31). The value of these bits is not guaranteed.

V: vector type identifier (Table 32).

Table 31 Numeric vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Table 32 Numeric vector definitions

V_2	V_1	V_0	TYPE	DESCRIPTION
0	1	1	standard numeric	No special formatting of characters is specified.
1	0	0	special format numeric	Formatting of the received characters is predetermined by special rules in the host (e.g. inserting spaces and dashes).
1	1	1	numbered numeric	Received information is numbered by the service provider to indicate all messages have been properly received.

8.7.5 SHORT MESSAGE/TONE-ONLY VECTOR PACKET

V: vector type identifier, these bits set to 010 for a short message/tone-only vector (Table 33).

WN: word number of vector (2 to 87 decimal) (Table 33). WN describes the location of the vector word in the frame.

e: error (Table 33). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 33). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

t: message type (Tables 33 and 34). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 33). The value of these bits is not guaranteed.

d: data bits whose definition depends on the value of t in this packet according to Table 34. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet from the word location immediately following the vector packet. Except for the short message on a non-network address (t = 0), all messages bits in the message packet are unused and should be ignored.

Table 33 Short message/tone-only vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

Table 34 Short message/tone-only vector definitions

t_1	t_0	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	c_3	c_2	c_1	c_0	b_3	b_2	b_1	b_0	a_3	a_2	a_1	a_0	first 3 numeric characters; note 1
0	1	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	S_2	S_1	S_0	8 sources (S) and 9 unused bits (s)
1	0	s_1	s_0	R_0	N_5	N_4	N_3	N_2	N_1	N_0	S_2	S_1	S_0	8 sources (S), message retrieval flag (R), message number (N) and 2 unused bits (s)
1	1													spare message type

Note

1. For long addresses, an extra 5 characters are sent in the message packet immediately following the vector packet.

8.7.6 HEX/BINARY, ALPHANUMERIC AND SECURE MESSAGE VECTORS

V: vector type identifier (Table 35).

WN: word number of vector (2 to 87 decimal) (Table 36). WN describes the location of the vector word in the frame.

e: error (Table 36). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 36). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

n: number of message words in this frame (Table 36), including the first message word that immediately follows a long address vector. Valid values are 1 to 85 decimal.

b: word number of message start in the message field (Table 36). Valid values are 3 to 87 decimal.

x: unused bits (Table 36). The value of these bits is not guaranteed.

Note that for long addresses, the first message packet is sent from the word location immediately following the word location of the vector packet. The b bits indicate the second message word in the message field if one exists.

Table 35 Non-numeric vector definitions

V_2	V_1	V_0	TYPE
0	0	0	secure
1	0	1	alphanumeric
1	1	0	hex/binary

Table 36 Hex/binary, alphanumeric and secure message vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

8.7.7 SHORT INSTRUCTION VECTOR

V: these bits are set 001 for a short instruction vector.

WN: word number of vector (2 to 87 decimal) (Table 37). WN describes the location of the vector word in the frame.

e: error (Table 37). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 37). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: instruction type (Tables 37 and 38). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 37). The value of these bits is not guaranteed.

d: data bits whose definition depend on the value of the i bits in this packet according to Table 38. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet immediately following the vector packet. All message bits in the message packet are unused and should be ignored.

Table 37 Short instruction vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

Table 38 Short instruction vector definitions

i_2	i_1	i_0	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	0	a_3	a_2	a_1	a_0	f_6	f_5	f_4	f_3	f_2	f_1	f_0	temporary address assignment, note 1
0	0	1												reserved
0	1	0												reserved
0	1	1												reserved
1	0	0												reserved
1	0	1												reserved
1	1	0												reserved
1	1	1												reserved for test

Note

1. Assigned temporary address index a and associated frame number f (Section 8.8.4).

8.7.8 MESSAGE PACKETS (ID = 03H TO 57H)

8.7.8.1 General

The message field follows the vector field in the FLEX™ protocol. It contains the message data, checksum information, and may contain fragment and message numbers (Sections 8.8.7 and 8.8.5). If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in message packets to the host.

The ID of the message packet is the word number where the message word was received in the frame.

WN: word number of message word (3 to 87 decimal) (Table 40). WN describes the location of the message word in the frame.

e: error (Table 40). Set if more than 2 bit errors are detected in the word.

p: phase (Table 40). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: these are the information bits of the message word (Table 40). The definition of these i bits depends on the vector type and which word of the message is being received.

8.7.8.2 Numeric Message

FLEX™ numeric messages are encoded using the 4-bit BCD encoded characters sets described in Table 39. Characters are placed in codewords along with additional information about the message as described in Tables 41 and 42 and the following definitions. The 4-bit numeric characters of the message are designated as letters a, b, c, d, ... z, A, B etc.

Only codewords containing the numeric message are to be transmitted. The space character CH is used to fill any unused 4-bit characters in the last word and zeros to fill any remaining partial characters. The checksum includes only the codewords comprising the shortened message, along with the space and fill characters used to fill in the last word.

Table 39 Standard and alternate numeric character sets; Peoples Republic of China (ROC) option 'on' and 'off'

B_3	B_2	B_1	B_0	CHARACTER	
				ROC 'on'	ROC 'off'
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	Spare
1	0	1	1	B	U
1	1	0	0	Space	Space
1	1	0	1	C	–
1	1	1	0	D	]
1	1	1	1	E	[

Table 40 Message packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

K: least significant 2 bits of 6 bit message checksum (Tables 41 and 42), most significant 4 bits are in the vector word. See Section 8.8.6 for a description of message checksums.

N: message number (Table 42). See Section 8.8.7 for a description of message numbering.

R: message retrieval flag (Table 42). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: special format, (Table 42). In the numbered message format, when this bit is set, a special display format should be used. Spaces and dashes, specified by the host, are inserted into the received message to ease reading of the message. This feature may avoid the transmission of an additional word on the channel. The actual format is undefined in FLEX™ and may be determined by the manufacturer.

Table 41 Standard (V = 011) or special format (V = 100) 4, 10, 15, 20, 25, 31, 36, or 41 characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 42 Numbered (V = 111) 2, 8, 13, 18, 23, 29, 34, or 39 numeric characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

8.7.8.3 Alphanumeric Message

FLEX™ alphanumeric messages are encoded using the 7-bit encoded alphanumeric character set defined in Table 43. Characters are placed in codewords along with additional information about the message as described in Tables 44 and 45 and the following definitions. The 7-bit characters of the message are designated lower case letters a, b, c, d, etc.

Alphanumeric messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation.

Control characters that are not acted upon by the pager are ignored in the display process (do not require display space) but are stored in memory for possible download to an external device. The ASCII character ETX (03H) should be used to fill any unused 7-bit characters in a word.

Where symbolic characters (e.g. Chinese, Kanji etc.) are being transmitted, special rules for fragment and message termination are defined in Section 8.8.5.1.

Each 7-bit field, starting with the second character of the second word in the message (first character of the second word in all remaining fragments), represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

Table 43 FLEX™ alphanumeric character set

LEAST SIGNIFICANT 4 BITS OF CHARACTER (HEX)	MOST SIGNIFICANT 3 BITS OF CHARACTER (HEX)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	“	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	’	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	TAB	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

K: 10-bit fragment checksum (Tables 44 and 45). See Section 8.8.6 for a description of message checksum.

C: 1-bit message continued flag (Tables 44 and 45). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2-bit message fragment number (Tables 44 and 45). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 44 and 45). See Section 8.8.7 for a description of message numbering.

M: 1-bit mail drop flag (Table 44). When this bit is set, it indicates the message is to be stored in a special area in memory and is written over existing data automatically in that memory space.

R: message retrieval flag (Table 44). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: 7-bit signature field (Table 44). The signature is defined to be the 1's complement of the binary sum over the total message (all fragments). 7 bits at a time are taken (on alpha character boundary) starting with the first 7 bits directly following the signature field, $a_6a_5a_4a_3a_2a_1a_0$, $b_6b_5b_4b_3b_2b_1b_0$, etc. The 7 LSBs of the result are transmitted as the message signature.

U, V: fragmentation control bits (Table 45). This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (character made up of 1, 2 or 3 ASCII characters) are transmitted using the alphanumeric message type. The default value is 0,0. See Section 8.8.5.1 for a description of fragment control.

Table 44 Vector type V = 101 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 45 Vector type V = 101 other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.8.4 Hex/binary message

FLEX™ hexadecimal/binary messages may be encoded using any word size (blocking length) in the range 1 to 16 bits. Words are placed in codewords along with additional information about the message as described in Tables 46 and 47 and these definitions. The message data in Tables 46 and 47 have blocking lengths of 4 bits; words are designated lower case letters a, b, c, d etc.

Hexadecimal/binary messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation. Messages and message fragments are terminated, or interrupted in the case of a non-terminating fragment, on the last full character boundary in the last codeword. Unused bits are cleared if the last valid data bit is logic 1, or set if the last valid data bit is logic 0. If the terminating fragment exactly fills its last codeword, an additional codeword is sent to indicate the location of the last character. This codeword is filled with logic 0s if the last valid data bit is logic 1 and filled with logic 1s if the last valid data bit is logic 0.

Fields K to N make up the first word of a message and the first word of every fragment in a long message.

K: 12 bit fragment checksum (Tables 46 and 47). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Tables 46 and 47). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Tables 46 and 47). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 46 and 47). See Section 8.8.7 for a description of message numbering.

H: 1 bit header message flag (Table 46). It is a header message only when this bit is set, otherwise it is a data message. A header message is a displayable tag associated with a non-displayable data message. The header message (which is sent first) and the data message, both have the same message number.

The second codeword of the first fragment of a hex/binary message contains fields R to S. These fields are only transmitted in the first fragment of a message.

R: message retrieval flag (Table 46). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

s: 5 bit field reserved for future use (Table 46). Default value = 00000.

M: 1 bit mail drop flag, see Table 46. When this bit is set, the message is to be stored in a special area in memory to overwrite existing data in the same memory space.

D: 1 bit display direction field (Table 46). D = 0 display left to right, D = 1 display right to left (valid only when data sent as characters i.e. blocking length not equal 0001).

B: 4 bit blocking length (Table 46). Indicates bits per character. $B_3B_2B_1B_0$ = 0001 = 1 bit per character (binary/transparent data), 1111 = 15 bits per character, 0000 = 16 bits per character. Data with a blocking length other than 1 is assumed to be displayed on a character by character basis (default value = 0001). Note: Tables 46 and 47 show B = 4 bit blocking length.

S: 8 bit signature field (Table 46). The 1's complement of the binary sum, taken 8 bits at a time, over the total message prior to formatting into fragments. The first 8 bits following the signature field are summed with the following 8 bits, $b_3b_2b_1b_0a_3a_2a_1a_0 + d_3d_2d_1d_0c_3c_2c_1c_0$, etc. continuing to the last valid data bit in the last word of the last fragment (the sum does not include termination bits). The 8 LSBs of the result are inverted (1's complement) and transmitted as the message signature.

8.7.8.5 Secure message

FLEX™ secure messages are encoded using the 7-bit FLEX™ alphanumeric character set (Section 8.7.8.3). These characters are placed in codewords along with additional information about the message as described in Table 48 and the following definitions. In Table 48, 7-bit characters of the message are designated lower case letters a, b, c, d etc.

Secure messages follow the same fragmentation and termination rules as alphanumeric messages (Section 8.7.8.3).

K: 10 bit fragment checksum (Table 48). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Table 48). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Table 48). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Table 48). See Section 8.8.7 for a description of message numbering.

s: spare bits (Table 48), are not used and are set to 0.

Table 46 Vector type V = 110 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 47 Vector type V = 110 all other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 48 Vector type V = 000 all fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.9 BLOCK INFORMATION WORD (BIW) PACKET (ID = 00H)

The FLEX™ protocol allows systems to transmit time information using block information words. The information carried in a BIW depends on the BIW word format (Table 49). The first BIW of each phase, carrying information about the frame structure, is used internally by the PCD5008 and is never transmitted to the host.

The PCD5008 can be configured to send all time and date BIWs (BIW001, BIW010 and BIW101) to the host by setting the SBI bit in the control packet, see Section 8.4.7. When the SBI bit is set and a BIW is received with an uncorrectable number of bit errors, the PCD5008 sends the BIW to the host indicating that the codeword was received in error (regardless of the BIW word format). The PCD5008 does not support decoding of vector and message words associated with the data/system message BIW101.

System providers supporting local time transmissions are required to transmit at least one time related BIW in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of sync 1 of frame 0 of the current cycle.
See Tables 50, 51, 52 and 53 and the following bit definitions of the time related BIWs.

e: error (Table 49). Set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

p: phase (Table 49), is the phase on which the BIW was found (0 = A, 1 = B, 2 = C and 3 = D).

x: unused bits (Table 49). Their value is not guaranteed.

f: word format type (Table 49). The value of these bits modify the meaning of the s bits in this packet as described in Tables 50, 51 and 52. If the e bit is not set, this field is one of 001, 010 or 101.

s: BIW information bits (Table 49). The definition of these bits depend on the f bits in this packet.

m: month field (Table 50). 0001 to 1100 binary correspond to January to December in month order.

d: day field (Table 50). 00001 to 11111 binary correspond to 1 to 31 days in the month.

Table 49 BIW packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	e	p_1	p_0	x	x	f_2	f_1	f_0
1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Table 50 Month/day/year BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	0	1	m_3	m_2	m_1	m_0	d_4	d_3	d_2	d_1	d_0	Y_4	Y_3	Y_2	Y_1	Y_0

Table 51 Second/minute/hour BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	1	1	S_2	S_1	S_0	M_5	M_4	M_3	M_2	M_1	M_0	H_4	H_3	H_2	H_1	H_0

Table 52 Accurate seconds/daylight savings time/time zone; system message BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	DESCRIPTION
1	0	1	S_2	S_1	S_0	x	L_0	z_4	z_3	z_2	z_1	z_0	0	1	0	X	system message; note 1

Note

1. When the $s_3s_2s_1s_0$ field is 0100 or 0101, then s_4 to s_{13} are defined as above, when the $s_3s_2s_1s_0$ field does not have one of these values, the system message does not contain time related information and is not sent to the host.

Y: year field (Table 50). This represents the year with modulo 32 arithmetic. 00000 to 11111 binary representing years 1994 to 2025 and 2026 to 2057.

S: seconds field (Table 51). This represents a coarse value of the seconds field. These bits represent the seconds in $\frac{1}{8}$ minute (7.5 s) increments. 000 to 111 binary correspond to 0 to 52.5 seconds.

M: minute field (Table 51). 000000 to 111011 binary correspond to 0 to 59 minutes.

H: hour field (Table 51). 00000 to 10111 binary correspond to 0 to 23 hours.

S: accurate seconds (Table 52). This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents the time that should be added to the coarse seconds in $\frac{1}{64}$ minute increments.

L: daylight savings time (Table 52). When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is daylight savings time.

z: time zone (Table 52). These bits indicate the time zone for the time which is being transmitted. The offset from GMT is the offset for local standard time. Table 53 describes the values for **z**.

Table 53 Time zone values

z_4	z_3	z_2	z_1	z_0	TIME ZONE
0	0	0	0	0	GMT
0	0	0	0	1	GMT + 01:00h
0	0	0	1	0	GMT + 02:00h
0	0	0	1	1	GMT + 03:00h
0	0	1	0	0	GMT + 04:00h
0	0	1	0	1	GMT + 05:00h
0	0	1	1	0	GMT + 06:00h
0	0	1	1	1	GMT + 07:00h
0	1	0	0	0	GMT + 08:00h
0	1	0	0	1	GMT + 09:00h
0	1	0	1	0	GMT + 10:00h
0	1	0	1	1	GMT + 11:00h
0	1	1	0	0	GMT + 12:00h
0	1	1	0	1	GMT + 03:30h
0	1	1	1	0	GMT + 04:30h
0	1	1	1	1	GMT + 05:30h

z_4	z_3	z_2	z_1	z_0	TIME ZONE
1	0	0	0	0	reserved
1	0	0	0	1	GMT + 05:45h
1	0	0	1	0	GMT + 06:30h
1	0	0	1	1	GMT + 09:30h
1	0	1	0	0	GMT – 03:30h
1	0	1	0	1	GMT – 11:00h
1	0	1	1	0	GMT – 10:00h
1	0	1	1	1	GMT – 09:00h
1	1	0	0	0	GMT – 08:00h
1	1	0	0	1	GMT – 07:00h
1	1	0	1	0	GMT – 06:00h
1	1	0	1	1	GMT – 05:00h
1	1	1	0	0	GMT – 04:00h
1	1	1	0	1	GMT – 03:00h
1	1	1	1	0	GMT – 02:00h
1	1	1	1	1	GMT – 01:00h

8.8 Message reception

8.8.1 FLEX™ SIGNAL STRUCTURE

The FLEX™ signal transmitted on the radio channel (see Fig.17) consists of a series of four minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames which are not assigned. The FLEX™ signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing or carry-on information within the FLEX™ signal.

Each FLEX™ frame has a synchronization portion followed by an eleven block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200 or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2 level FSK modulation and consists of a single phase of information at 1600 bps, phase-A. The 3200 bps rate is transmitted at either 1600 sps using 4 level FSK modulation or 3200 sps using 2 level FSK modulation and consists of two concurrent phases of information at 1600 bps, phase-A and phase-C. The 6400 bps rate is transmitted at 3200 sps using 4 level FSK modulation and consists of four concurrent phases of information at 1600 bps (phase-A, -B, -C and -D).

Each block has eight interleaved words per phase, thus there are 88 codewords (numbered 0 to 87) per phase in every frame. Each word has information contained within an error correcting code which allows for bit error correction and detection. The 88 words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field.
The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of: a first sync signal at 1600 bps; a frame information word having the frame number 0 to 127 (7 bits) and the cycle number 0 to 14 (4 bits); and a second sync signal at the data rate of the interleaved portion.

The block information field contains BIWs. These can be used for determining time and date information and certain paging system information.

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. Information in the FLEX™ signal may indicate that an address is a priority address. An address may be either a short (one word) address or a long (two word) address. An address may be a tone-only address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX™ signal indicates the location of the vector word in the vector field associated with the address. A pager may perform battery saving at the end of the address field when its address(es) is not detected.

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information. Short addresses have one associated vector word in the vector field. Long addresses have one associated vector word in the vector field directly followed by the first message codeword of the call.

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD or binary depending upon the message type.

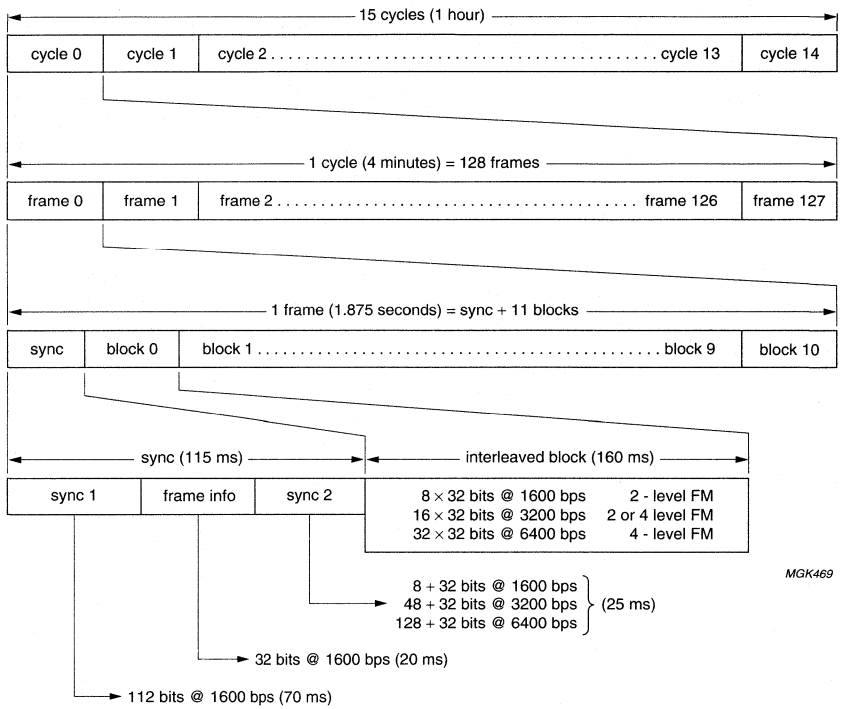


Fig.17 FLEX™ signal structure.

8.8.2 MESSAGE BUILDING

The PCD5008 sends data from the FLEX™ signal to the host in packets. Data is transmitted one block at a time, and one phase at a time. For a 2 phase transmission, information in block 0 phase-A is converted into packets and sent to the host, then information in block 0 phase-C is sent to the host followed by information in block 1 phase-A and then information in block 1 phase-C etc. Codewords for different calls may therefore be interleaved, so the host must use the phase and word number embedded in each packet to associate that packet with a particular call.

The phase and word number of the vector packet provides a unique key which allows the host to associate all the data for a particular call within a frame. The host must then use information embedded in the vector word to calculate what message word locations are associated with the vector.

Table 54 FLEX™ transmission sequence

BLOCK	WORD	PHASE-A	PHASE-C
0	0	BIW1; note 1	BIW1; note 1
	1	addr; note 2	BIW
	2	addr; note 2	BIW
	3	$addr_1$	addr; note 2
	4	$addr_2$	addr; note 2
	5	vect; note 2	long $addr_3$ (cw 1)
	6	vect; note 2	long $addr_3$ (cw 2)
	7	$vect_1$	addr; note 2
1	8	$vect_2$	vect; note 2
	9	$mess_1$ (cw 1)	vect; note 2
	10	$mess_1$ (cw 2)	$vect_3$; note 3
	11	$mess_1$ (cw 3)	$mess_3$ (cw 1); note 4
	12	$mess_2$ (cw 1)	mess; note 2
	13	$mess_2$ (cw 2)	mess; note 2
	14	$mess_2$ (cw 3)	$mess_3$ (cw 2)
	15	$mess_2$ (cw 4)	$mess_3$ (cw 3)

Notes

1. Phases begin with BIW1, which is not sent to the host.
2. Codewords not addressed to the pager.
3. Vector for long address indicates the location of the second and third message words.
4. For long addresses, the first message word immediately follows the vector.

Tables 54 and 55 show an example of receiving three messages (possibly portions of fragmented or group messages), and two BIW packets in the first two blocks of a 2 phase 3200 bps FLEX™ frame in case of an any-phase pager. Table 54 shows the block number, word number and word content of both phase-A and phase-C (subscripts indicate the call number). In a 6400 bps FLEX™ frame, there would be four phases: A, B, C and D; in a 1600 bps signal there would be only phase-A. Table 55 shows the sequence of packets transmitted to the host.

Table 55 PCD5008 packet sequence

PACKET	PHASE	PACKET TYPE	WORD NO.	COMMENT
1	A	address	7	note 1
2	A	address	8	note 1
3	A	vector	7	pointer to phase-A word 9
4	C	BIW	n.a.	note 2
5	C	BIW	n.a.	note 2
6	C	long address	10	note 1
7	A	vector	8	pointer to phase-A word 12
8	A	message	9	$mess_1$ (cw 1)
9	A	message	10	$mess_1$ (cw 2)
10	A	message	11	$mess_1$ (cw 3)
11	A	message	12	$mess_2$ (cw 1)
12	A	message	13	$mess_2$ (cw 2)
13	A	message	14	$mess_2$ (cw 3)
14	A	message	15	$mess_2$ (cw 4)
15	C	vector	10	pointer to phase-A word 14
16	C	message	11	$mess_3$ (cw 1)
17	C	message	14	$mess_3$ (cw 2)
18	C	message	15	$mess_3$ (cw 3)

Notes

1. Word number in an address is that of the corresponding vector.
2. BIW sent if BIW reception enabled by SBI bit in the control packet.

8.8.3 ALL FRAME MODE (ID = 03H)

The FLEX™ protocol requires pagers to be capable of receiving data in frames other than pagers' programmed frames and frames implied by collapse values. This is achieved in the PCD5008 by all frame mode (AFM) which is required to implement the following features:

- Fragmented messages Section 8.8.5)
- Temporary addresses (Section 8.8.4).

The PCD5008 enters AFM automatically and when in AFM, it decodes every FLEX™ frame irrespective of whether it is a programmed frame. In AFM the PCD5008 sends a status packet with the end-of-frame (EOF) bit set at the end of every frame. In addition the host can force AFM by sending an AFM packet with the force all frame mode (FAF) bit set.

The PCD5008 contains a number of counters which are used to track the number of active calls requiring AFM. These consist of an AFM counter for tracking the number of active fragmented messages and 16 temporary address enable (TAE) counters which count the number of times each temporary address has been enabled. These counters are automatically incremented when a corresponding vector is received, i.e.:

- A short instruction vector indicating a temporary address has been assigned to this pager
- A vector indicating a message for this pager with a format which allows fragmentation.

The host must determine when no further data can be received for a message associated with a temporary address, or a fragmented message, and send an AFM packet, see Table 56, to decrement the appropriate counter. AFM remains active until the host determines that no further data can be sent to it outside programmed frames, i.e:

- The TAE counters are all zero indicating that no further temporary message data is expected
- The AFM counter is zero indicating that no further data is expected for fragmented messages
- The FAF bit is clear.

Both the AFM counter and the TAE counters can only be incremented internally by the PCD5008 and can only be decremented by the host via AFM packet. Neither the TAE counters nor the AFM counter can be incremented past the value 127 (it does not roll-over) or decremented past the value 0. The TAE counters and the AFM counter are cleared on a reset and when the decoder is turned off.

DAF: decrement all frame mode counter, see Table 56. Setting this bit decrements the AFM counter by one. If a packet is sent with this bit clear, the AFM counter is not affected. Value after reset = 0.

FAF: force all frame mode, see Table 56. Setting this bit forces the PCD5008 to enter AFM. If this bit is clear, the PCD5008 may or may not be in AFM depending on the status of the AFM counter and the TAE counters. This functionality may be useful in acquiring transmitted time information. Value after reset = 0.

DTA: decrement temporary address enable counter, see Table 56. When a bit in this word is set, the corresponding TAE counter is decremented by one. When a bit is clear, the corresponding TAE counter is not affected. When a TAE counter reaches zero, the temporary address is disabled. Value after reset = 0.

Table 56 All frame mode packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	1
2	DAF	FAF	0	0	0	0	0	0
1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_9	DTA_8
0	DTA_7	DTA_6	DTA_5	DTA_4	DTA_3	DTA_2	DTA_1	DTA_0

8.8.4 TEMPORARY ADDRESSES

FLEX™ allows dynamic group calls in which a common message is sent to a group of paging devices. This is achieved by assigning the same temporary address (TA) to each pager in the group using the pagers' personal addresses and the short instruction vector. The short instruction vector causes the TA to be active in the next occurrence of a specific frame (if the designated frame is equal to the present frame the host is to interpret this as the next occurrence of this frame in the following cycle).

FLEX™ specifies sixteen TAs which remain valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. The FLEX™ protocol restricts the placement of TAs such that once assigned to a specific frame they cannot occur in the FLEX™ transmission before that frame.

The PCD5008 uses AFM (Section 8.8.3) to allow the reception of TAs outside programmed frames.
The sequence for the host and the PCD5008 to operate a TA is:

1. The PCD5008 receives an address codeword followed by a vector codeword with $V_2V_1V_0 = 001$ and $I_2I_1I_0 = 000$ indicating a short instruction vector which assigns a TA to this pager.
2. The PCD5008 passes the address and vector codeword to the host as packets and increments the corresponding TA counter and enters AFM.
3. The host examines the vector packet to identify which TA is assigned and the frame in which the TA is expected.
4. The PCD5008 continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
5. The host processes data packets received while the PCD5008 is in AFM. It uses the AFM packet to decrement the appropriate TA counter when no further data can be expected for the corresponding TA. This occurs when:
   a) The TA is not found in the assigned frame.
   b) The TA is found in the frame it was assigned and was not a fragmented message.
   c) The TA is found in the assigned frame was a fragmented message and the rules for message fragmentation (Section 8.8.5) indicate that no further data can be expected. In this case the host must send an AFM packet with both the DAF and the appropriate DTA bits set in order to terminate both the fragmented message and the TA.
6. The above operation is repeated for every enabled TA.

8.8.5 MESSAGE FRAGMENTATION

The FLEX™ frame length limits the maximum number of message codewords that can be associated with an address codeword. Messages longer than 84 codewords must be sent as several fragments. The PCD5008 uses AFM (Section 8.8.3) to allow the reception of fragmented messages.

The fragments of a message are sent in sequence. Each fragment contains a checksum character to detect errors in the fragment, a message number to identify which message the fragment is a part, and the continue bit which either indicates that more fragments are in queue or that the last fragment has been received. Each fragment also contains a fragment number starting with 3 for the first fragment and then incremented through the sequence 0, 1 or 2 in subsequent fragments. This allows the detection of missing fragments.

Message fragments may not be separated by more than 32 frames (1 minute) or 128 frames (4 minutes), as indicated by the service provider. During the reception of a fragmented message, the PCD5008 examines every frame for additional fragments until the last fragment is encountered or the host determines that more than 32 or 128 frames have elapsed since the reception of the previous message fragment.

The sequence for the host and the PCD5008 to receive a fragmented message is as follows:

1. The PCD5008 receives an address codeword followed by a vector indicating one of:
   a) Secure (vector type = 000)
   b) Alphanumeric (vector type = 101)
   c) Hexadecimal/binary (vector type = 110).

   The PCD5008 passes the address, vector and message codewords to the host as packets and increments its internal AFM counter and enters AFM.
2. While in AFM, the PCD5008 decodes all of the frames passing any address, vector and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
3. Every time the host receives a secure, alphanumeric or hexadecimal/binary vector packet, it inspects the message continued flag (C) in the first message packet:
   a) If this is not a fragmented message (C is clear and no fragmented messages are in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a temporary address, then the appropriate DTA bit should also be set in the AFM packet.
   b) If this is the first fragment of a fragmented message (C is set and no fragmented messages are in progress for this address and message number), then the host does not decrement the AFM counter and expects further fragments to be received for this address in subsequent frames.
   c) If this is the second or subsequent fragment of a fragmented message and further fragments will follow, (C is set and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set.
   d) If this is the last fragment of a fragmented message, (C is clear and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by 2, sending 2 AFM packets to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then one of these AFM packets should also have the appropriate DTA bit set.
4. If, on receiving a status packet, the host determines that more than 32 or 128 frames have elapsed since the reception of a fragment for a fragmented message then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then the appropriate DTA bit should also be set in the AFM packet.
5. When no fragmented messages are in progress (the AFM counter = 0) and no TAs are pending (all TA counters = 0) and the FAF bit is clear in the AFM packet, the PCD5008 leaves AFM.

As an alternative to the above scheme, the host may choose to decrement the AFM counter at the end of the entire message by decrementing it once for each fragment received. This method is limited to a maximum of 127 fragments.

Tables 57 and 58 show examples of message reception with and without message fragmentation.

Table 57 Alphanumeric message without fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 0; no more fragments are expected
4th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

Table 58 Alphanumeric message with fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 1; message is fragmented, more expected
4th	status		1	end of frame indication (EOF = 1)
5th	address 1	B	1	address 1 is received
6th	vector 1	B	2	vector = alphanumeric type
7th	message	B	2	message word received; C bit = 1; message is fragmented, more expected
8th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
9th	status		1	end of frame indication (EOF = 1)
10th	address 1	A	1	address 1 is received
11th	vector 1	A	2	vector = alphanumeric type
12th	message	A	2	message word received; C bit = 0; no more fragments are expected
13th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
14th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

8.8.5.1 *Fragmentation of non-7-bit character sets*

FLEX™ alphanumeric messages can be used to send symbolic characters like Chinese, Kanji, etc. In this case several ASCII characters are used to represent each symbolic character. Enhanced fragmentation (EF) rules are provided by FLEX™ to allow character positions within a fragment to be determined in the event of missing fragments under poor signal conditions:

1. The pager must remove <NUL> characters from the end of fragments (where they are used as fill characters) so that the displayed message is not affected. To determine character boundaries, <NUL> (00H) characters in all other positions must be considered a result of channel errors. This allows each fragment to end with a complete character and does not disrupt pagers which do not follow all the EF rules.
2. The last fragment of a message containing symbolic characters is completed by filling unused character positions with <ETX> (03H) characters or <NUL> characters. When a message ends at exactly the last character position of the last BCH codeword, no additional <ETX> is required.
3. The U and V bits (Table 45) which aid decoding, are available in all fragments following the initial fragment. In the first fragment the message starts in the default character mode (U and V = 10). For subsequent fragments the definition of the U and V field is as shown in Table 59. When the U and V field is 00, characters may be split between fragments. When the U and V field is not 00, each fragment starts on a character boundary with the character mode defined as in Table 59.

8.8.6 MESSAGE CHECKSUMS

FLEX™ provides a message checksum facility for alphanumeric, numeric, hex/binary, and secure messages. The checksum is calculated by summing the information bits of each codeword in the message or message fragment (including control information and termination characters and bits in the last message codeword). Information bits of each codeword are broken into three groups as indicated in Table 60. Bits i_0, i_8 and i_{16} are the LSBs of each group and bit i_0 is the first bit of the codeword to be transmitted. The 3 groups are for each codeword are added to form a binary sum. The message checksum is the 1's complement of the LSBs of the binary sum, where the number of bits taken is determined by the message type (Section 8.7.8).

In the case of the 6-bit message checksum used in numeric messages, a binary sum is first calculated as described above. The binary sum is then truncated to its 8 LSBs, then the 2 MSBs are shifted right by 6 bits and added to the least significant 6 bits to form a new binary sum. The 6 LSBs of this new sum are taken and 1's complemented to form the 6-bit message checksum.

8.8.7 MESSAGE NUMBERING

FLEX™ messages may be numbered (Section 8.7.8), in this case the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in numerical order. The maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. When a message number is missed, the subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval.

Messages which can be received out of sequence are indicated by clearing the message retrieval flag R. Messages with R cleared number should not be included in the missed message calculation.

In case of fragmented messages, this number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

Table 59 Fragmentation control bit definitions

U_0	V_0	DEFINITION
0	0	EF not supported in controller
0	1	reserved (for a second alternate character mode)
1	0	default character mode start position 1
1	1	alternate character mode start position 1

Table 60 Bit groups for message checksums

i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
group 1								group 2								group 3				

9 LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	−0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current (any input)		−10	+10	mA
I_O	DC output current (any output)		−10	+10	mA
V_I	input voltages (all inputs)	note 2	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−65	+150	°C

Notes

1. V_{DD1} and V_{DD2} respectively V_{SS1} and V_{SS2} must be connected at the same potential.
2. $V_{I(max)}$ = 5.0 V.

10 DC CHARACTERISTICS

T_{amb} = −25 to +70 °C; V_{DD} = 2.2 V; f = 76.8 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	2.2	3.6	V
$I_{DD(stby)}$	standby supply current	on = 0; note 1	–	4.2	10	µA
I_{DD}	operating supply current	on = 1; note 2	–	4.4	–	µA
Digital inputs: OSCPD, TEST2, TEST3, $\overline{\text{RESET}}$, LOBAT, EXTS0, EXTS1, $\overline{\text{SS}}$ and MOSI						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_{LI}	LOW/HIGH-level input leakage current		–	–	1	µA
Digital outputs: MISO, $\overline{\text{READY}}$, CLKOUT, SYMCLK and S0 to S7						
V_{OL}	LOW-level output voltage	I_{sink} = 0.8 mA	–	0.1	0.4	V
V_{OH}	HIGH-level output voltage	I_{source} = −0.8 mA	V_{DD} − 0.4	V_{DD} − 0.1	–	V
I_{LO}	LOW/HIGH-level output leakage current	3-state outputs	–	–	1	µA

Notes

1. External clock signal (frequency = 76.8 kHz, amplitude = V_{SS} to V_{DD}) at pin EXTAL; OSCPD = HIGH; test inputs = LOW; other inputs = HIGH; outputs unconnected (note that any additional capacitive load at pin CLKOUT increases the supply current); SPI transmit enabled; to obtain the supply current of an application with a crystal connected as in Fig.18, a typical oscillator current of 2 µA needs to be added to this value (see Chapter 12); T_{amb} = 25 °C.
2. As note 1, but PCD5008 configured via SPI and synchronous to a typical FLEX™ data stream (collapse value = 4), T_{amb} = 25 °C.

11 AC CHARACTERISTICS

T_{amb} = −25 to +70 °C, V_{DD} = 1.8 to 3.6 V, f_{EXTAL} = 76.8 kHz, maximum load capacitance = 50 pF connected to any digital output; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset timing						
$t_{W(rst)}$	$\overline{\text{RESET}}$ pulse width		200	–	–	ns
$t_{LH(RESET-READY)}$	$\overline{\text{RESET}}$ LOW to $\overline{\text{READY}}$ HIGH		–	–	200	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	stable 76.8 kHz clock	–	1	–	s
Start-up timing						
$t_{strt(osc)}$	oscillator start-up time	see Fig.18	–	1	–	s
$t_{h(rst)}$	$\overline{\text{RESET}}$ hold time		200	–	–	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	note 1	–	76800	–	T
$t_{WUL(osc-READY)}$	oscillator warmed up to $\overline{\text{READY}}$ LOW		–	1	–	s
SPI timing						
f_{SCK}	operating frequency		0	–	1	MHz
$T_{cy(SCK)}$	cycle time		1000	–	–	ns
t_{LEAD1}	select lead time		200	–	–	ns
t_{LAG1}	de-select lag time		200	–	–	ns
$t_{d(SS-READY)}$	$\overline{\text{SS}}$-to-$\overline{\text{READY}}$ delay time	previous packet did not program an address word; note 2	–	–	80	µs
		previous packet programmed an address word; note 2	–	–	420	µs
t_{READYH}	$\overline{\text{READY}}$ HIGH time		50	–	–	µs
t_{LEAD2}	$\overline{\text{READY}}$ lead time		200	–	–	ns
t_{LAG2}	$\overline{\text{READY}}$ lag time		–	–	200	ns
$t_{su(i)(D)}$	MOSI data setup time		200	–	–	ns
$t_{h(i)(D)}$	MOSI data hold time		200	–	–	ns
$t_{ACC(o)}$	MISO access time		0	–	200	ns
$t_{o(dis)}$	MISO disable time		–	–	300	ns
t_{DOV}	MISO data valid time		–	–	200	ns
$t_{h(o)(D)}$	MISO data hold time		0	–	–	ns
t_{SSH}	$\overline{\text{SS}}$ HIGH time		200	–	–	ns
t_{SCKH}	SCK HIGH time		300	–	–	ns
t_{SCKL}	SCK LOW time		300	–	–	ns
t_r	SCK rise time	10% to 90% V_{DD}	–	–	1	µs
t_f	SCK fall time	10% to 90% V_{DD}	–	–	1	µs

Notes

1. T is one period of the 76.8 kHz clock source. Note that from power-up, the oscillator start-up time can influence the availability and period of clock strobes. This can affect the $\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW timing.
2. When the host re-programs an address word with a host-to-decoder packet ID > 7FH, there is an added delay before the PCD5008 is ready for another packet.

12 OSCILLATOR CHARACTERISTICS

T_{amb} = −25 to +70 °C; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_1	external capacitor at pin EXTAL	note 1	–	15	–	pF
C_2	external capacitor at pin XTAL	note 1	–	15	–	pF
R_f	external feedback resistor	note 1	–	10	–	MΩ
$g_{m(osc)}$	oscillator transconductance	V_{DD} = 1.8 V	9.4	19.6	–	μS
		V_{DD} = 3.6 V	–	22.6	50	μS
I_{osc}	oscillator operating supply current	V_{DD} = 2.2 V; note 2	–	2	–	μA

Notes

1. Designed for quartz crystal type: SEIKO VTC200 or equivalent; parameters: f = 76800Hz, R_S = 35 kΩ (max.), $C_L = (C_1//C_2) + C_{stray}$ = 8 to 12 pF, C_0 = crystal shunt capacitance = 0.8 pF (typ.), C_f = typical parasitic pin capacitance = 2 pF; maximum overall frequency tolerance (including transmitter) is 300 ppm (Section 8.4.4).
2. Extracted from evaluations under conditions as in Fig.18; this value is strongly dependent on external conditions (load and parasitic capacitances).

13 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

15 TEST AND APPLICATION INFORMATION

15.1 Example application

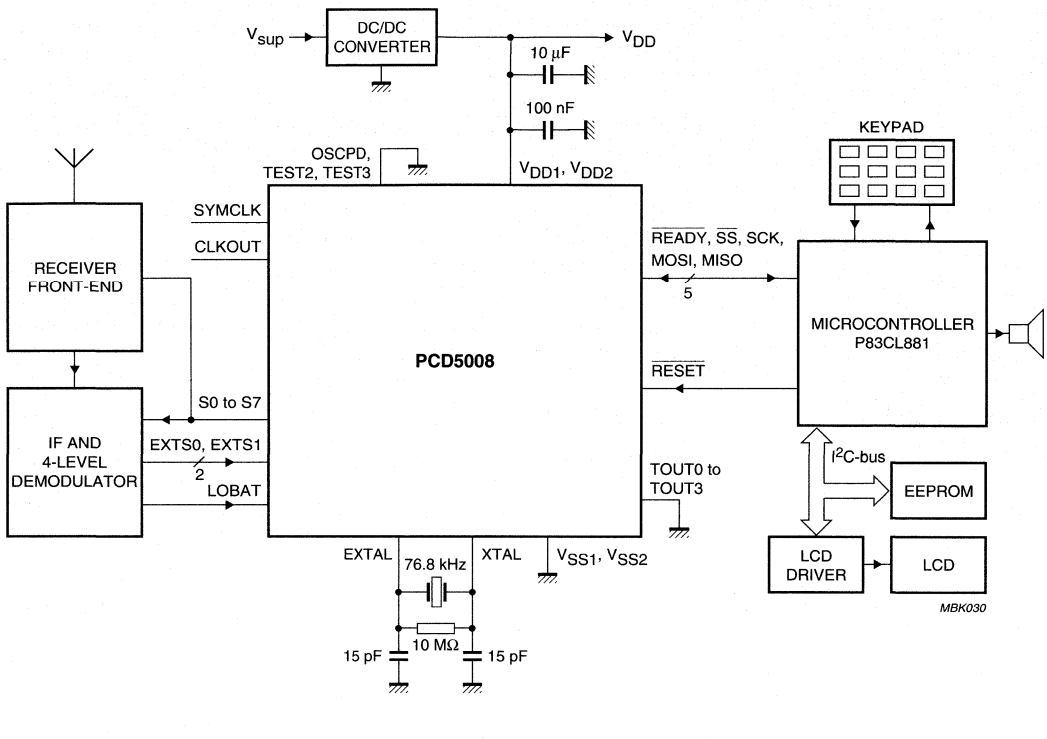


Fig.18 Example application.

15.2 System block diagram

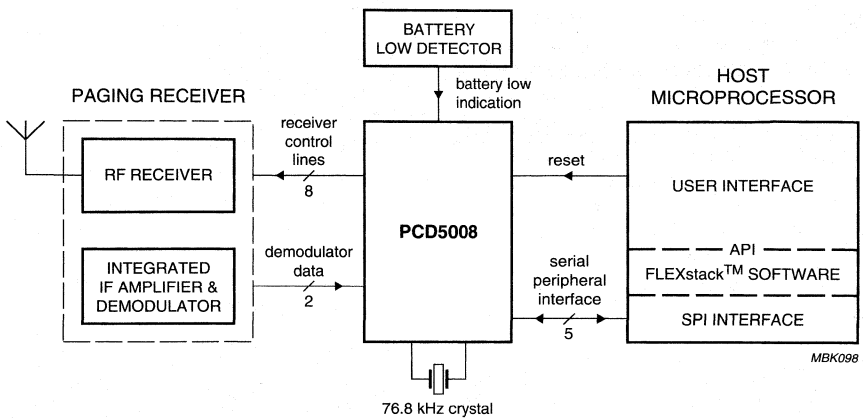


Fig.19 System block diagram.

15.3 FLEX™ encoding and decoding rules

The encoding and decoding rules identify the minimum requirements which must be met by the paging device, paging terminal or other encoding equipment to properly format a FLEX™ data stream for RF transmission and to successfully decode it.

15.3.1 FLEX™ ENCODING RULES

The FLEX™ encoding rules are as follows:

- The stability of the encoder clock used to establish time positions of FLEX™ frames must be no worse than ±25 ppm (including worst case temperature and aging effects).
- A maximum of 2 occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for decoding devices that support any-phase addressing, an any-phase address may appear at once in two different phases in a single multi-phase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new fragmented transmission until the first fragmented transmission has been completed.
- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0$ = 011, 100 and 111) cannot be fragmented, and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (i.e. at least once a minute) or 1 every 128 frames (i.e. at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment in order to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- Message numbers must be assigned sequentially in ascending order.
- Message number sequences must be separately maintained for each individual and radio group address.
- Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- When a missed message is re-transmitted from message retrieval storage, the message must have R = 0 to avoid creating an out of sequence message which may cause the pager to indicate a missed message.

15.3.2 FLEX™ DECODING RULES

The FLEX™ decoding rules are as follows:

- FLEX™ decoding devices may implement either single-phase addressing or any-phase addressing.
- FLEX™ decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- FLEX™ decoding devices that support the alphanumeric vector type ($V_2V_1V_0$ = 101) must support the numeric vector type ($V_2V_1V_0$ = 011) and the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00, FLEX™ paging devices that implement any-phase and support the alphanumeric vector type ($V_2V_1V_0$ = 101) must also support the short instruction vector ($V_2V_1V_0$ = 001) with the instruction type ($i_2i_1i_0$) set to 000.
- FLEX™ decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode. They are: 1600 bps 2 level; 3200 bps 2 level; 3200 4 level and 6400 bps 4 level.
- FLEX™ decoding devices must be designed to tolerate 4 minute fragment separation times.

CONTENTS

FLEX™ roaming decoder II PCD5013

1 FEATURES

- FLEX™ paging protocol decoder
- 16 programmable user address words
- 16 fixed temporary addresses
- 16 operator messaging addresses
- 1600, 3200 and 6400 bits/s decoding
- Any-phase or single-phase decoding
- Uses standard Serial Peripheral Interface (SPI) in slave mode
- SSID and NID roaming support
- Backward compatible to the standard and roaming FLEX™ decoder ICs
- Allows low current power-down mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX™ fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- Low cost LQFP32 plastic package
- Optional internal 4-level FSK demodulator and data slicer
- Operates using a 76.8 or 160 kHz crystal
- Very low power consumption
- Operates at low supply voltage
- Full support for revision 1.9 of the FLEX™ protocol.

2 APPLICATIONS

- Numeric FLEX™ pagers
- Alphanumeric FLEX™ pagers
- Roaming FLEX™ pagers
- Remote metering
- Car security systems
- Personal digital assistants.

3 GENERAL DESCRIPTION

This data sheet describes the operation of the PCD5013 integrated paging decoder. It is fully compatible with other FLEXchip™ ICs including the PCD5008.

The PCD5013, also referred to as the decoder, simplifies implementation of a FLEX™ paging device, by being able to interface with several off-the-shelf paging receivers and host microcontrollers/processors. Its primary function is to process information received and demodulated from a FLEX™ radio paging channel, select messages addressed to the paging device and communicate the message information to the host.

The PCD5013 fully supports the FLEX™ protocol (version G1.9) including all roaming aspects.

Motorola FLEXstack™ software, installed on the product host processor, communicates with the PCD5013 and interprets the codewords that are passed to the host.

The PCD5013 operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when monitoring a single channel for message information.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	2.2	3.6	V
I_{DD}	supply current	see Chapters 12 and 14	–	6.0	–	µA
T_{amb}	operating ambient temperature		−25	+25	+70	°C
f_{EXTAL}	external clock frequency	internal demodulator not in use	–	76.8	–	kHz
		internal demodulator in use	–	160.0	–	kHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5013H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

6 BLOCK DIAGRAM

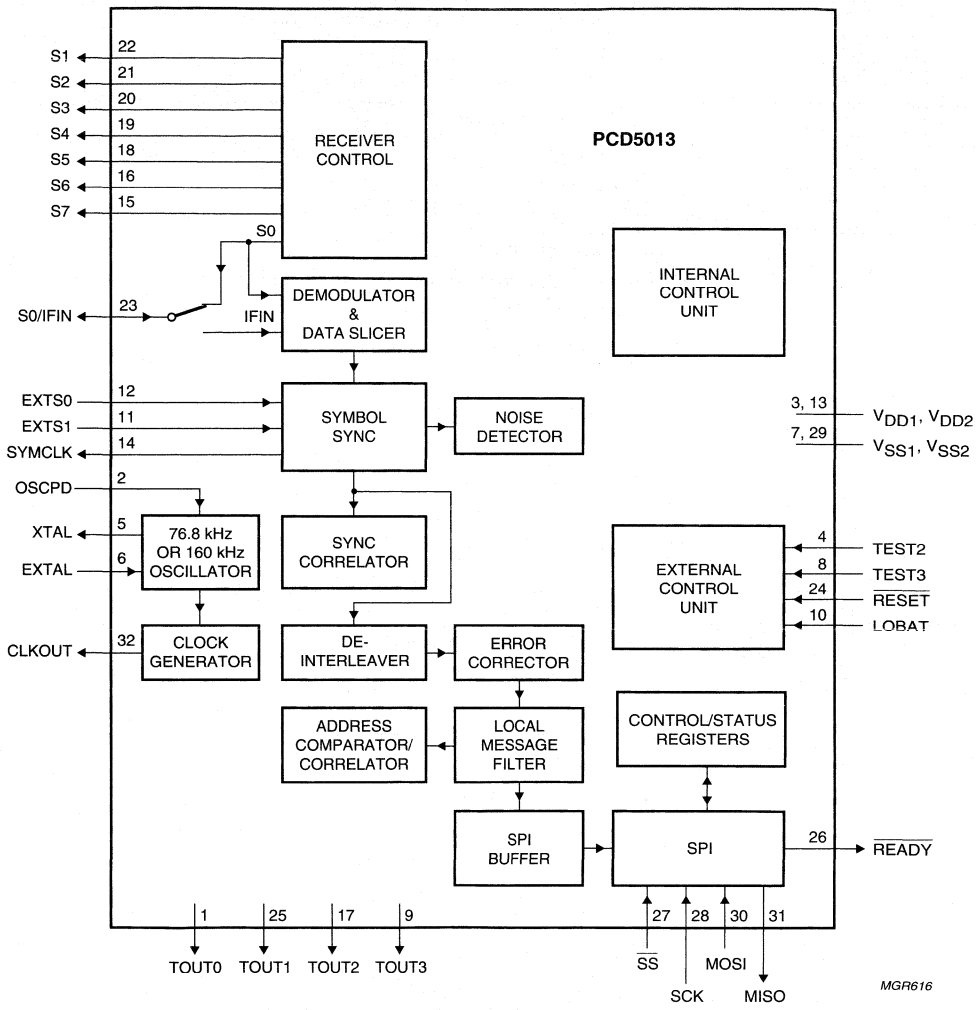


Fig.1 Functional block diagram for PCD5013 pager decoder.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
TOUT0	1	O	3-state test output; note 1
OSCPD	2	I	internal oscillator power-down; connected to V_{SS} when using the internal oscillator, connected to V_{DD} when using an external source
V_{DD1}	3	–	supply voltage
TEST2	4	I	manufacturing test mode input pin; has to be connected to V_{SS}
XTAL	5	O	76.8 or 160 kHz crystal oscillator output
EXTAL	6	I	76.8 or 160 kHz crystal oscillator input or external clock input
V_{SS1}	7	–	ground supply
TEST3	8	I	manufacturing test mode input pin; has to be connected to V_{SS}
TOUT3	9	O	3-state test output; note 1
LOBAT	10	I	low battery voltage detect input
EXTS1	11	I	most significant bit (MSB) of the symbol currently being decoded
EXTS0	12	I	least significant bit (LSB) of the symbol currently being decoded
V_{DD2}	13	–	supply voltage
SYMCLK	14	O	recovered symbol clock output
S7	15	O	receiver control output port, 3-state
S6	16	O	receiver control output port, 3-state
TOUT2	17	O	3-state test output; note 1
S5	18	O	receiver control output port, 3-state
S4	19	O	receiver control output port, 3-state
S3	20	O	receiver control output port, 3-state
S2	21	O	receiver control output port, 3-state
S1	22	O	receiver control output port, 3-state
S0/IFIN	23	I/O	receiver control output port, 3-state when using external demodulator; limited IF input 455 or 140 kHz when using internal demodulator
$\overline{\text{RESET}}$	24	I	active LOW reset input
TOUT1	25	O	3-state test output; note 1
$\overline{\text{READY}}$	26	O	output driven LOW when the PCD5013 is ready for an SPI packet
$\overline{\text{SS}}$	27	I	slave select input for SPI communications
SCK	28	I	serial clock input for SPI communications
V_{SS2}	29	–	ground supply
MOSI	30	I	data input for SPI communications
MISO	31	O	data output for SPI communications, 3-state
CLKOUT	32	O	38.4 kHz clock output (derived from 76.8 kHz oscillator); note 2

Notes

1. These test outputs may be either left unconnected or connected to V_{SS} in the application.
2. For a 160 kHz oscillator either a 38.4 or a 40 kHz output frequency can be selected. See Section 8.4.4.

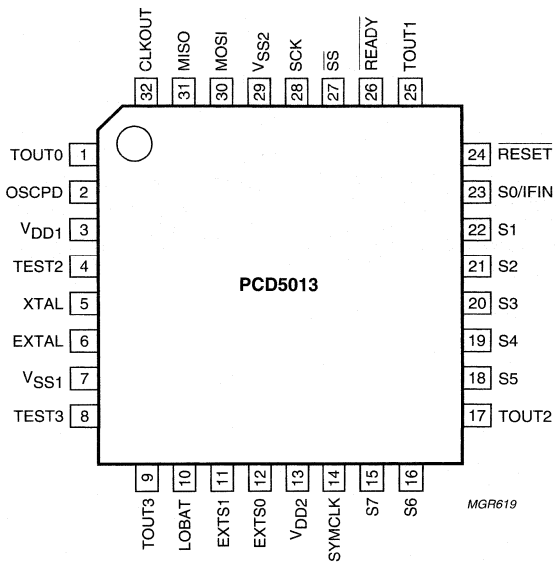


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The PCD5013 simplifies implementation of a FLEX™ paging device by interfacing with off-the-shelf components such as a paging receiver and a microcontroller or microprocessor (called a host). The PCD5013 is fully compatible with FLEXstack™ software which provides a complete, platform independent, software driver for the PCD5013.

The PCD5013 fully supports all aspects of the FLEX™ protocol (version G1.9), and can operate in either single-phase or any-phase mode. The PCD5013 supports FLEX™ dynamic grouping, allowing up to 16 temporary addresses to be enabled simultaneously. It is also capable of retrieving real time information from a FLEX™ channel.

The PCD5013 connects to any receiver capable of providing a 2-bit digital signal. The PCD5013 operates the paging receiver in an efficient power consumption mode. The PCD5013 has 8 receiver control lines used for warming up, operating and shutting down a receiver in stages.

The PCD5013 has the ability to detect a battery-low signal from an external detector during the receiver control sequences.

The PCD5013 carries out the following functions:

- Synchronises to a FLEX™ data stream
- Processes received, demodulated information
- Performs de-interleaving and error correction
- Selects calls addressed to the paging device using up to 16 programmable addresses
- Communicates the message information to the host.

The PCD5013 interfaces to a host through a serial peripheral interface (SPI). The host can then interpret the message information in an appropriate manner (numeric, alphanumeric, binary, etc.). This function is provided by the FLEXstack™ software.

When configured to use the internal demodulator, the PCD5013 connects to a receiver capable of generating a limited (i.e. 1-bit digitized) 455 or 140 kHz IF signal (IF frequency automatically detected).

The PCD5013 enables the host to operate in a low-power mode when monitoring a single channel for message information. It has a 38.4 kHz clock output (40 kHz available when using the internal demodulator) capable of driving other devices, and has a 1-minute timer that offers low-power support for a real-time clock function on the host.The host can use receiver control lines which are not required by the receiver as expansion ports to control other peripheral devices.

8.2 Clocking, reset and start-up

8.2.1 OSCILLATOR

The PCD5013 uses an inverting crystal oscillator. The clock signal for the internal circuitry is derived via an amplifier from the oscillator input pin EXTAL. Alternatively, an external clock signal can be fed in at input pin EXTAL. In this case the internal oscillator can be disabled by pulling the OSCPD input pin HIGH. This reduces current consumption and routes EXTAL directly to the internal clock signal. When using a crystal, an external feedback resistor and the load capacitances need to be connected to pins EXTAL and XTAL (Fig.19). See Chapter 14 for the recommended crystal parameters and the specification of the oscillator transconductance to guarantee correct start-up.

The PCD5013 oscillator can operate at either 76.8 kHz or 160 kHz by selecting the appropriate crystal. The choice of frequency is determined by the setting of the IDE bit in the configuration packet; see Section 8.4.4.

8.2.2 RESET AND START-UP CONDITIONS

The PCD5013 is reset by pulling the $\overline{\text{RESET}}$ input LOW. After releasing the $\overline{\text{RESET}}$ by pulling it HIGH, the PCD5013 counts 76 800 clock cycles (independent of the oscillator frequency) before pulling $\overline{\text{READY}}$ LOW to indicate that the decoder is ready for configuration via the SPI.

See Fig.3 and Chapter 13 for the PCD5013 timing specifications when power is applied.

See Fig.4 and Chapter 13 for the PCD5013 timing specifications when it is reset.

After switch-on, the PCD5013 operates in Asynchronous mode, periodically sampling the channel for incoming data. As soon as data is detected, the PCD5013 maintains the receiver on to synchronize to the channel. Once the pager is synchronized to the channel it enters Synchronous mode, switching the receiver on only for the programmed frames.

When the receiver is programmed for Roaming operation, the PCD5013 sends information which allows the host to calculate when to switch frequencies in a roaming network.

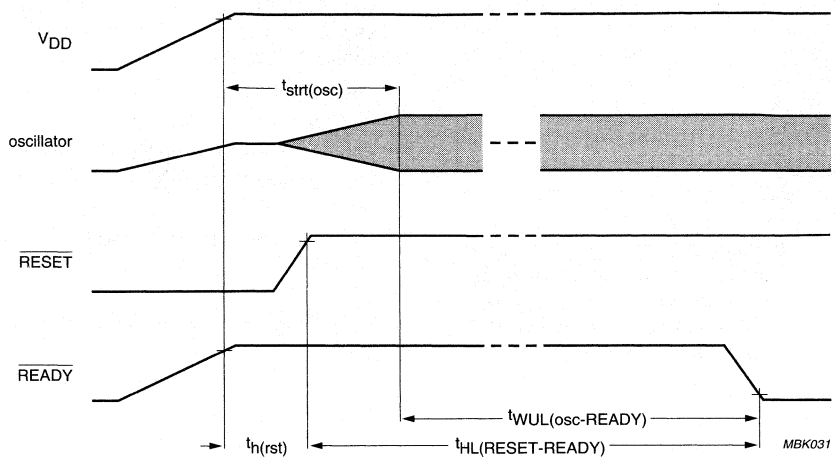


Fig.3 Start-up timing.

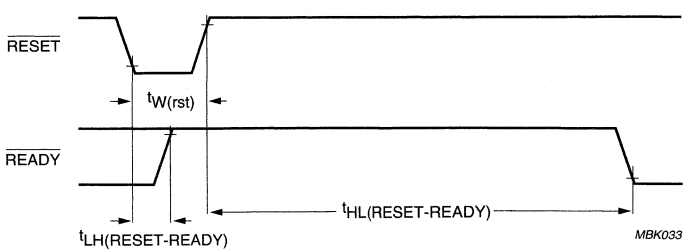


Fig.4 Reset timing.

8.3 Serial Peripheral Interface (SPI)

8.3.1 GENERAL

All data communication between the PCD5013 and the host is done via the SPI using 32-bit data packets at data rates up to 1 Mbits/s. SPI transfers are full-duplex and can be initiated by either the host which acts as the SPI master providing the data clock for packet transfer, or the PCD5013 as an SPI slave.

The host can send packets to configure or control the PCD5013 or a checksum packet to validate SPI communication (Section 8.4.2). The PCD5013 buffers data packets, relating to received data, into a 32 packet transmit buffer. The PCD5013 can send either a status packet, a part ID packet, or packets from the transmit buffer. In the event of a buffer overflow, the PCD5013 stops decoding and clears the transmit buffer.

8.3.2 SPI INTERCONNECT

Connection on the PCD5013 consists of a $\overline{\text{READY}}$ pin and 4 SPI pins ($\overline{\text{SS}}$, SCK, MOSI and MISO):

$\overline{\text{READY}}$: output signal; indicates that data is available from the PCD5013

$\overline{\text{SS}}$: SPI select; used as PCD5013 chip select

SCK: serial clock; output from the host used for clocking data

MOSI: master output slave input; data output from the host

MISO: master input slave output; data output from the PCD5013.

8.3.3 SPI TRANSFER INITIATED BY THE HOST

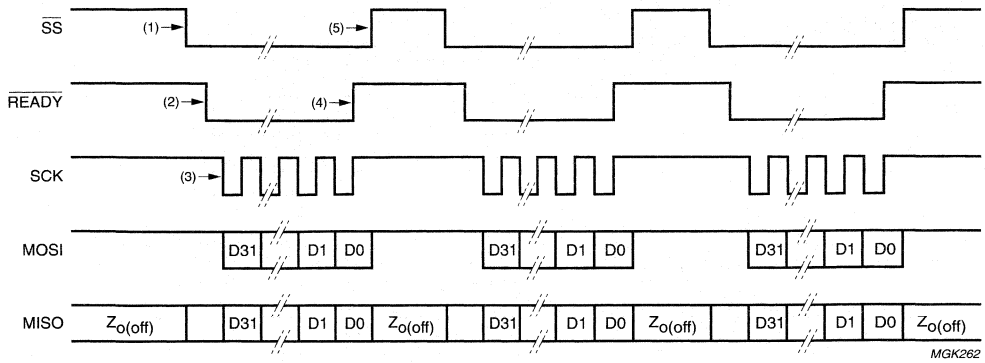
The following steps occur when the host initiates an SPI packet transfer, see Fig.5 for event timings:

1. The host selects the PCD5013 by driving the $\overline{\text{SS}}$ pin LOW.
2. The PCD5013 indicates that it is ready to start the SPI transfer by driving the $\overline{\text{READY}}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5013 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5013 pulls the $\overline{\text{READY}}$ line HIGH, to indicate that the transfer is complete.
5. The host waits until the $\overline{\text{READY}}$ line is pulled HIGH, then de-selects the PCD5013 SPI by driving the $\overline{\text{SS}}$ pin HIGH.
6. The first 5 steps are repeated for each additional packet.

8.3.4 SPI TRANSFER INITIATED BY THE DECODER

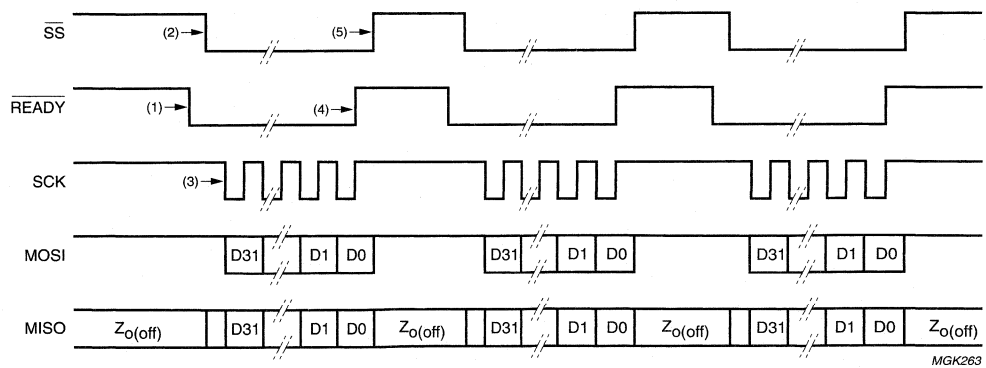
The following steps occur when the PCD5013 initiates an SPI packet transfer, see Fig.6 for event timings:

1. The PCD5013 initiates the SPI transfer by driving the $\overline{\text{READY}}$ pin LOW.
2. If the PCD5013 is not already selected, the host selects the PCD5013 SPI by driving the $\overline{\text{SS}}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5013 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5013 pulls the $\overline{\text{READY}}$ line HIGH, to indicate that the transfer is complete.
5. The host may then either de-select the SPI interface of the PCD5013 (Fig.7) by driving the $\overline{\text{SS}}$ pin HIGH or maintain $\overline{\text{SS}}$ LOW to continue sending packets to the PCD5013.



Numbers within parenthesis refer to sequence numbers, see Section 8.3.3.

Fig.5 Typical multiple SPI transfers initiated by the host.



Numbers within parenthesis refer to sequence numbers, see Section 8.3.4.

Fig.6 Typical multiple SPI transfers initiated by the PCD5013.

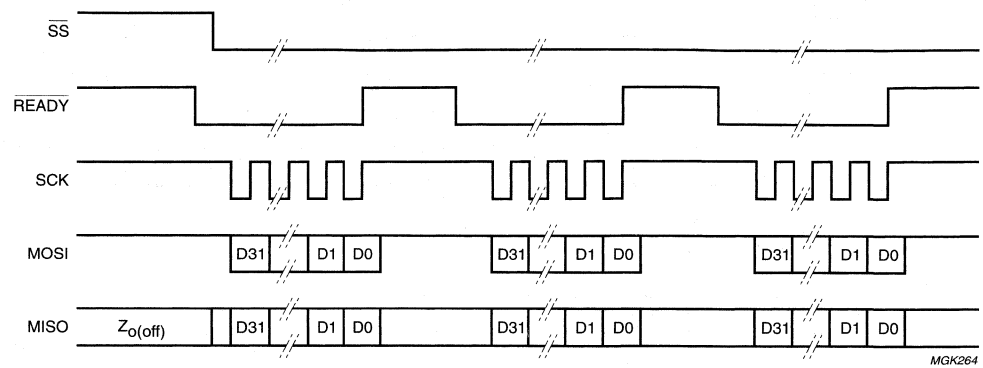


Fig.7 Multiple SPI transfers initiated by the PCD5013 with $\overline{SS}$ maintained LOW.

8.3.5 SPI PACKET FORMAT

SPI data packets consist of an 8-bit ID (byte 3), followed by 24 bits of information (byte 2 to byte 0). See Table 1, note that bit 7 of byte 3 is the first bit on the bus.

8.3.6 SPI TIMING

See Fig.8 and Chapter 13 for the timing specifications of the SPI.

Table 1 Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	D31	D30	D29	D28	D27	D26	D25	D24
2	D23	D22	D21	D20	D19	D18	D17	D16
1	D15	D14	D13	D12	D11	D10	D9	D8
0	D7	D6	D5	D4	D3	D2	D1	D0

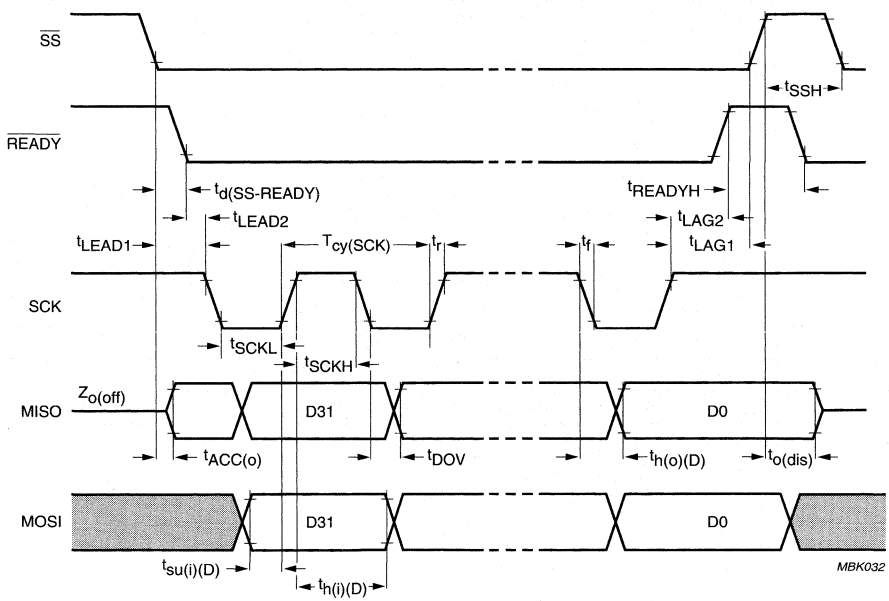


Fig.8 SPI timing.

8.3.7 HOST-TO-DECODER PACKETS OVERVIEW

This section summarises the packets which can be sent from the host to the decoder.

Table 2 Host-to-decoder packet ID map2

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	checksum	8.4.6
01	configuration	8.4.4
02	control	8.4.7
03	all frame mode	8.8.4
04	operator message address enable	8.6.9
05	roaming control	8.4.9
06	timing control	8.4.10
07 to 0E	reserved (host should never send)	–
0F	receiver line control	8.5.7
10	receiver control configuration (off setting)	8.5.4
11	receiver control configuration (warm-up 1 setting)	8.5.5.3
12	receiver control configuration (warm-up 2 setting)	8.5.5.3
13	receiver control configuration (warm-up 3 setting)	8.5.5.3
14	receiver control configuration (warm-up 4 setting)	8.5.5.3
15	receiver control configuration (warm-up 5 setting)	8.5.5.3
16	receiver control configuration (3200 sps sync setting)	8.5.6.2
17	receiver control configuration (1600 sps sync setting)	8.5.6.2
18	receiver control configuration (3200 sps data setting)	8.5.6.2
19	receiver control configuration (1600 sps data setting)	8.5.6.2
1A	receiver control configuration (shut-down 1 setting)	8.5.8.1
1B	receiver control configuration (shut-down 2 setting)	8.5.8.1
1C to 1F	special (ignored by decoder)	–
20	frame assignment (frames 112 to 127)	8.6.7
21	frame assignment (frames 96 to 111)	8.6.7
22	frame assignment (frames 80 to 95)	8.6.7
23	frame assignment (frames 64 to 79)	8.6.7
24	frame assignment (frames 48 to 63)	8.6.7
25	frame assignment (frames 32 to 47)	8.6.7
26	frame assignment (frames 16 to 31)	8.6.7
27	frame assignment (frames 0 to 15)	8.6.7
28 to 77	reserved (host should never send)	–
78	user address enable	8.6.6
79 to 7F	reserved (host should never send)	–
80	user address assignment (user address 0)	8.6.6
81	user address assignment (user address 1)	8.6.6
82	user address assignment (user address 2)	8.6.6

PACKET		
ID (HEX)	**TYPE**	**SECTION**
83	user address assignment (user address 3)	8.6.6
84	user address assignment (user address 4)	8.6.6
85	user address assignment (user address 5)	8.6.6
86	user address assignment (user address 6)	8.6.6
87	user address assignment (user address 7)	8.6.6
88	user address assignment (user address 8)	8.6.6
89	user address assignment (user address 9)	8.6.6
8A	user address assignment (user address 10)	8.6.6
8B	user address assignment (user address 11)	8.6.6
8C	user address assignment (user address 12)	8.6.6
8D	user address assignment (user address 13)	8.6.6
8E	user address assignment (user address 14)	8.6.6
8F	user address assignment (user address 15)	8.6.6
90 to FF	reserved (host should never send)	–

8.3.8 DECODER-TO-HOST PACKETS OVERVIEW

This section summarises the packets which can be sent from the PCD5013 to the host (Table 3).

Table 3 Decoder-to-host packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	block information word	8.7.9
01	address	8.7.2
02 to 57	vector or message (ID is word number in frame)	8.7.3 and 8.7.8
58 to 5F	reserved	–
60	roaming status	8.4.13
61 to 7D	reserved	–
7E	receiver shutdown	8.4.12
7F	status	8.4.11
80 to FE	reserved	–
FF	part ID	8.4.5

8.4 Configuration and synchronisation

8.4.1 GENERAL

After a reset, all configuration data has to be (re)loaded into the PCD5013 by the host using the SPI. PCD5013 features which do not change during operation are configured using the configuration packet (Section 8.4.4), the receiver control packets (Section 8.5) and the address configuration packets (Section 8.6). PCD5013 features which can be changed during operation are configured using the control packet. The checksum packet ensures proper communication between the host and the PCD5013.

8.4.2 SPI SECURITY ALGORITHM

The PCD5013 provides a security algorithm to verify correct SPI operation (Figs 9 and 10). The PCD5013 maintains a checksum register equal to the result of XORing the 24 data bits of every packet it receives, except the checksum packet 00H and special packets 1CH to 1FH. When the PCD5013 is reset, the internal checksum register is initialized to the 24-bit part ID defined in the part ID packet.

Immediately following a reset and whenever the host sends a packet other than a checksum packet, the SPI output of status and data (SPI transmit) is disabled. The PCD5013 then initiates SPI transfers continuously, sending the part ID packet (Section 8.4.5). Note that when SPI transmit is disabled all decoding and timing functions are unaffected. The SPI transmit can be enabled by sending a checksum packet for which the checksum value matches the checksum register.

Checksum packets sent when the SPI transmit is enabled, are ignored by the PCD5013 irrespective of the value of the checksum packet data bits. Thus when the PCD5013 initiates an SPI transfer and the host has no data to send, the host should send the checksum packet so as not to disable the SPI transmit. The data in the checksum packet could be a null packet (32-bit stream of all zeros).

Sending a packet other than the checksum packet when the SPI transmit is enabled causes the SPI transmit to be disabled until a checksum packet is sent with the correct value. Thus when the host re-configures the PCD5013 after a reset, the SPI transmit is disabled until the host sends a checksum packet at the end of the configuration data, with the checksum value equal to the result of XORing together the data bits of each of the configuring packets and the data bits of the part ID packet.

If the SPI transmit is enabled and a receiver shutdown packet is pending, the receiver shutdown packet is sent. If there is no receiver shutdown packet pending, but there is a roaming status packet pending, the roaming status packet is sent. If neither the receiver shutdown packet nor the roaming status packet is pending and there is data in the transmit buffer, the PCD5013 initiates an SPI transfer sending a packet from its transmit buffer. The PCD5013 sends the status packet (which is not buffered) when the host initiates an SPI transfer and the transmit buffer is empty.

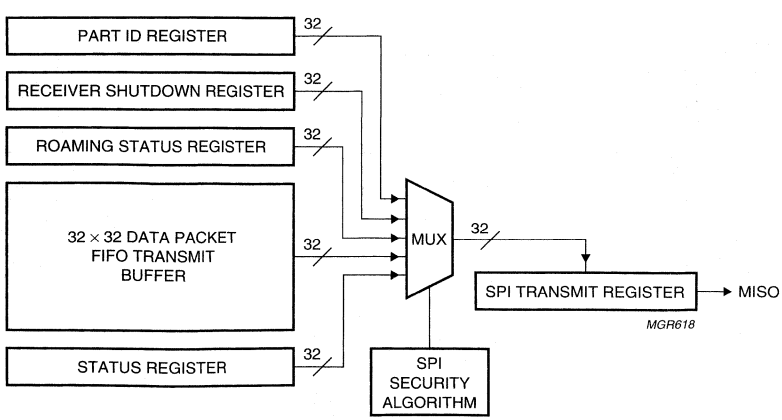


Fig.9 SPI transmit functional block diagram.

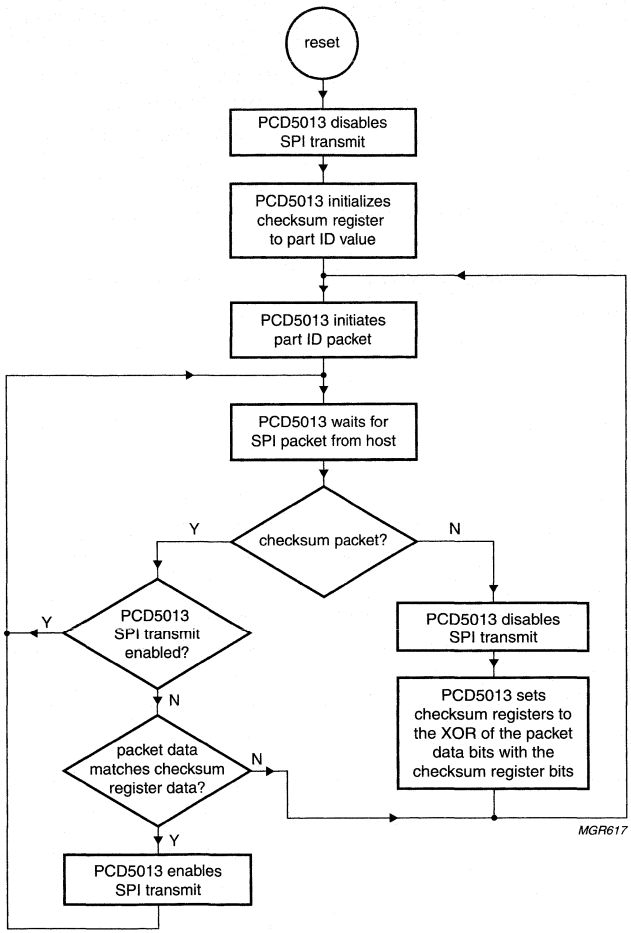


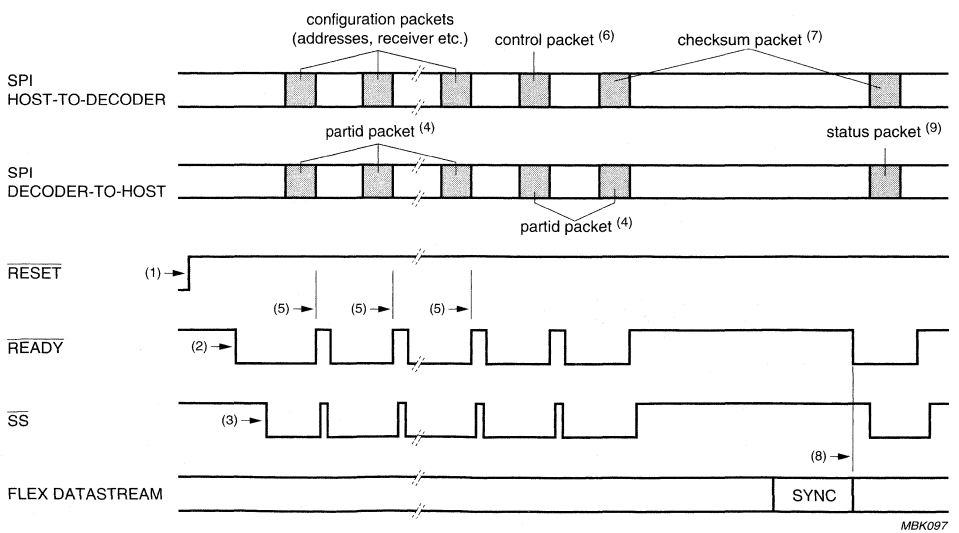
Fig.10 SPI security algorithm.

8.4.3 CONFIGURATION SEQUENCE

A typical configuration and synchronisation sequence would be as follows, see Fig.11 for event timings:

1. The PCD5013 is reset by the host.
2. After 76800 clock cycles the PCD5013 interrupts the host to read the part ID by pulling the $\overline{\text{READY}}$ line LOW.
3. The host pulls $\overline{\text{SS}}$ LOW at the start of each SPI transfer and clocks out the part ID data.
4. The host configures the following aspects of PCD5013 operation:
   a) General configuration (Section 8.4.4)
   b) Receiver operation (Section 8.5)
   c) FLEX™ CAPCODE configuration (Section 8.6).

   The PCD5013 writes a part ID packet in response to each incoming packet.
5. At the end of each packet the PCD5013 pulls the $\overline{\text{READY}}$ line HIGH, and then LOW again to indicate that packet processing is complete.
6. The host writes a control packet to enable FLEX™ decoding in the PCD5013 (Section 8.4.7).
7. The host writes a checksum packet to enable SPI data output by the PCD5013 (Section 8.4.2).
8. On recognising a SYNC word, the PCD5013 synchronises to the channel.
9. The PCD5013 initiates an SPI transfer writing the status packet, indicating that it is now in synchronous mode.



Numbers within parenthesis refer to sequence numbers, see Section 8.4.3.

Fig.11 Typical configuration and synchronization sequence.

8.4.4 CONFIGURATION PACKET (ID = 01H)

The configuration packet defines a number of different configuration options for the PCD5013. The PCD5013 ignores this packet when decoding is enabled, i.e. the ON bit in the control packet is set (Table 12).

DFC: disable fractional clock (Table 8). When this bit is set and IDE is set, the CLKOUT signal generates a 40 kHz signal (EXTAL divided-by-4). When this bit is cleared and IDE is set, the CLKOUT signal generates a 38.4 kHz signal (EXTAL fractionally divided by $^{25}/_{6}$). This bit has no effect when IDE is cleared. Value after reset = 0.

IDE: internal demodulator enable (Table 8). When this bit is set, the internal demodulator is enabled and the clock frequency at EXTAL is expected to be 160 kHz. When this bit is cleared, the internal demodulator is disabled and the clock frequency at EXTAL is expected to be 76.8 kHz. Value after reset = 0.

OFD: oscillator frequency difference (Tables 4 and 8). These bits represent the maximum frequency difference between the 76.8 kHz oscillator (accounting for ageing, temperature variation, manufacturing tolerance etc.) and the worst case transmitter bit rate (specified as ±25 parts per million (ppm) in the FLEX™ specification).
For example, if the transmitter tolerance is ±25 ppm and the 76.8 kHz oscillator tolerance is ±140 ppm, the transmitter-oscillator frequency difference is ±165 ppm and OFD should be cleared (300 ppm maximum). Value after reset = 0. Note that configuring a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios.

Table 4 Oscillator frequency difference

OFD_1	OFD_0	FREQUENCY DIFFERENCE (ppm)
0	0	±300
0	1	±150
1	0	±75
1	1	±0

PCE: partial correlation enable (Table 8). When this bit is set, partial correlation of addresses is enabled. When partial correlation is enabled, the PCD5013 shuts down the receiver before the end of the last FLEX™ block which contains addresses if it can determine that none of the addresses in that FLEX™ block matches any enabled address in the PCD5013. When this bit is cleared, the receiver is controlled as in the PCD5008. Value after reset = 0.

SP: signal polarity (Tables 8, 5 and 6). These bits set the polarity of EXTS1 and EXTS0 input signals. The polarity of the EXTS1 and EXTS0 bits is determined by the receiver design. Value after reset = 0.

Table 5 Input signal polarity

SP_1	SP_0	SIGNAL POLARITY	
		EXTS1	EXTS0
0	0	normal	normal
0	1	normal	inverted
1	0	inverted	normal
1	1	inverted	inverted

Table 6 FLEX™ 4 level FSK modulation (SP = 00)

EXTS1	EXTS0	DEVIATION (Hz)
1	0	+4800
1	1	+1600
0	1	−1600
0	0	−4800

SME: synchronous mode enable (Table 8). When this bit is set, a status packet is sent automatically whenever the synchronous mode update (SMU) bit in the status packet is set. This happens whenever a change occurs in the synchronous mode (SM) status bit, which indicates that the decoder is synchronized to a FLEX™ data stream. The host can use the SM bit in the status packet as an in-range/out-of-range indication. Value after reset = 0.

COD: clock output disable (Table 8). When this bit is cleared, a 38.4 or 40 kHz signal is output on the CLKOUT pin (depending on the values of IDE and DFC). When this bit is set, the CLKOUT pin is driven LOW. Value after reset = 0.

- Setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4 kHz period.
- When the clock output is enabled and not set for intermittent operation (see ICO in this packet), the CLKOUT pin always outputs the clock signal even when the PCD5013 is in reset (as long as a clock signal is available to the PCD5013 oscillator).
- When the PCD5013 is used in internal demodulator mode (i.e. uses a 160 kHz oscillator), the CLKOUT pin is 80 kHz from reset until the time the IDE bit is set.

LBP: low battery polarity (Table 8). This bit defines the polarity of the PCD5013's LOBAT pin: When this bit is set, a HIGH at input LOBAT represents a low battery condition. The LB bit in the status packet is initialized to the inverse (i.e. inactive) value of the LBP bit when the PCD5013 is turned on (by setting the ON bit in the control packet). When the PCD5013 is turned on, the first low battery update in the status packet is sent to the host when a low battery condition is detected on the LOBAT pin. Value after reset = 0.

MOT: maximum off time (Table 8). When this bit is set, the PCD5013 assumes that the service provider leaves up to 1 minute between transmitted frames. When this bit is clear, the PCD5013 assumes that there can be up to 4 minutes between transmitted frames. This bit has no effect if AST in the Timing Control Packet is non-zero. Value after reset = 0.

MTE: minute timer enable (Table 8). When this bit is set, a status packet is sent at one minute intervals with the minute time-out (MT) bit in the status packet set. When this bit is clear, the internal 1-minute timer stops counting. See Section 8.4.8 for details of 1-minute timer operation. Note that the minute timer is not accurate using a 160 kHz oscillator until the IDE bit is set. Value after reset = 0.

ICO: intermittent clock out (Table 8). When this bit is clear and COD is clear, a 38.4 or 40 kHz (depending on the values of IDE and DFC) signal is output on the CLKOUT pin. When this bit is set and COD is clear, the clock is only output on the CLKOUT pin while the receiver is not in the Off state. The clock is output for a few cycles before the receiver transitions from the off state and for a few cycles after the receiver transitions to the off state (this is to insure that the receiver receives enough clocks to detect and process the changes to and from the off state).
The CLKOUT pin is driven LOW when it is not driving a clock.

Note that when the clock is automatically enabled and disabled (i.e. when ICO is set), the CLKOUT signal transitions are clean (i.e. no pulses less than half the clock period) when it transitions between no clock and clocked output. This bit has no effect when COD is set. Value after reset = 0.

8.4.5 PART ID PACKET (ID = FFH)

The part ID packet is output by the PCD5013 SPI whenever the SPI transmit is disabled due to the checksum feature. The value of the part ID packet for the PCD5013 is FF000308H.

MDL: model (Table 9). The PCD5013 model value is 0.

CID: compatibility ID (Table 9). This value describes other parts with the same model number, which are compatible with this part.

Table 7 CID Compatibilities

BIT	COMPATIBILITY	VALUE FOR PCD5013
CID_0	Alphanumeric Decoder I	1 (true)
CID_1	Roaming Decoder I	1 (true)
CID_2	Numeric Decoder	0 (false)

REV: revision (Table 9). This identifies the manufacturing version of the PCD5013. For the PCD5013 the value is 8.

8.4.6 CHECKSUM PACKET (ID = 00H)

See Table 10 for checksum packet bit assignment.

CV: checksum value (24 bits), see Section 8.4.2.

Table 8 Configuration packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	0	DFC	0	0	0	IDE	OFD_1	OFD_0
1	0	0	0	0	0	PCE	SP_1	SP_0
0	SME	MOT	COD	MTE	LBP	ICO	0	0

Table 9 Part ID packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	1	1	1	1	1	1	1
2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

Table 10 Checksum packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

8.4.7 CONTROL PACKET (ID = 02H)

The control packet defines a number of different control bits for the PCD5013.

FF: force frame 0 to 7 (Table 12). When set, each of these bits forces the PCD5013 to decode one of the FLEX™ frames 0 to 7 irrespective of the system collapse value (for details of collapse values see Section 8.6.2). For example, if the system collapse causes the PCD5013 to decode frames 0, 32, 64 and 96, setting FF_2 causes the PCD5013 to also decode FLEX™ frame 2. This may be used to acquire transmitted time information or channel attributes (e.g. Local ID). Value after reset = 0.

SPM: single phase mode (Table 12). When this bit is set, the PCD5013 decodes only one of the transmitted phases. When this bit is clear, the PCD5013 decodes all transmitted phases. This value is determined by the CAPCODE (Section 8.6). A change to this bit while the PCD5013 is on does not take effect until the next block 0 of a frame. Value after reset = 0.

PS: phase select (Tables 11 and 12). When the SPM bit is set, these bits define which phase the PCD5013 shall decode. This value is determined by the CAPCODE (Section 8.6). A change to these bits, while the PCD5013 is on, does not take effect until the next block 0 of a frame. Value after reset = 0.

Table 11 Phase selection (by PS bits)

PS_1	PS_0	DECODED PHASE (BASED ON FLEX™ DATA RATE)		
		1600 bits/s	3200 bits/s	6400 bits/s
0	0	A	A	A
0	1	A	A	B
1	0	A	C	C
1	1	A	C	D

SBI: send block information words (BIW) 2 to 4 (Table 12). When this bit is set, BIWs with time and date information and BIWs received in error are sent to the host, (Section 8.7.9). Value after reset = 0.

MTC: minute timer clear (Table 12). Setting this bit causes the 1-minute timer to restart from 0 (Section 8.4.8).

ON: turn on decoder (Table 12). When this bit is set, the PCD5013 decodes FLEX™ signals. If this bit is cleared, signal processing stops. However, to assure proper operation, the PCD5013 requires that it be set into asynchronous mode when turned off. To achieve that the following sequence must be used:

1. Send control packet with ON bit clear (decoder off)
2. Send control packet with ON bit set (decoder on)
3. Send control packet with ON bit clear (decoder off).

Timing between these steps is specified below and is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet.

- The minimum time between steps 1 and 2 is the greater of 2 ms or the programmed shut-down time.
  The programmed shut-down time is the sum of all of the times programmed in the used receiver shut-down settings packets.
- There is no maximum time between steps 1 and 2.
- The minimum time between steps 2 and 3 is 2 ms.
- The maximum time between steps 2 and 3 is the programmed warm-up time minus 2 ms.
  The programmed warm-up time is the sum of all the times programmed in the used receiver warm-up settings packets.

EAE: end of addresses enable. When this bit is set, the EA bit in the Status Packet is PCD5013 set immediately after the PCD5013 decodes the last address word in the frame if any of the enabled PCD5013 addresses was detected in the frame. When this bit is cleared, the EA bit is never set.

Table 12 Control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	0
2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
1	0	SPM	PS_1	PS_0	0	0	0	0
0	0	SBI	0	MTC	0	0	EAE	ON

8.4.8 Operating the 1-minute timer

The PCD5013 provides a 1-minute timer which allows the host to implement a time-of-day function while maintaining low-power operation. The 1-minute timer is enabled using the MTE bit in the configuration packet (Section 8.4.4). When the 1-minute timer is enabled, a status packet is sent at 1-minute intervals with the MT bit set (Section 8.4.11). When the MTE bit is clear, the internal 1-minute timer stops counting. When the host sends a control packet with MTC bit set, the 1-minute timer restarts from 0. This allows accurate setting of a time-of-day function.

8.4.9 Roaming Control Packet (ID = 05H)

The roaming control packet controls the features of the PCD5013 that allow implementation of a roaming pager.

IRS: ignore re-synchronization signal (Table 13). When this bit is set, the PCD5013 does not go asynchronous when detecting an Ar or $\overline{Ar}$ signal during searches for A-words. It merely reports that the re-synchronization signal was received by setting RSR to 1 in the Roaming Status packet. This allows the host to decide what to do when the paging device is synchronous to more than one channel and only one channel is sending the re-synchronization signal. It also prevents the PCD5013 from losing synchronization when it detects the re-synchronization signal while the paging device is checking an unknown channel. This bit is set and cleared by the host. Value after reset = 0.

NBC: network bit check (Table 13). Setting this bit enables reporting of the received network bit value (NBU and n) in the Roaming Status Packet. Setting this bit also makes the PCD5013 abandon a frame after the Frame Info word without synchronizing to the frame if the frame information word is uncorrectable or if the n bit in the frame information word is not set. If the PCD5013 is in synchronous mode when this occurs (probably due to synchronizing to a second channel), it maintains synchronization to the original channel. If the PCD5013 is in asynchronous mode when this occurs, it stays in asynchronous mode and end the A-word search. This is done to avoid synchronizing to a non-roaming channel when searching for roaming channels. This bit is set and cleared by the host. Value after reset = 0.

MCM: manual collapse mode (Table 13). When this bit is set, the PCD5013 behaves as if the system collapse was 7. The PCD5013 does not apply the received system collapse to the AF bits. When this bit is set, the received system collapse is reported to the host via SCU and RSC in the Roaming Status Packet. This is so the host can modify the AF bits based on the system collapse of the channel. This bit is set and cleared by the host. Value after reset = 0.

IS1: invert EXTS1 (Table 13). Setting this bit inverts the expected polarity of the EXTS1 pin from the way it is configured by SP 1 in the Configuration Packet (e.g. if both IS1 and SP 1 are set, the polarity of the EXTS1 pin is untouched). This bit is intended to be changed when a change in a channel changes the polarity of the received signal. This bit is set and cleared by the host. This bit has the equivalent effect when using the internal demodulator. Value after reset = 0.

SDF: stop decoding frame (Table 13). Setting this bit causes the PCD5013 to stop decoding a frame without losing frame synchronization. This bit is set by the host, and cleared by the PCD5013 once it has been processed. The packet with the SDF bit set must be sent after receiving the status packet with EA bit set. It must be sent within 40 ms of the end of block in which the PCD5013 set the EA bit. Value after reset = 0.

RSP: receiver shutdown packet enable (Table 13). When this bit is set, a Receiver Shutdown Packet is sent whenever the receiver is shut down. The receiver shutdown packet informs the host that the receiver shutdown, and gives the time period before the PCD5013 automatically warms the receiver back up. Value after reset = 0.

Table 13 Roaming Control Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	1	0	1
2	IRS	NBC	MCM	IS1	SDF	RSP	SND	CND
1	RND	ABI	SAS	DAS	AF_{11}	AF_{10}	AF_9	AF_8
0	0	0	MFC_1	MFC_0	0	0	MCO_1	MCO_0

SND: start noise detect (Table 13). Setting this bit while the PCD5013 is battery saving causes it to warm-up the receiver, run a noise detect, and report the result of the noise detect via NDR in the Roaming Status Packet. This bit is set by the host, and cleared by the PCD5013 once it has been processed. If the time comes for the PCD5013 to warm-up automatically or the SAS bit is set while an SND is being processed, the noise detect is abandoned and the abandoned noise detect result (NDR = 01) is sent in the Roaming Status Packet. Value after reset = 0.

CND: continuous noise detect (Table 13). Setting this bit causes the PCD5013 to do continuous noise detects during the decoded block data of a frame. The results of the noise detect is only reported if noise is detected (NDR = 11). Only one noise detected result (NDR = 11) is sent per block. If the PCD5013 has not completed a noise detect when it shuts down for the frame, that noise detect is abandoned, but no abandon result (NDR = 01) is sent. This bit is set and cleared by the host. Value after reset = 0.

RND: report noise detects (Table 13). Setting this bit causes the PCD5013 to report the results of the noise detects it does under normal asynchronous operation (when first turned on and when asynchronous). The results of the noise detect is reported via NDR in the Roaming Status Packet. This bit is set and cleared by the host. Value after reset = 0.

ABI: all block information words (Table 13). When this bit is set, the PCD5013 sends all received Block Information words 2-4 to the host. Note: Setting the SBI bit in the Control Packet only enables errored and real-time clock related block info words. Value after reset = 0.

SAS: start A-word search (Table 13). Setting this bit while in asynchronous battery save mode causes the PCD5013 to warm-up the receiver and run an A-word search. If, during the A-word search, the PCD5013 finds sufficient FLEX™ signal, it enters synchronous mode and start decoding the frame. If the A-word search times-out without finding sufficient FLEX™ signal, it enters a battery save mode and continue doing periodic noise detects.

The time-out for the A-word searches is controlled by the AST bits in the Timing Control Packet and the MOT bit in the Configuration Packet. The A-word search takes priority over noise detects. Therefore, if the PCD5013 is performing an A-word search and the time comes to do automatic noise detect, the noise detect is not performed. This bit is set by the host, and cleared by the PCD5013 once it has been acted on. Value after reset = 0.

MFC: missed frame control (Tables 14 and 13). These bits control the frames for which missing frame data (MS1, MFI, MS2, MBI, and MAW) is reported in the Roaming Status Packet. Value after reset = 0.

Table 14 Missed Frame Control (MFC bits)

MFC_1	MFC_0	MISSING FRAME DATA REPORTED
0	0	never
0	1	only during frames 0 through 3
1	0	only during frames 0 through 7
1	1	always

MCO: maximum carry on (Table 13). The value of these bits sets the maximum carry on that the PCD5013 follows. For example, if the PCD5013 receives a carry on of 3 over the air and MCO is set to 1, the PCD5013 only carries on for one frame. Value after reset = 3.

DAS: disable A-word search (Table 13). When this bit is set, an A-word search does not automatically occur after a noise detect in asynchronous mode finds FLEX™ signal. This includes automatic noise detects and noise detects initiated by the host by setting SND. The PCD5013 shuts down the receiver after the noise detect completes regardless of the result. When this bit is cleared, A-word searches occur after a noise detect finds signal in asynchronous mode. Value after reset = 0.

8.4.10 Timing Control Packet (ID = 06H)

The timing control packet gives the host control of the timing used when the PCD5013 is in asynchronous mode. The packet ID for the timing control packet is 6.

AST: A-word search time (Table 15). The value of these bits sets the A-word search time for all asynchronous A-word searches in units of 80 ms (e.g. value of 1 is 80 ms, a value of 2 is 160 ms, etc.). If the value is 0, the PCD5013 defaults to the 1-minute (MOT = 1) or 4-minute (MOT = 0) A-word search time controlled by the MOT bit in the configuration packet. Value after reset = 0.

ABT: asynchronous battery-save time (Table 15). The value of these bits sets the battery save time (time from the beginning of one automatic noise detect to the beginning of the next automatic noise detect) in asynchronous mode in units of 80 ms (e.g. value of 1 is 80 ms, a value of 2 is 160 ms, etc.) If the value is 0, the battery save time is set to the default value of 1.5 seconds. The minimum allowed ABT is 320 ms, therefore values of 1, 2, 3, and 4 are invalid. Value after reset = 0.

8.4.11 Status Packet (ID = 7FH)

The status packet contains various types of information that the host may require and is sent to the host:

- Whenever the PCD5013 is polled and has no other data to send
- On events for which the PCD5013 is configured to send the status packet (Sections 8.4.4 and 8.4.7). In this case, the PCD5013 prompts the host to read a status packet for the following conditions:
  - SMU bit in the status packet and the SME bit in the configuration packet are set
  - MT bit in the status packet and the MTE bit in the configuration packet are set
  - EOF bit in the status packet is set
  - LBU bit in the status packet is set
  - EA bit in the status packet is set
  - BOE bit in the status packet is set.

FIV: frame information valid (Table 16). This bit is set, when a valid frame information word has been received since becoming synchronous to the system and the f and c fields contain valid values. If this bit is clear, no valid frame information words have been received since the PCD5013 became synchronous to the system. This value changes from 0 to 1 at the end of block 0 (Fig.18) of the frame in which the first frame information word was properly received. It is cleared when the PCD5013 goes into asynchronous mode (see SM bit below). This bit is initialized to 0 when the PCD5013 is reset and when the PCD5013 is turned off by clearing the ON bit in the control packet.

f: current frame number (Table 16). This value is updated every frame regardless of whether the PCD5013 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

c: current system cycle number (Table 16). This value is updated every frame regardless of whether the PCD5013 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: synchronous mode (Table 16). This bit is set, when the PCD5013 is synchronous to the system. The PCD5013 sets this bit when the first synchronization words are received. It clears this bit when the PCD5013 has not properly received both synchronization words in any frame for 8, 16, or 32 minutes (depending on the number of assigned frames and the system collapse). This bit is initialized to 0 when the PCD5013 is reset and when it is turned off by clearing the ON bit in the control packet.

Table 15 Timing Control Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AST_7	AST_6	AST_5	AST_4	AST_3	AST_2	AST_1	AST_0
0	ABT_7	ABT_6	ABT_5	ABT_4	ABT_3	ABT_2	ABT_1	ABT_0

SMU: synchronous mode update (Table 16). This bit is set if the SM bit has been updated in this packet. After the PCD5013 has been turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search period (meaning the receiver is active during this time) expires (SM stays 0), after the PCD5013 is turned on. The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial search period expires. After the initial synchronous mode update, the SMU bit is set whenever the PCD5013 switches from/to synchronous mode. The bit is cleared when read. Changes in the SM bit due to turning off the PCD5013 does not set the SMU bit. This bit is initialized to 0 when the PCD5013 is reset.

LB: low battery (Table 16). Set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the receiver control packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the configuration packet, when the PCD5013 is turned on, by setting the ON bit in the control packet.

LBU: low battery update (Table 16). This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. The bit is cleared when read. The host controls when the LOBAT pin is read via the receiver control packets. Changes in the LB bit due to turning on the PCD5013 do not cause the LBU bit to be set. This bit is initialized to 0 when the PCD5013 is reset.

EOF: end of frame (Table 16). Set when the PCD5013 is in all frame mode (AFM) (Section 8.8.4), and the end of the frame has been reached. The PCD5013 is in the AFM if the AFM enable counter is non-zero, if any temporary address enabled (TAE) counter is non-zero (Section 8.8.4) or if the FAF bit in the AFM packet is set. The bit is cleared when read and initialized to 0 when the PCD5013 is reset.

MT: minute time-out (Table 16). Set if one minute has elapsed. The bit is cleared when read. This bit is initialized to 0 when the PCD5013 is reset.

BOE: buffer overflow error (Table 16). Set when information has been lost owing to slow host response time. When the PCD5013 detects that its SPI transmit buffer has overflowed, it clears the transmit buffer, turns off decoding by clearing the ON bit in the control packet, and sets this bit. The bit is cleared when read. This bit is initialized to 0 when the PCD5013 is reset.

EA: end of addresses (Table 16). If EAE of the control packet is set and an address is detected in a frame, EA is set after the PCD5013 processes the last address in the frame. Since data packets take priority over the status packet, the status packet with the EA bit set is guaranteed to come after all address packets for the frame. Cleared when read. This bit is initialized to 0 when the PCD5013 is reset.

x: unused bits (Table 16). The value of these bits is not guaranteed.

8.4.12 Receiver Shutdown Packet (ID = 7EH)

The Receiver Shutdown Packet is sent in both synchronous and asynchronous mode. It is designed to indicate to the host that the receiver is turned off and how much time there is until the PCD5013 automatically turns it back on. This enables the host to perform other tasks such as monitoring other pager channels.

FNV: frame number valid (Table 17). This bit is set if the last decoded frame information word was correctable and the frame number was the expected value. When in asynchronous mode, this value is 0.

CF: current frame (Table 17). When in synchronous mode, this is the current frame number. This value is latched on the negative edge of the READY line when this packet is sent to the host. The value of this field is valid only if the PCD5013 is in synchronous mode and the FIV bit in the status packet is set. When in asynchronous mode, this value is 0.

TNF: time to next frame (Table 17). When in synchronous mode TNF indicates the time to the start of the A-word check if the PCD5013 were to warm-up for the next frame. When in asynchronous mode TNF indicates the time to the start of the next automatic noise detect. See section 8.8.9 for an explanation on how to use this value. This value is latched on the negative edge of the READY line when this packet is sent to the host.

FCO: frame carried on (Table 17). Set if the PCD5013 is decoding the next frame due to the reception of a non-zero carry-on value in the current or a previous frame. When in asynchronous mode, this value is 0.

NAF: next assigned frame (Table 17). This is the frame number of the next frame the PCD5013 was scheduled to decode when the receiver shut down. The value of this field is valid only if the PCD5013 is in synchronous mode and the FIV bit in the status packet is set. When in asynchronous mode this value is 0.

Table 16 Status packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	1	1	1
2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	SM	LB	x	x	c_3	c_2	c_1	c_0
0	SMU	LBU	x	MT	x	EOF	EA	BOE

Table 17 Receiver Shutdown Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	1	1	0
2	FNV	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1	TNF_7	TNF_6	TNF_5	TNF_4	TNF_3	TNF_2	TNF_1	TNF_0
0	FCO	NAF_6	NAF_5	NAF_4	NAF_3	NAF_2	NAF_1	NAF_0

8.4.13 Roaming Status Packet (ID = 60H)

The PCD5013 automatically prompts the host to read a Roaming Status Packet if RSR, MS1, MFI, MS2, MBI, MAW, NBU, NDR 1, NDR 0, or SCU is set.

RSR: re-synchronization signal received (Table 19). Set when the PCD5013 detected a re-synchronization signal (Ar/$\overline{Ar}$) and the host configured the PCD5013 to ignore it via the IRS bit in the roaming control packet. This bit is cleared when read.

MS1: missed synchronization 1 (Table 19). Set when the PCD5013 fails to detect the first synchronization pattern (A/$\overline{A}$) of a FLEX™ frame and the PCD5013 was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is cleared when read.

MFI: missed frame information word (Table 19). Set when the frame information word is received with an uncorrectable number of errors and the PCD5013 was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is cleared when read.

MS2: missed synchronization 2 (Table 19). Set when the PCD5013 failed to detect the second synchronization pattern (C/$\overline{C}$) of a frame and PCD5013 was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is cleared when read.

MBI: missed block information word 1 (Table 19). Set when at least one of the block information word ones is received with an uncorrectable number of errors and PCD5013 was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is set no more than once per frame regardless of the number of missed block information word 1's in the frame. This bit is cleared when read.

MAW: missed address word (Table 19). Set when any address words in the address field is received with an uncorrectable number of errors and PCD5013 was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is set no more than once per frame regardless of the number of missed address words in the frame. This bit is cleared when read.

NBU: network bit update (Table 19). Set when the NBC bit in the roaming control packet is set and a frame information word is received with a correctable number of errors. This bit is not set when the frame information word is not received due to missing the first synchronization pattern (A/$\overline{A}$). This bit is cleared when read.

n: network bit value (Table 19). When NBU is set, this is the value of the n bit in the last received frame information word.

NDR: noise detect result (Tables 18 and 19). These bits indicate the result of a noise detect. The results of noise detects initiated by setting the SND bit in the roaming control packet is always reported. The results of the automatic noise detects performed in asynchronous mode is only reported if the RND bit is set in the roaming control packet. When continuous noise detects during block data are enabled by setting the CND bit in the roaming control packet, only the 'No FLEX™ signal detected' result is reported. These bits are cleared when read.

Table 18 Noise Detect Result (NDR bits)

NDR_1	NDR_0	NOISE DETECT RESULT
0	0	No Information
0	1	Noise Detect was abandoned
1	0	FLEX™ signal detected
1	1	FLEX™ signal not detected

SCU: system collapse update (Table 19). Set when the PCD5013 is configured for manual collapse mode by setting the MCM bit in the roaming control packet and the system collapse of a frame is received. This bit is set no more than once per frame regardless of the number of phases in the frame. This bit is not set in frames in which no block information word 1's is received properly. This bit is cleared when read.

RSC: received system collapse (Table 19). When SCU is set, this value represents the system collapse value that was received in the frame.

Table 19 Roaming Status packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	0	0	0	1	0
2	RSR	MS1	MFI	MS2	MBI	MAW	NBU	n
1	x	x	x	x	x	x	NDR_1	NDR_0
0	x	x	x	x	SCU	RSC_2	RSC_1	RSC_0

8.5 Receiver control interface

8.5.1 General

The PCD5013 has 8 programmable receiver control lines, S0 to S7. The host can program via SPI packets what setting is applied to the receiver control lines, the duration of warm-up and shut-down stages and the polling of the LOBAT pin. This programmability allows the PCD5013 to interface with many off-the-shelf receiver ICs. Note that these packets are ignored when sent while decoding is enabled (ON bit is set in the control packet).

8.5.2 Low battery detection

The PCD5013 can be configured to poll the LOBAT pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the PCD5013 activates the next setting on the receiver control lines. The PCD5013 sends a status packet whenever the value differs from the previous time that the LOBAT pin was polled.

8.5.3 Receiver settings at reset

The receiver control ports are 3-state outputs which are set to high impedance when the PCD5013 is reset, until the corresponding FRS bit in the receiver line control packet is set or the PCD5013 is turned on for the first time after a reset (by setting the ON bit in the control packet).

This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the PCD5013.

8.5.4 Receiver off state (ID = 10H)

The receiver off state is configured by the receiver off setting packet (Table 20), which defines the settings to be applied when the PCD5013 decides to switch the receiver off.

LBC: low battery check (Table 20). If this bit is set, the PCD5013 checks the status of the LOBAT port just before leaving the receiver off state. Value after reset = 0.

CLS: control line setting (Table 20). This is the value to be output on the receiver control lines for the receiver off state. Value after reset = 0.

ST: step time (Table 20). This sets the duration of the warm-up off time. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 159.375 ms (ST = FFH). Value after reset = 01H.

Table 20 Receiver off setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	0	0	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.5 RECEIVER WARM-UP SEQUENCES

8.5.5.1 Normal receiver warm-up sequence

The PCD5013 allows for up to 6 steps associated with warming-up the receiver. When the PCD5013 turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS1 and EXTS0 input pins.

1. The PCD5013 leaves the receiver control lines in the off state for the programmed warm-up off time.
2. The first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting.
3. Subsequent warm-up settings are applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found.
4. At the end of the last used warm-up setting, the 1600 symbols per second (sps) sync setting or the 3200 sps sync setting is applied to the receiver control lines depending on the PCD5013 current state.

The PCD5013 must be configured such that the sum of all of the used warm-up times and the warm-up off time does not exceed 160 ms. If it exceeds 160 ms, the PCD5013 executes the receiver shut-down sequence 160 ms after the start of the warm-up off time. If the sum of all of the used warm-up times and the warm-up off times is less than 160 ms, the receiver remains in the 1600 sps sync setting or the 3200 sps sync setting from the end of the last used warm-up setting until valid signals are expected (160 ms after the start of the warm-up off time). Figure 12 shows the receiver warm-up sequence while decoding, when all warm-up settings are enabled.

8.5.5.2 Host initiated receiver warm-up sequence

A host can initiate a receiver warm-up sequence is by one of the following actions:

- Turning on the PCD5013 by setting the ON bit in the control packet
- Requesting a noise detect by setting the SND bit in the roaming control packet
- Requesting an A-word search by setting the SAS bit in the roaming control packet.

A host initiated receiver warm-up sequence (see Fig.13) differs from the sequence described in Section 8.5.5.1. No receiver warm-up off time is applied, instead the PCD5013 immediately begins to apply the receiver warm-up settings. Once a disabled warm-up setting is found, the "3200 sps sync setting" (for ON and SND warm-ups) or the "1600 sps sync setting" (for SAS warm-ups) is applied to the receiver control lines. The decoder then expects valid signals after the 3200 sps sync warm-up time.

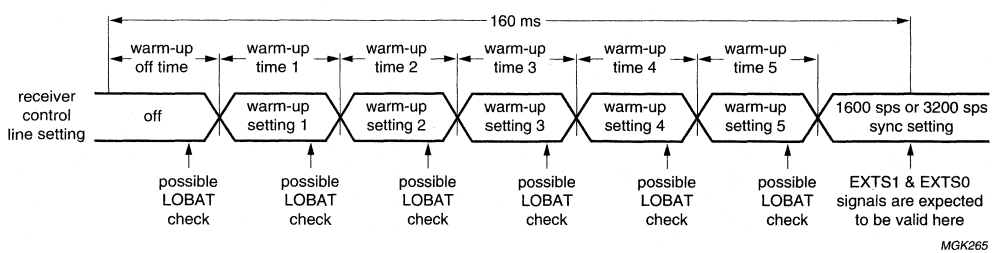


Fig.12 Receiver warm-up sequence while decoding.

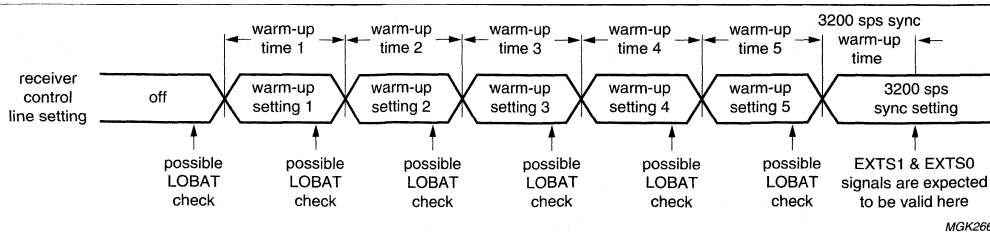


Fig.13 First receiver warm-up sequence after turning decoding on.

8.5.5.3 Receiver warm-up setting packets (ID = 11H to 15H)

CLS: control line setting (Table 22). This is the value to be output on the receiver control lines (S0 to S7) for this receiver warm-up state. Value after reset = 0.

SE: step enable (Table 22). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver warm-up sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 22). If this bit is set, the PCD5013 checks the status of the LOBAT port just before leaving this receiver warm-up state. Value after reset = 0.

ST: step time (Table 22). This sets the duration time for receiver warm-up until the next receiver state. The setting is in 625 µs steps and valid values are:

625 µs (ST = 01H) to 79.375 ms (ST = 7FH).

Value after reset = 01H.

s: setting number, see Tables 21 and 22 for the s names and values and location in the receiver warm-up packet.

Table 21 Receiver warm-up setting numbers

s_3	s_2	s_1	s_0	SETTING NAME
0	0	0	1	warm-up 1
0	0	1	0	warm-up 2
0	0	1	1	warm-up 3
0	1	0	0	warm-up 4
0	1	0	1	warm-up 5

Table 22 Receiver warm-up setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.6 ACTIVE RECEIVER STATES

8.5.6.1 General

In addition to the warm-up and shut-down states, the PCD5013 has four active receiver states. When these settings are applied to the receiver control lines, the PCD5013 is decoding the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the FLEX™ data stream. Because of this, there is no time setting associated with these settings (with the exception of the 3200 sps sync setting).

The four settings are as follows:

1600 sps sync setting: applied when the PCD5013 searches for a 1600 sps signal.

3200 sps sync setting: applied when the PCD5013 searches for a 3200 sps signal.

1600 sps data setting: applied after the PCD5013 has found the C or $\overline{C}$ sync word in the sync 2 section of a 1600 sps frame.

3200 sps data setting: applied after the PCD5013 has found the C or $\overline{C}$ sync word in the sync 2 section of a 3200 sps frame.

Figure 14 shows some examples of how these settings are used in the PCD5013.

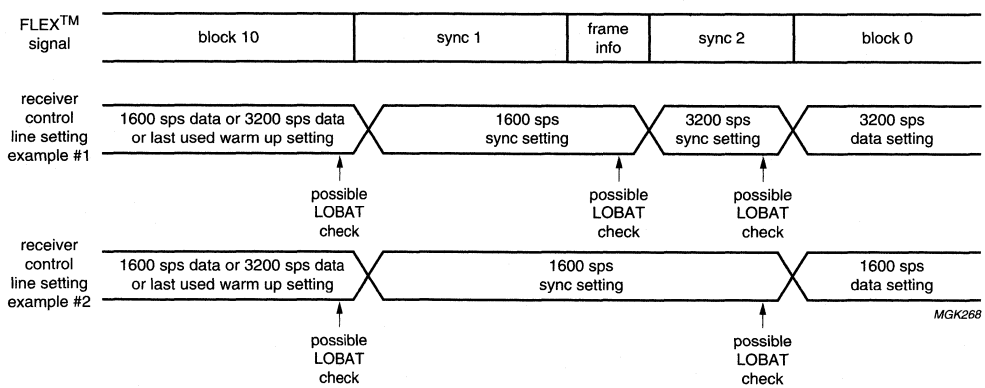


Fig.14 Examples of receiver control transitions.

8.5.6.2 Receiver on setting packets (ID = 16H to 19H)

LBC: low battery check (Tables 24 and 25). If this bit is set, the PCD5013 checks the status of the LOBAT port just before leaving this receiver sync setting state. Value after reset = 0.

CLS: control line setting (Tables 24 and 25). This is the value to be output on the receiver control lines for this receiver sync setting state. Value after reset = 0.

ST: step time (Table 24). This sets the waiting time, before expecting good signals at EXTS1 and EXTS0 at the end of the warm-up sequence, after turning decoding on. The setting is in steps of 625 µs. Valid values are: 625 µs (ST = 01H) to 79.375 ms (ST = 7FH). Value after reset = 01H.

s: setting number, see Tables 23 and 25 for the s names and values and location in the receiver on setting packet.

Table 23 s names and values

s_3	s_2	s_1	s_0	SETTING NAME
0	1	1	1	1600 sps sync
1	0	0	0	3200 sps data
1	0	0	1	1600 sps data

8.5.7 FORCING RECEIVER LINES (ID = 0FH)

This packet (Table 26) enables host control over the receiver control line (S0 to S7) settings in all modes except reset. In reset, the receiver control lines are high impedance.

FRS: force receiver setting (Table 26). Setting a bit causes the associated CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line. Clearing a bit returns control of the corresponding receiver control line to the PCD5013. Value after reset = 0.

CLS: control line setting (Table 26). This bit setting is applied to the corresponding receiver control line if the associated FRS bit is set in this packet. Value after reset = 0.

Table 24 3200 sps sync setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	1	1	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

Table 25 Receiver on setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	0	0	0	0	0	0

Table 26 Receiver line control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	1	1	1	1
2	0	0	0	0	0	0	0	0
1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

8.5.8 Receiver shut-down sequence

The PCD5013 allows up to 3 steps associated with shutting down the receiver. When the PCD5013 decides to turn off the receiver, the first shut-down setting, if enabled, is applied to the receiver control lines for the corresponding shut-down time. At the end of the last used shut-down time, the receiver off setting is applied to the receiver control lines. If the first shut-down setting is not enabled, the PCD5013 switches directly from the receiver on to the receiver off setting.

Figure 15 shows the receiver shut-down sequence when all shut-down settings are enabled. If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the control packet), the PCD5013 immediately executes the receiver shut-down sequence. If the PCD5013 is executing the shut-down sequence when turned on (with the ON bit in the control packet set) the PCD5013 completes the shut-down sequence before starting the warm-up sequence.

8.5.8.1 Receiver shut-down setting packets (ID = 1AH to 1BH)

SE: step enable (Table 28). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver shut-down sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 28). If this bit is set, the PCD5013 checks the status of the LOBAT port just before leaving this receiver shut-down state. Value after reset = 0.

CLS: control line setting (Table 28). This is the value to be output on the receiver control lines (S0 to S7) for this receiver shut-down state. Value after reset = 0.

ST: step time (Table 28). This sets the duration time for receiver shut-down, until the next receiver state. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 39.375 ms (ST = 3FH). Value after reset = 01H.

s: setting number, see Tables 27 and 28 for the s names and values and location in the receiver shut-down packet.

Table 27 s names and values

s	SETTING NAME
0	shut-down 1
1	shut-down 2

Table 28 Receiver shut-down stages

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	1	0	1	s
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

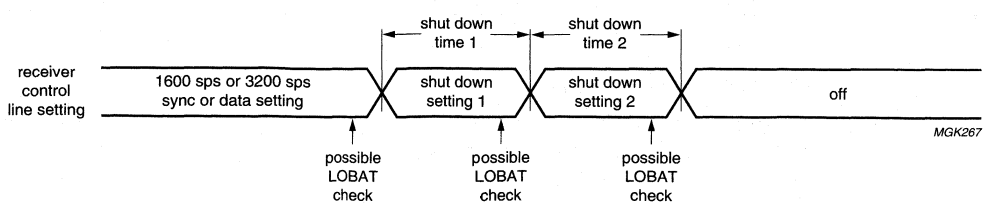


Fig.15 Receiver shut-down sequence.

8.6 Configuration of the FLEX™ CAPCODE

8.6.1 GENERAL

A CAPCODE specifies a decoder address, the collapse value of the address and whether single-phase, any-phase or all-phase address. The PCD5013 supports single-phase and any-phase operation. The FLEX™ protocol provides a standard mechanism to derive phase and frame in which an address should be transmitted. If this mechanism is not used, a CAPCODE also specifies the phase and frame assigned to the address.

8.6.2 CAPCODE FORMAT

The FLEX™ CAPCODE consist of a series of decimal and alphabetic fields, see Fig.16 for the field definitions.

When the FLEX™ standard pager collapse value of 4 (battery cycle of 16 frames) is used, the pager collapse field can be omitted.

The collapse value is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX™ channel. For a given collapse value b, the decoding device looks in every 2^b frames. Thus an address with an assigned base frame of 3 and a collapse value of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e. frames 3, 35, 67 and 99).

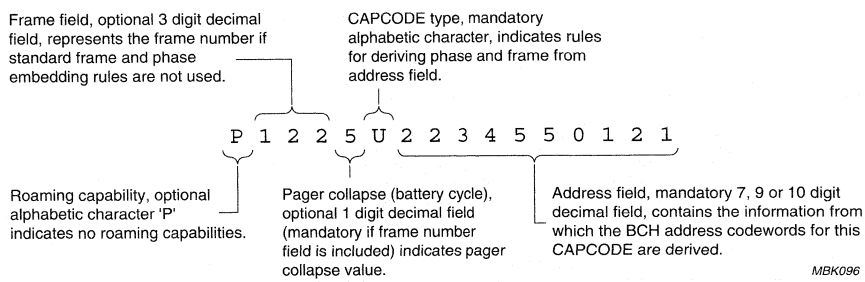


Fig.16 CAPCODE format.

8.6.3 CAPCODE RANGES

A CAPCODE represents user addresses ranging from 1 to 5370810366. A short CAPCODE can have address values below 2031615 and are represented in the data stream by a single address codeword. Some short addresses have been reserved for special purposes: information service addresses, network addresses, temporary (group) addresses and operator messaging addresses.

A long CAPCODE represents addresses situated above 2101248 subdivided into categories (uncoordinated, global, country) to allow different allocation schemes to coexist.

Table 29 defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table 29 CAPCODE assignment table

CAPCODE ADDRESS VALUE		DESCRIPTION
from	to	
0000000000		illegal
0000000001	0001933312	short addresses
0001933313	0001998848	illegal
0001998849	0002009087	reserved for future use
0002009088	0002025471	Information service addresses
0002025472	0002029567	network addresses
0002029568	0002029583	temporary addresses
0002029584	0002029599	operator messaging addresses
0002029600	0002031614	reserved for future use
0002031615	0002101248	invalid, not used
0002101249	0102101250	long address set 1-2 uncoordinated
0102101251	0402101250	long address set 1-2 country; note 1
0402101251	1075843072	long address set 1-2 global; note 2
1075843073	2149584896	long address set 1-3 global; note 2
2149584897	3223326720	long address set 1-4 global; note 2
3223326721	3923326750	long address set 2-3 country; note 1
3923326751	4280000000	long address set 2-3 reserved
4280000001	4285000000	long address set 2-3 information service, global; notes 2 and 3
4285000001	4290000000	long address set 2-3 information service, country; notes 1 and 3
4290000001	4291000000	long address set 2-3 information service, world-wide; notes 3 and 4
4291000001	4297068542	reserved for future use

Notes

1. Country: the addresses are coordinated within each country and with countries along borders.
2. Global: address is coordinated to be unique world-wide.
3. Information service: currently, the rules governing the use of these addresses are not defined.
4. World-wide: 1000 addresses are assigned to each country for world-wide use.

8.6.4 ADDRESS CALCULATION

Address codeword values generally do not coincide with (part of) the user address as specified in the CAPCODE. To find the address codewords corresponding to a user address a conversion has to be done (Table 31). The type of conversion depends on the CAPCODE range in which the user address is located. Note that addresses are transmitted LSB first (differently to POCSAG).

Short addresses, are transmitted in a single address codeword where as long addresses are transmitted in two consecutive address codewords. The first codeword of a long address contains the lower part of the address, the second codeword the upper part. By combining two long address codewords from different banks 6 long address ranges are created: 1 to 2, 1 to 3, 1 to 4, 2 to 3, 2 to 4 and 3 to 4. Ranges 2 to 4 and 3 to 4 are as yet undefined and reserved.

Table 31 describes how to calculate the 21-bit address codeword which is transmitted over the air.

Table 30 Address word range definitions

TYPE	HEX VALUE
Idle word (illegal address)	000000
Long address 1	000001 to 008000
Short address	008001 to 1E0000
Long address 3	1E0001 to 1E8000
Long address 4	1E8001 to 1F0000
Short address (reserved)	1F0001 to 1F27FF
Information service address	1F2800 to 1F67FF
Network address	1F6800 to 1F77FF
Temporary address	1F7800 to 1F780F
Operator messaging address	1F7810 to 1F781F
Short address (reserved)	1F7820 to 1F7FFE
Long address 2	1F7FFF to 1FFFFE
Idle word (illegal address)	1FFFFF

Table 31 Address word calculation

TYPE	LOWER ADDRESS CODEWORD; notes 1, 2 and 3	UPPER ADDRESS CODEWORD; notes 1, 3 and 4
Short address	CAPCODE + 8000	note 5
Long address, range 1 to 2; note 6	1 + ((CAPCODE – 1F9001) MOD 8000)	1FFFFF – ((CAPCODE – 1F9001) DIV 8000)
Long address, ranges 1 to 3 and 1 to 4	1 + ((CAPCODE – 1F9001) MOD 8000)	1D8000 + ((CAPCODE – 1F9001) DIV 8000)
Long address, range 2 to 3	1F7FFF + ((CAPCODE – 1F8FFF) MOD 8000)	1C8000 + ((CAPCODE – 1F8FFF) DIV 8000)

Notes

1. All numbers are in hexadecimal format.
2. The MOD operator gives the remainder of an integer division.
3. CAPCODE refers to the value of the address field in a FLEX™ CAPCODE.
4. The DIV operator is the integer division.
5. A short address consists of a single codeword.
6. The upper codeword range in bank 2 is used from the highest address downwards, i.e. the lowest value of the CAPCODE produces a codeword value of 1FFFFEH.

8.6.5 PHASE AND FRAME CALCULATION

The method for specifying phase and base frame of a pager is specified in the CAPCODE type.

- The phase and base frame are extracted by standard rules from the user address field in the CAPCODE (CAPCODE types A to L)
- The phase is indicated by the CAPCODE type (Table 32) and the base frame is specified in the frame field of the CAPCODE (CAPCODE types U to Z).

For easy allocation of (up to 4) consecutive CAPCODEs having the same phase and frame, an offset in the range 0 to 3 is subtracted from the user address for the purposes of phase and frame extraction. The offset is determined by the CAPCODE type.

The standard rules for extracting phase and base frame from the user address are (phase numbers 0 to 3 correspond to phases A to D):

Phase number = ((Address – Offset) DIV 4) MOD 4

Frame = ((Address – Offset) DIV 16) MOD 128

where DIV is the integer division and MOD is the remainder of an integer division.

For a CAPCODE not using the standard rules for extracting phase and base frame (types U to Z) the 3-digit frame field 000 to 127 and a single digit decimal pager collapse 0 to 5 can precede the CAPCODE type. When these fields are not included, the paging device or the subscriber database must be accessed to determine the assigned frame and collapse value.

The CAPCODE for a roaming pager uses an Alpha character to describe the level of roaming capability. The Alpha characters descriptions are shown in Table 33.

Table 32 Frame and phase extraction for different CAPCODE types

CAPCODE TYPE	PAGER TYPE	FRAME/PHASE EXTRACTION
A	single-phase	standard rules; Offset: 0
B	single-phase	standard rules; Offset: 1
C	single-phase	standard rules; Offset: 2
D	single-phase	standard rules; Offset: 3
E	any-phase	standard rules; Offset: 0
F	any-phase	standard rules; Offset: 1
G	any-phase	standard rules; Offset: 2
H	any-phase	standard rules; Offset: 3
I	all-phase; note 1	standard rules; Offset: 0
J	all-phase; note 1	standard rules; Offset: 1
K	all-phase; note 1	standard rules; Offset: 2
L	all-phase; note 1	standard rules; Offset: 3
U	single-phase	no frame extraction rules, phase-A
V	single-phase	no frame extraction rules, phase-B
W	single-phase	no frame extraction rules, phase-C
X	single-phase	no frame extraction rules, phase-D
Y	any-phase	no frame extraction rules, any-phase
Z	all-phase; note 1	no frame extraction rules, all-phase

Note

1. All-phase decoding is not defined in FLEX™ G1.8 and, therefore, is not supported by the PCD5013.

Table 33 Roaming CAPCODE character

CHARACTER	DESCRIPTION
P	non-roaming or single frequency pager
Q	no frame offset, follows the Traffic Management Flags
R	frame offset BIW101, does not follow the Traffic Management Flags
S	frame offset BIW101, follows the Traffic Management Flags

8.6.6 Configuration of user addresses (ID = 78H, 80H to 8FH)

The PCD5013 has 16 user address locations which can be programmed as network IDs or as long or short addresses, which can be configured as priority and/or tone-only. After a reset all address locations are disabled. Short addresses and network IDs occupy a single location, long addresses occupy two locations. The first word of a long address must be in an even address location and the second word must be in the address index immediately following the first word. Address location containing long addresses of the 2-3 and 2-4 set (Section 8.6.3) must follow any address locations programmed as long addresses of the 1-2, 1-3 and 1-4 set.

User addresses are programmed using the address assignment packets, and are enabled and disabled using the address enable packet. To allow easy reprogramming of user addresses without disrupting normal operation, the host can send address assignment packets while the PCD5013 is on.

In this case, the host must disable the user address location(s) by clearing the corresponding user address enable (UAE) bit in the UAE packet before changing any of the bits in the corresponding address assignment packet.

a: address location (Table 34). This specifies which address location is being configured. A zero in this field corresponds to address index zero (AI = 0) in the address packet received from the PCD5013 when an address is detected (Section 8.7.2).

LA: long address (Table 34). When this bit is set, the address is configured as a long address. Both words of a long address must have this bit set.

TOA: tone-only address (Table 34). When this bit is set, the PCD5013 considers this address a tone-only address and does not decode a vector word when the address is received. Both words of a long, tone only address must have this bit set.

A: address word (Table 34). This is the 21-bit value of the address word (A20 = MSB). Valid FLEX™ messaging addresses or Network ID's must be used. For the conversion from a CAPCODE (Section 8.6.4).

UAE: user address enable (Table 35). When a bit is set, the corresponding user address location is enabled. When it is cleared, the corresponding user address location is disabled. UAE_0 corresponds to the user address location configured using a packet ID of 80H and UAE_{15} corresponds to the user address location configured using a packet ID of 8FH. In some instances, if an invalid FLEX™ messaging address is programmed, it is not detected even when the address is enabled. Value after reset = 0.

Table 34 Address assignment packet bit assignments (ID = 80H to 8FH)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	0	0	0	a_3	a_2	a_1	a_0
2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Table 35 Address enable packet bit assignments (ID = 78H)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	0	0	0
2	0	0	0	0	0	0	0	0
1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_9	UAE_8
0	UAE_7	UAE_6	UAE_5	UAE_4	UAE_3	UAE_2	UAE_1	UAE_0

8.6.7 CONFIGURATION OF ASSIGNED FRAMES AND PAGER COLLAPSE (ID = 20H TO 27H)

The assigned frame and collapse value determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The PCD5013 must be configured explicitly to receive all required frames by setting the associated assigned frame (AF) bits. For each enabled CAPCODE these are the base frame and the associated frames implied by the pager collapse value. For example if the PCD5013 has one enabled address and it is assigned to base frame 3 with a collapse value of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99 and 115 should be set and the AF bits for all other frames should be cleared.

When the PCD5013 is configured for manual collapse mode by setting the MCM bit in the Roaming Control Packet, the PCD5013 does not apply the received system collapse to the AF bits. The host should set the AF bits for all frames that should be decoded on all channels. For example, if frames 0 and 64 should be decoded on one channel and frames 4, 36, 68, and 100 should be decoded on another channel, all six of the corresponding AF bits should be set. The host can then change the receiver's carrier frequency after the PCD5013 decodes frames 0, 36, 64, and 100.

There are 8 frame assignment packets each capable of assigning a range of 16 consecutive frame numbers.

f: frame range, see Table 38 for location in the frame assignment packet and Table 36 for the AFs and values. The value determines which 16 frames out of a range of 128 correspond to the 16 AF bits in the packet. At least one of these bits must have been set when the PCD5013 is turned on by setting the ON bit in the control packet. Value after reset = 0.

AF: assigned frame (Table 38). If a bit is set, the PCD5013 decodes the associated FLEX™ frame and scans its contents for enabled addresses. Value after reset = 0.

8.6.8 CONFIGURATION OF ASSIGNED PHASE

The assigned phase is required only for single-phase devices. It determines the phase (A, B, C, or D) in which the messages are received.

For details of phase calculation see Section 8.6.5. For details of programming the assigned phase see Section 8.4.7.

Table 36 Frame assignment ranges

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	frame 127	frame 112
0	0	1	frame 111	frame 96
0	1	0	frame 95	frame 80
0	1	1	frame 79	frame 64
1	0	0	frame 63	frame 48
1	0	1	frame 47	frame 32
1	1	0	frame 31	frame 16
1	1	1	frame 15	frame 0

8.6.9 OPERATOR MESSAGING ADDRESS ENABLE PACKET (ID = 04H)

The operator messaging address enable packet is used to enable and disable the built-in FLEX™ operator messaging addresses. Enabling and disabling operator messaging addresses does not affect on which frames the decoder IC decodes. To ensure that the correct frames are decoded, the host must modify the FF bits in the Control Packet or the AF bits in the Frame Assignment Packets.

OAE: operator messaging address enable (Table 37). When a bit is set, the corresponding operator messaging address is enabled. When it is cleared, the corresponding operator messaging address is disabled. OAE_0 to OAE_{15} corresponds to the hexadecimal operator messaging address values of 1F7810 through to 1F781F respectively. Value after reset = 0.

Table 37 Operator messaging address enable packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	1	0	0
2	0	0	0	0	0	0	0	0
1	OAE_{15}	OAE_{14}	OAE_{13}	OAE_{12}	OAE_{11}	OAE_{10}	OAE_9	OAE_8
0	OAE_7	OAE_6	OAE_5	OAE_4	OAE_3	OAE_2	OAE_1	OAE_0

Table 38 Frame assignment packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

8.7 Call data packets

8.7.1 General

The PCD5013 sends data extracted from the FLEX™ signal to the host in SPI packets using the following packet types:

- BIW packets which contain data transmitted in BIWs
- Address packets which indicate that a call has been detected and give additional information about call attributes
- Vector packets which indicate the call type and indicate which message word numbers (WN) are associated with the call
- Message packets which contain the information contained within the message codewords of a call.

For more information about the function of these packets within the FLEX™ data stream see Section 8.8.

8.7.2 Address packet (ID = 01H)

Information from address codewords in received calls is sent to the host in address packets. If less than 3-bit errors are detected in a received address word and it matches an enabled address assigned to the PCD5013, the address packet is sent to the host processor. The address packet contains the call address, the location in the data stream of the associated vector, and other miscellaneous call data.

PA: priority address (Table 39). This bit is set if the address was received as a priority address.

p: phase (Table 39). This is the phase on which the address was detected (0 = A, 1 = B, 2 = C and 3 = D).

LA: long address (Table 39). This bit is set if the address was programmed in the PCD5013 as a LA.

AI: address index (Table 39). This index identifies which address was detected. Valid values are 00H to 0FH, corresponding to the 16 programmable address words and 80H to 8FH, corresponding to the 16 temporary addresses (Section 8.8.5). Values 144 through to 159 correspond to 16 operator messaging addresses.

For long addresses, the address packet is only sent once with AI referring to the second word of the address.

TOA: tone-only address (Table 39). This bit is set if the address was programmed as a tone-only address. No vector word is sent for tone-only addresses. This bit is never set for temporary or operator messaging addresses.

WN: word number of vector (2 to 87 decimal) (Table 39). The location of the vector within this frame for the detected address. This value is invalid for this packet if the TOA bit is set.

x: unused bits (Table 39). The value of these bits is not guaranteed.

8.7.3 Vector packets (ID = 02H to 57H)

Information from vector codewords in received calls is sent to the host in vector packets. For any address packet sent to the host (except tone-only addresses), a corresponding vector packet is always sent.

The ID of the vector packet is the word number where the vector word was received in the frame. The host must associate vector packets with a call by searching for an address packet previously received on the same phase and with WN bits which match the ID of the vector packet.

The vector type of a vector packet indicates the format of a call as one of:

- Numeric (3 types)
- Short message/tone-only
- Hex/binary
- Alphanumeric
- Secure message
- Short instruction.

The numeric, hex/binary, alphanumeric, and secure message vector packets indicate the location and number of message word packets in the message field. If more than two bit errors are detected in the vector word (via BCH calculations, parity calculations, check character calculations, or value validation) the e bit is set and the message words are not sent.

Table 39 Address packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	PA	p_1	p_0	LA	x	x	x	x
1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

8.7.4 NUMERIC VECTOR PACKET

WN: word number of vector (2 to 87 decimal) (Table 40). WN describes the location of the vector word in the frame.

e: error (Table 40). Set if more than 2-bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 40). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

x: unused bits (Table 40). The value of these bits is not guaranteed.

V: vector type identifier (Table 41).

K: first check bits of the message checksum (Table 40 and Section 8.8.7).

n: number of message words in the message (Table 40), including the second vector word for long addresses, (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.

b: word number of message start in the message field (3 to 87 decimal) (Table 40). For long addresses, the word number indicates the location of the second message word.

Table 40 Numeric vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Table 41 Numeric vector definitions

V_2	V_1	V_0	TYPE	DESCRIPTION
0	1	1	standard numeric	No special formatting of characters is specified.
1	0	0	special format numeric	Formatting of the received characters is predetermined by special rules in the host (e.g. inserting spaces and dashes).
1	1	1	numbered numeric	Received information is numbered by the service provider to indicate all messages have been properly received.

8.7.5 SHORT MESSAGE/TONE-ONLY VECTOR PACKET

V: vector type identifier, these bits set to 010 for a short message/tone-only vector (Table 42).

WN: word number of vector (2 to 87 decimal) (Table 42). WN describes the location of the vector word in the frame.

e: error (Table 42). Set if more than 2-bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 42). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

t: message type (Tables 42 and 43). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 42). The value of these bits is not guaranteed.

d: data bits whose definition depends on the value of t in this packet according to Table 43. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet from the word location immediately following the vector packet. Except for the short message on a non-network address (t = 0), all messages bits in the message packet are unused and should be ignored.

Table 42 Short message/tone-only vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

Table 43 Short message/tone-only vector definitions; note 1

t_1	t_0	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	c_3	c_2	c_1	c_0	b_3	b_2	b_1	b_0	a_3	a_2	a_1	a_0	first 3 numeric characters; note 2
0	1	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	S_2	S_1	S_0	8 sources (S) and 9 unused bits (s)
1	0	s_1	s_0	R_0	N_5	N_4	N_3	N_2	N_1	N_0	S_2	S_1	S_0	8 sources (S), message retrieval flag (R), message number (N) and 2 unused bits (s)
1	1													spare message type

Notes

1. When this vector is sent in conjunction with a Network Address, the t_1,t_0 value '00' represents Network ID information. In this case the bit definitions are: T3 T2 T1 T0 M2 M1 M0 A4 A3 A2 A1 A0
   Where T are Traffic Management Flags, M represents a multiplier and A is the service area.
2. For long addresses, an extra 5 characters are sent in the message packet immediately following the vector packet. t_0 and t_1 are also set to '00' when defining the last 12 bits of a Network Address.

8.7.6 HEX/BINARY, ALPHANUMERIC AND SECURE MESSAGE VECTORS

V: vector type identifier (Table 44).

WN: word number of vector (2 to 87 decimal) (Table 45). WN describes the location of the vector word in the frame.

e: error (Table 45). Set if more than 2-bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 45). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

n: number of message words in this frame (Table 45), including the first message word that immediately follows a long address vector. Valid values are 1 to 85 decimal.

b: word number of message start in the message field (Table 45). Valid values are 3 to 87 decimal.

x: unused bits (Table 45). The value of these bits is not guaranteed.

Note that for long addresses, the first message packet is sent from the word location immediately following the word location of the vector packet. The b bits indicate the second message word in the message field if one exists.

Table 44 Non-numeric vector definitions

V_2	V_1	V_0	TYPE
0	0	0	secure
1	0	1	alphanumeric
1	1	0	hex/binary

Table 45 Hex/binary, alphanumeric and secure message vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

8.7.7 SHORT INSTRUCTION VECTOR

V: these bits are set 001 for a short instruction vector.

WN: word number of vector (2 to 87 decimal) (Table 46). WN describes the location of the vector word in the frame.

e: error (Table 46). Set if more than 2-bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 46). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: instruction type (Tables 46 and 47). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 46). The value of these bits is not guaranteed.

d: data bits whose definition depend on the value of the i bits in this packet according to Table 47. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet immediately following the vector packet. All message bits in the message packet are unused and should be ignored.

Table 46 Short instruction vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

Table 47 Short instruction vector definitions

i_2	i_1	i_0	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	0	a_3	a_2	a_1	a_0	f_6	f_5	f_4	f_3	f_2	f_1	f_0	temporary address assignment, note 1
0	0	1	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	system event; note 2
0	1	0	a_3	a_2	a_1	a_0	f_6	N_5	N_4	N_3	N_2	N_1	N_0	temporary address with message sequence number; note 2
0	1	1												reserved
1	0	0												reserved
1	0	1												reserved
1	1	0												reserved
1	1	1												reserved for test

Notes

1. Assigned temporary address index a and associated frame number f (Section 8.8.5).
2. Refer to *"FLEX™ Protocol specification G1.9".*

8.7.8 MESSAGE PACKETS (ID = 03H TO 57H)

8.7.8.1 General

The message field follows the vector field in the FLEX™ protocol. It contains the message data, checksum information, and may contain fragment and message numbers (Sections 8.8.8 and 8.8.6). If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in message packets to the host.

The ID of the message packet is the word number where the message word was received in the frame.

WN: word number of message word (3 to 87 decimal) (Table 49). WN describes the location of the message word in the frame.

e: error (Table 49). Set if more than 2-bit errors are detected in the word.

p: phase (Table 49). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: these are the information bits of the message word (Table 49). The definition of these i bits depends on the vector type and which word of the message is being received.

8.7.8.2 Numeric Message

FLEX™ numeric messages are encoded using the 4-bit BCD encoded characters sets described in Table 48. Characters are placed in codewords along with additional information about the message as described in Tables 50 and 51 and the following definitions. The 4-bit numeric characters of the message are designated as letters a, b, c, d, ... z, A, B etc.

Only codewords containing the numeric message are to be transmitted. The space character CH is used to fill any unused 4-bit characters in the last word and zeros to fill any remaining partial characters. The checksum includes only the codewords comprising the shortened message, along with the space and fill characters used to fill in the last word.

Table 48 Standard and alternate numeric character sets; Peoples Republic of China (PRC) option 'on' and 'off'

B_3	B_2	B_1	B_0	CHARACTER	
				PRC 'on'	PRC 'off'
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	spare
1	0	1	1	B	U
1	1	0	0	space	space
1	1	0	1	C	–
1	1	1	0	D	]
1	1	1	1	E	[

Table 49 Message packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

K: least significant 2 bits of 6-bit message checksum (Tables 50 and 51), most significant 4 bits are in the vector word. See Section 8.8.7 for a description of message checksums.

N: message number (Table 51). See Section 8.8.8 for a description of message numbering.

R: message retrieval flag (Table 51). When this bit is set, the pager expects this message to be numbered. See Section 8.8.8 for a description of message numbering.

S: special format, (Table 51). In the numbered message format, when this bit is set, a special display format should be used. Spaces and dashes, specified by the host, are inserted into the received message to ease reading of the message. This feature may avoid the transmission of an additional word on the channel. The actual format is undefined in FLEX™ and may be determined by the manufacturer.

Table 50 Standard (V = 011) or special format (V = 100) 4, 10, 15, 20, 25, 31, 36, or 41 characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 51 Numbered (V = 111) 2, 8, 13, 18, 23, 29, 34, or 39 numeric characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

8.7.8.3 Alphanumeric Message

FLEX™ alphanumeric messages are encoded using the 7-bit encoded alphanumeric character set defined in Table 52. Characters are placed in codewords along with additional information about the message as described in Tables 53 and 54 and the following definitions. The 7-bit characters of the message are designated lower case letters a, b, c, d, etc.

Alphanumeric messages can be sent as fragments. See Section 8.8.6 for a description of message fragmentation.

Control characters that are not acted upon by the pager are ignored in the display process (do not require display space) but are stored in memory for possible download to an external device. The ASCII character ETX (03H) should be used to fill any unused 7-bit characters in a word.

Where symbolic characters (e.g. Chinese, Kanji etc.) are being transmitted, special rules for fragment and message termination are defined in Section 8.8.6.1.

Each 7-bit field, starting with the second character of the second word in the message (first character of the second word in all remaining fragments), represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

Table 52 FLEX™ alphanumeric character set

LEAST SIGNIFICANT 4 BITS OF CHARACTER (HEX)	MOST SIGNIFICANT 3 BITS OF CHARACTER (HEX)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	“	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	’	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	TAB	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

K: 10-bit fragment checksum (Tables 53 and 54). See Section 8.8.7 for a description of message checksum.

C: 1-bit message continued flag (Tables 53 and 54). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.6 for a description of message fragmentation.

F: 2-bit message fragment number (Tables 53 and 54). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.6 for a description of message fragmentation.

N: message number (Tables 53 and 54). See Section 8.8.8 for a description of message numbering.

M: 1-bit mail drop flag (Table 53). When this bit is set, it indicates the message is to be stored in a special area in memory and is written over existing data automatically in that memory space.

R: message retrieval flag (Table 53). When this bit is set, the pager expects this message to be numbered. See Section 8.8.8 for a description of message numbering.

S: 7-bit signature field (Table 53). The signature is defined to be the 1's complement of the binary sum over the total message (all fragments). 7 bits at a time are taken (on alpha character boundary) starting with the first 7 bits directly following the signature field, $a_6a_5a_4a_3a_2a_1a_0$, $b_6b_5b_4b_3b_2b_1b_0$, etc. The 7 LSBs of the result are transmitted as the message signature.

U, V: fragmentation control bits (Table 54). This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (character made up of 1, 2 or 3 ASCII characters) are transmitted using the alphanumeric message type. The default value is 0,0. See Section 8.8.6.1 for a description of fragment control.

Table 53 Vector type V = 101 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 54 Vector type V = 101 other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.8.4 Hex/binary message

FLEX™ hexadecimal/binary messages may be encoded using any word size (blocking length) in the range 1 to 16 bits. Words are placed in codewords along with additional information about the message as described in Tables 55 and 56 and these definitions. The message data in Tables 55 and 56 have blocking lengths of 4 bits; words are designated lower case letters a, b, c, d etc.

Hexadecimal/binary messages can be sent as fragments. See Section 8.8.6 for a description of message fragmentation. Messages and message fragments are terminated, or interrupted in the case of a non-terminating fragment, on the last full character boundary in the last codeword. Unused bits are cleared if the last valid data bit is logic 1, or set if the last valid data bit is logic 0. If the terminating fragment exactly fills its last codeword, an additional codeword is sent to indicate the location of the last character. This codeword is filled with logic 0s if the last valid data bit is logic 1 and filled with logic 1s if the last valid data bit is logic 0.

Fields K to N make up the first word of a message and the first word of every fragment in a long message.

K: 12-bit fragment checksum (Tables 55 and 56). See Section 8.8.7 for a description of message checksums.

C: 1-bit message continued flag (Tables 55 and 56). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.6 for a description of message fragmentation.

F: 2-bit message fragment number (Tables 55 and 56). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.6 for a description of message fragmentation.

N: message number (Tables 55 and 56). See Section 8.8.8 for a description of message numbering.

H: 1-bit header message flag (Table 55). It is a header message only when this bit is set, otherwise it is a data message. A header message is a displayable tag associated with a non-displayable data message. The header message (which is sent first) and the data message, both have the same message number.

The second codeword of the first fragment of a hex/binary message contains fields R to S. These fields are only transmitted in the first fragment of a message.

R: message retrieval flag (Table 55). When this bit is set, the pager expects this message to be numbered. See Section 8.8.8 for a description of message numbering.

s: 5-bit field reserved for future use (Table 55). Default value = 00000.

M: 1-bit mail drop flag, see Table 55. When this bit is set, the message is to be stored in a special area in memory to overwrite existing data in the same memory space.

D: 1-bit display direction field (Table 55). D = 0 display left to right, D = 1 display right to left (valid only when data sent as characters i.e. blocking length not equal 0001).

B: 4-bit blocking length (Table 55). Indicates bits per character. $B_3B_2B_1B_0$ = 0001 = 1-bit per character (binary/transparent data), 1111 = 15 bits per character, 0000 = 16 bits per character. Data with a blocking length other than 1 is assumed to be displayed on a character by character basis (default value = 0001). Note: Tables 55 and 56 show B = 4-bit blocking length.

S: 8-bit signature field (Table 55). The 1's complement of the binary sum, taken 8 bits at a time, over the total message prior to formatting into fragments. The first 8 bits following the signature field are summed with the following 8 bits, $b_3b_2b_1b_0a_3a_2a_1a_0 + d_3d_2d_1d_0c_3c_2c_1c_0$, etc. continuing to the last valid data bit in the last word of the last fragment (the sum does not include termination bits). The 8 LSBs of the result are inverted (1's complement) and transmitted as the message signature.

8.7.8.5 Secure message

FLEX™ secure messages are encoded using the 7-bit FLEX™ alphanumeric character set (Section 8.7.8.3). These characters are placed in codewords along with additional information about the message as described in Table 57 and the following definitions. In Table 57, 7-bit characters of the message are designated lower case letters a, b, c, d etc.

Secure messages follow the same fragmentation and termination rules as alphanumeric messages (Section 8.7.8.3).

K: 10-bit fragment checksum (Table 57). See Section 8.8.7 for a description of message checksums.

C: 1-bit message continued flag (Table 57). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.6 for a description of message fragmentation.

F: 2-bit message fragment number (Table 57). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.6 for a description of message fragmentation.

N: message number (Table 57). See Section 8.8.8 for a description of message numbering.

s: spare bits (Table 57), are not used and are set to 0.

Table 55 Vector type V = 110 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 56 Vector type V = 110 all other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 57 Vector type V = 000 all fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.9 Block Information Word packet (ID = 00H)

The FLEX™ protocol allows systems to transmit time information using block information words. The information carried in a BIW depends on the BIW word format (Table 58). The first BIW of each phase, carrying information about the frame structure, is used internally by the PCD5013 and is never transmitted to the host with the exception of the system collapse which is sent to the host when the PCD5013 is in manual collapse mode.

The PCD5013 can be configured to send all time and date BIWs (BIW001, BIW010 and BIW101) to the host by setting the SBI bit in the control packet, see Section 8.4.7. All block information words 2-4 can be optionally sent to the host by setting the ABI bit in the roaming control packet. When the SBI or ABI bit is set and a BIW is received with an uncorrectable number of bit errors, the PCD5013 sends the BIW to the host indicating that the codeword was received in error (regardless of the BIW word format). The PCD5013 does not support decoding of vector and message words associated with the data/system message BIW101.

System providers supporting local time transmissions are required to transmit at least one time related BIW in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of sync 1 of frame 0 of the current cycle. See Tables 58, 59, and 60 and the following bit definitions of the time related BIWs.

e: error (Table 58). Set if more than 2-bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

p: phase (Table 58), is the phase on which the BIW was found (0 = A, 1 = B, 2 = C and 3 = D).

x: unused bits (Table 58). Their value is not guaranteed.

f: word format type (Table 58). The value of these bits modify the meaning of the s bits in this packet as described in Table 59.

s: BIW information bits (Table 58). The definition of these bits depend on the f bits in this packet.

Table 58 BIW packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	e	p_1	p_0	x	x	f_2	f_1	f_0
1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Table 59 BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	DESCRIPTION
0	0	0	i_8	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0	C_4	C_3	C_2	C_1	C_0	Local ID, Coverage Zone(1)
0	0	1	m_3	m_2	m_1	m_0	d_4	d_3	d_2	d_1	d_0	Y_4	Y_3	Y_2	Y_1	Y_0	month/day/year(2)
0	1	0	S_2	S_1	S_0	M_5	M_4	M_3	M_2	M_1	M_0	H_4	H_3	H_2	H_1	H_0	second/minute/hour(2)
0	1	1	Reserved by FLEX™ protocol for future use (1)														
1	0	0	Reserved by FLEX™ protocol for future use (1)														
1	0	1	z_9	z_8	z_7	z_6	z_5	z_4	z_3	z_2	z_1	z_0	0	1	0	X	system message; (2)
1	1	0	Reserved by FLEX™ protocol for future use (1)														
1	1	1	c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0	T_4	T_3	T_2	T_1	T_0	Country Code, Traffic Management Flags(1)

Notes

1. Decoded only if ABI bit is set.
2. Decoded only if SBI or ABI bit is set.

i: Local ID (Table 59). A Local ID along with the Coverage Zone, Country Code and Traffic Management Flags define a specific simulcast coverage area for SSID roaming.

C: Coverage Zone (Table 59). A Coverage Zone along with a Local ID, Country Code and Traffic Management Flags define a specific simulcast coverage area for SSID roaming.

m: month field (Table 59). 0001 to 1100 binary correspond to January to December in month order.

d: day field (Table 59). 00001 to 11111 binary correspond to 1 to 31 days in the month.

Y: year field (Table 59). This represents the year with modulo 32 arithmetic. 00000 to 11111 binary representing years 1994 to 2025 and 2026 to 2057.

S: seconds field (Table 59). This represents a coarse value of the seconds field. These bits represent the seconds in 1/8 minute (7.5 s) increments.
000 to 111 binary correspond to 0 to 52.5 seconds.

M: minute field (Table 59). 000000 to 111011 binary correspond to 0 to 59 minutes.

H: hour field (Table 59). 00000 to 10111 binary correspond to 0 to 23 hours.

L: daylight savings time (Table 59). When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is daylight savings time.

z: time zone (Table 59). These bits indicate the time zone for the time which is being transmitted. The offset from GMT is the offset for local standard time. Table 60 describes the values for z.

c: Country code (Table 59) identified in the CCITT (ITU-T) Standard E.212, Annex A.

T: Traffic management flags (Table 59). indicate a possible assignment of any combination of 4 groups of traffic to an RF channel. Each roaming subscriber unit, after finding an RF channel which matches its programmed Local ID, Coverage Zone and Country Code responds to only one of the 4 Traffic Management Flags. When one or more of the transmitted Traffic Management Flags are set to O, subscriber units assigned to those traffic groups must find another RF channel with the same LID, Coverage Zone and Country Code information with its assigned Traffic Flag set to 1.

Table 60 Time zone values

z_4	z_3	z_2	z_1	z_0	TIME ZONE
0	0	0	0	0	GMT
0	0	0	0	1	GMT + 01:00h
0	0	0	1	0	GMT + 02:00h
0	0	0	1	1	GMT + 03:00h
0	0	1	0	0	GMT + 04:00h
0	0	1	0	1	GMT + 05:00h
0	0	1	1	0	GMT + 06:00h
0	0	1	1	1	GMT + 07:00h
0	1	0	0	0	GMT + 08:00h
0	1	0	0	1	GMT + 09:00h
0	1	0	1	0	GMT + 10:00h
0	1	0	1	1	GMT + 11:00h
0	1	1	0	0	GMT + 12:00h
0	1	1	0	1	GMT + 03:30h
0	1	1	1	0	GMT + 04:30h
0	1	1	1	1	GMT + 05:30h

z_4	z_3	z_2	z_1	z_0	TIME ZONE
1	0	0	0	0	reserved
1	0	0	0	1	GMT + 05:45h
1	0	0	1	0	GMT + 06:30h
1	0	0	1	1	GMT + 09:30h
1	0	1	0	0	GMT – 03:30h
1	0	1	0	1	GMT – 11:00h
1	0	1	1	0	GMT – 10:00h
1	0	1	1	1	GMT – 09:00h
1	1	0	0	0	GMT – 08:00h
1	1	0	0	1	GMT – 07:00h
1	1	0	1	0	GMT – 06:00h
1	1	0	1	1	GMT – 05:00h
1	1	1	0	0	GMT – 04:00h
1	1	1	0	1	GMT – 03:00h
1	1	1	1	0	GMT – 02:00h
1	1	1	1	1	GMT – 01:00h

8.8 Message reception

8.8.1 FLEX™ SIGNAL STRUCTURE

The FLEX™ signal transmitted on the radio channel (see Fig.18) consists of a series of four minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames which are not assigned. The FLEX™ signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing or carry-on information within the FLEX™ signal.

Each FLEX™ frame has a synchronization portion followed by an eleven block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200 or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2 level FSK modulation and consists of a single phase of information at 1600 bps, phase-A. The 3200 bps rate is transmitted at either 1600 sps using 4 level FSK modulation or 3200 sps using 2 level FSK modulation and consists of two concurrent phases of information at 1600 bps, phase-A and phase-C. The 6400 bps rate is transmitted at 3200 sps using 4 level FSK modulation and consists of four concurrent phases of information at 1600 bps (phase-A, -B, -C and -D).

Each block has eight interleaved words per phase, thus there are 88 codewords (numbered 0 to 87) per phase in every frame. Each word has information contained within an error correcting code which allows for bit error correction and detection. The 88 words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field. The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of: a first sync signal at 1600 bps; a frame information word having the frame number 0 to 127 (7 bits) and the cycle number 0 to 14 (4 bits); and a second sync signal at the data rate of the interleaved portion.

The block information field contains BIWs. These can be used for determining time and date information and certain paging system information.

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. Information in the FLEX™ signal may indicate that an address is a priority address. An address may be either a short (one word) address or a long (two word) address. An address may be a tone-only address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX™ signal indicates the location of the vector word in the vector field associated with the address. A pager may perform battery saving at the end of the address field when its address(es) is not detected.

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information. Short addresses have one associated vector word in the vector field. Long addresses have one associated vector word in the vector field directly followed by the first message codeword of the call.

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD or binary depending upon the message type.

8.8.2 FLEX™ ROAMING STRUCTURE

The FLEX™ paging protocol defines two methods for supporting roaming pagers:

- Simulcast System identification (SSID) roaming, where pagers scan a pre-programmed set of channels and identify each simulcast area which is to be included in the desired roaming area
- Network identification (NID) roaming where pagers examine all frequencies within the subscriber units's range for the presence of a marker (NID). The NID indicates whether the channel is affiliated with the desired roaming network.

A Simulcast System Identifier (SSID) is carried in the Block Identification Field. A SSID is composed of a Local Identifier (LID), a Coverage Zone, a Country Code and Traffic Management Flags. These components define a simulcast area which is unique worldwide. An LID is unique within a Country Code and cannot be reassigned to another operator in any paging RF band.

A Network Identifier (NID) is carried in the address and vector fields. NIDs are unique within an RF band and are composed of a Network Address, a Service Area Identifier, a Multiplier and Traffic Management Flags. An RF channel may combine roaming traffic from several different Service Providers by carrying their respective NIDs.

NIDs and SSIDs are referred to as Roaming IDs.
In addition pagers may be programmed to search for calls on a channel without finding an SSID or an NID in order to receive calls on that RF channel. In this case the Roaming ID associated with the channel is programmed within the pager as having ANY ID.

8.8.2.1 Example Roaming System

Figure 17 shows six RF frequencies servicing three cities. NID1 is used to identify a network covering all three cities and SSIDs A, B and C identify the specific simulcast areas covering cities A, B and C. In city C, the large amount of traffic has resulted in the service provider activating additional RF channels identified as a, b, d, e and f. In this example, the pager is assigned Roaming IDs as follows:

$SSID_C$

NID_1

traffic management group 2 (0100)

Thus the pager will monitor frequencies as follows:

f_b when in the area of city A

f_c when in the area of city B

f_d when in the area of city C.

For further information on FLEX™ Roaming, see the *"FLEX™ specification G1.9"*.

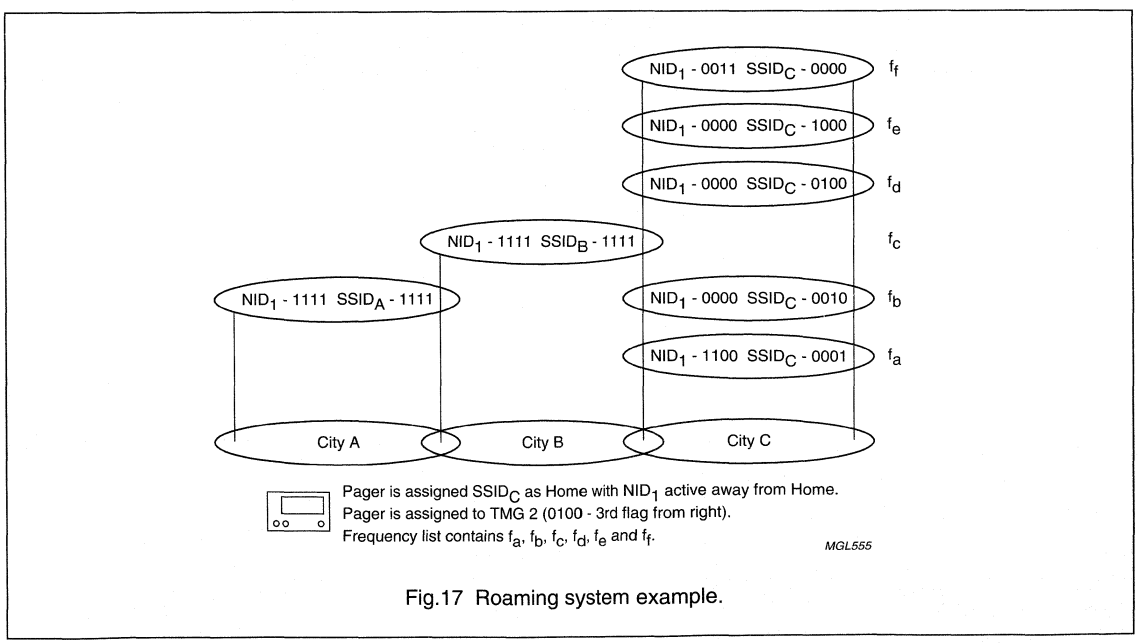


Fig.17 Roaming system example.

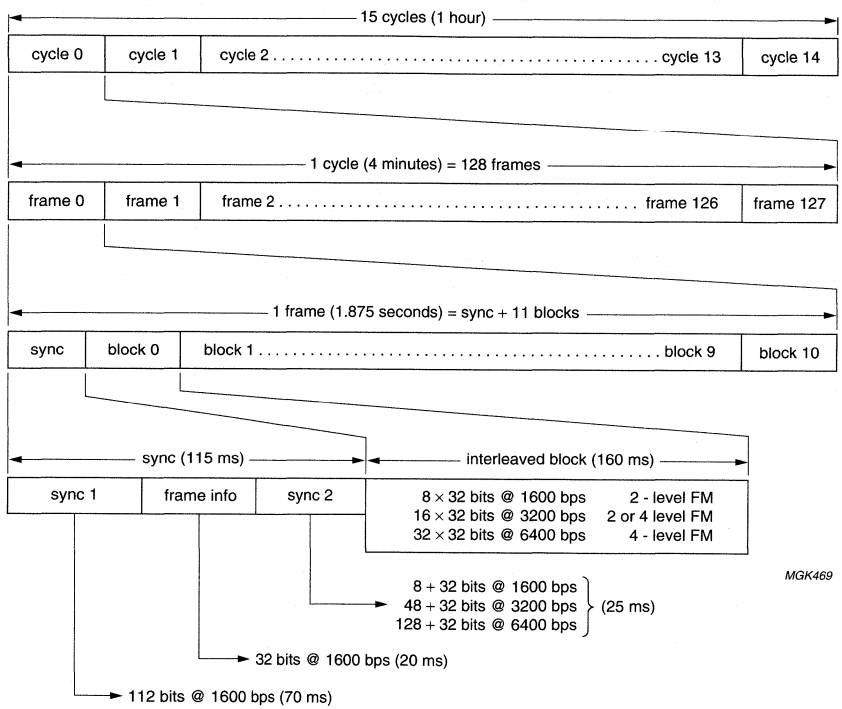


Fig.18 FLEX™ signal structure.

8.8.3 MESSAGE BUILDING

The PCD5013 sends data from the FLEX™ signal to the host in packets. Data is transmitted one block at a time, and one phase at a time. For a 2 phase transmission, information in block 0 phase-A is converted into packets and sent to the host, then information in block 0 phase-C is sent to the host followed by information in block 1 phase-A and then information in block 1 phase-C etc. Codewords for different calls may therefore be interleaved, so the host must use the phase and word number embedded in each packet to associate that packet with a particular call.

The phase and word number of the vector packet provides a unique key which allows the host to associate all the data for a particular call within a frame. The host must then use information embedded in the vector word to calculate what message word locations are associated with the vector.

Table 61 FLEX™ transmission sequence

BLOCK	WORD	PHASE-A	PHASE-C
0	0	BIW1; note 1	BIW1; note 1
	1	addr; note 2	BIW
	2	addr; note 2	BIW
	3	$addr_1$	addr; note 2
	4	$addr_2$	addr; note 2
	5	vect; note 2	long $addr_3$ (cw 1)
	6	vect; note 2	long $addr_3$ (cw 2)
	7	$vect_1$	addr; note 2
1	8	$vect_2$	vect; note 2
	9	$mess_1$ (cw 1)	vect; note 2
	10	$mess_1$ (cw 2)	$vect_3$; note 3
	11	$mess_1$ (cw 3)	$mess_3$ (cw 1); note 4
	12	$mess_2$ (cw 1)	mess; note 2
	13	$mess_2$ (cw 2)	mess; note 2
	14	$mess_2$ (cw 3)	$mess_3$ (cw 2)
	15	$mess_2$ (cw 4)	$mess_3$ (cw 3)

Notes

1. Phases begin with BIW1, which is not sent to the host.
2. Codewords not addressed to the pager.
3. Vector for long address indicates the location of the second and third message words.
4. For long addresses, the first message word immediately follows the vector.

Tables 61 and 62 show an example of receiving three messages (possibly portions of fragmented or group messages), and two BIW packets in the first two blocks of a 2 phase 3200 bps FLEX™ frame in case of an any-phase pager. Table 61 shows the block number, word number and word content of both phase-A and phase-C (subscripts indicate the call number). In a 6400 bps FLEX™ frame, there would be four phases: A, B, C and D; in a 1600 bps signal there would be only phase-A. Table 62 shows the sequence of packets transmitted to the host.

Table 62 PCD5013 packet sequence

PACKET	PHASE	PACKET TYPE	WORD NO.	COMMENT
1	A	address	7	note 1
2	A	address	8	note 1
3	A	vector	7	pointer to phase-A word 9
4	C	BIW	n.a.	note 2
5	C	BIW	n.a.	note 2
6	C	long address	10	note 1
7	A	vector	8	pointer to phase-A word 12
8	A	message	9	$mess_1$ (cw 1)
9	A	message	10	$mess_1$ (cw 2)
10	A	message	11	$mess_1$ (cw 3)
11	A	message	12	$mess_2$ (cw 1)
12	A	message	13	$mess_2$ (cw 2)
13	A	message	14	$mess_2$ (cw 3)
14	A	message	15	$mess_2$ (cw 4)
15	C	vector	10	pointer to phase-A word 14
16	C	message	11	$mess_3$ (cw 1)
17	C	message	14	$mess_3$ (cw 2)
18	C	message	15	$mess_3$ (cw 3)

Notes

1. Word number in an address is that of the corresponding vector.
2. BIW sent if BIW reception enabled by SBI bit in the control packet.

8.8.4 ALL FRAME MODE (ID = 03H)

The FLEX™ protocol requires pagers to be capable of receiving data in frames other than pagers' programmed frames and frames implied by collapse values. This is achieved in the PCD5013 by all frame mode (AFM) which is required to implement the following features:

- Fragmented messages (Section 8.8.6)
- Temporary addresses (Section 8.8.5).

The PCD5013 enters AFM automatically and when in AFM, it decodes every FLEX™ frame irrespective of whether it is a programmed frame. In AFM the PCD5013 sends a status packet with the end-of-frame (EOF) bit set at the end of every frame. In addition the host can force AFM by sending an AFM packet with the force all frame mode (FAF) bit set.

The PCD5013 contains a number of counters which are used to track the number of active calls requiring AFM. These consist of an AFM counter for tracking the number of active fragmented messages and 16 temporary address enable (TAE) counters which count the number of times each temporary address has been enabled. These counters are automatically incremented when a corresponding vector is received, i.e.:

- A short instruction vector indicating a temporary address has been assigned to this pager
- A vector indicating a message for this pager with a format which allows fragmentation.

The host must determine when no further data can be received for a message associated with a temporary address, or a fragmented message, and send an AFM packet, see Table 63, to decrement the appropriate counter.

AFM remains active until the host determines that no further data can be sent to it outside programmed frames, i.e:

- The TAE counters are all zero indicating that no further temporary message data is expected
- The AFM counter is zero indicating that no further data is expected for fragmented messages
- The FAF bit is clear.

Both the AFM counter and the TAE counters can only be incremented internally by the PCD5013 and can only be decremented by the host via AFM packet. Neither the TAE counters nor the AFM counter can be incremented past the value 127 (it does not roll-over) or decremented past the value 0. The TAE counters and the AFM counter are cleared on a reset and when the decoder is turned off.

DAF: decrement all frame mode counter, see Table 63. Setting this bit decrements the AFM counter by one. If a packet is sent with this bit clear, the AFM counter is not affected. Value after reset = 0.

FAF: force all frame mode, see Table 63. Setting this bit forces the PCD5013 to enter AFM. If this bit is clear, the PCD5013 may or may not be in AFM depending on the status of the AFM counter and the TAE counters. This functionality may be useful in acquiring transmitted time information. Value after reset = 0.

DTA: decrement temporary address enable counter, see Table 63. When a bit in this word is set, the corresponding TAE counter is decremented by one. When a bit is clear, the corresponding TAE counter is not affected. When a TAE counter reaches zero, the temporary address is disabled. Value after reset = 0.

Table 63 All frame mode packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	1
2	DAF	FAF	0	0	0	0	0	0
1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_9	DTA_8
0	DTA_7	DTA_6	DTA_5	DTA_4	DTA_3	DTA_2	DTA_1	DTA_0

8.8.5 TEMPORARY ADDRESSES

FLEX™ allows dynamic group calls in which a common message is sent to a group of paging devices. This is achieved by assigning the same temporary address (TA) to each pager in the group using the pagers' personal addresses and the short instruction vector. The short instruction vector causes the TA to be active in the next occurrence of a specific frame (if the designated frame is equal to the present frame the host is to interpret this as the next occurrence of this frame in the following cycle).

FLEX™ specifies sixteen TAs which remain valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. The FLEX™ protocol restricts the placement of TAs such that once assigned to a specific frame they cannot occur in the FLEX™ transmission before that frame.

The PCD5013 uses AFM (Section 8.8.4) to allow the reception of TAs outside programmed frames.
The sequence for the host and the PCD5013 to operate a TA is:

1. The PCD5013 receives an address codeword followed by a vector codeword with $V_2V_1V_0 = 001$ and $I_2I_1I_0 = 000$ indicating a short instruction vector which assigns a TA to this pager.
2. The PCD5013 passes the address and vector codeword to the host as packets and increments the corresponding TA counter and enters AFM.
3. The host examines the vector packet to identify which TA is assigned and the frame in which the TA is expected.
4. The PCD5013 continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
5. The host processes data packets received while the PCD5013 is in AFM. It uses the AFM packet to decrement the appropriate TA counter when no further data can be expected for the corresponding TA. This occurs when:
   a) The TA is not found in the assigned frame.
   b) The TA is found in the frame it was assigned and was not a fragmented message.
   c) The TA is found in the assigned frame was a fragmented message and the rules for message fragmentation (Section 8.8.6) indicate that no further data can be expected. In this case the host must send an AFM packet with both the DAF and the appropriate DTA bits set in order to terminate both the fragmented message and the TA.
6. The above operation is repeated for every enabled TA.

8.8.6 MESSAGE FRAGMENTATION

The FLEX™ frame length limits the maximum number of message codewords that can be associated with an address codeword. Messages longer than 84 codewords must be sent as several fragments. The PCD5013 uses AFM (Section 8.8.4) to allow the reception of fragmented messages.

The fragments of a message are sent in sequence. Each fragment contains a checksum character to detect errors in the fragment, a message number to identify which message the fragment is a part, and the continue bit which either indicates that more fragments are in queue or that the last fragment has been received. Each fragment also contains a fragment number starting with 3 for the first fragment and then incremented through the sequence 0, 1 or 2 in subsequent fragments. This allows the detection of missing fragments.

Message fragments may not be separated by more than 32 frames (1 minute) or 128 frames (4 minutes), as indicated by the service provider. During the reception of a fragmented message, the PCD5013 examines every frame for additional fragments until the last fragment is encountered or the host determines that more than 32 or 128 frames have elapsed since the reception of the previous message fragment.

The sequence for the host and the PCD5013 to receive a fragmented message is as follows:

1. The PCD5013 receives an address codeword followed by a vector indicating one of:
   a) Secure (vector type = 000)
   b) Alphanumeric (vector type = 101)
   c) Hexadecimal/binary (vector type = 110).

   The PCD5013 passes the address, vector and message codewords to the host as packets and increments its internal AFM counter and enters AFM.
2. While in AFM, the PCD5013 decodes all of the frames passing any address, vector and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
3. Every time the host receives a secure, alphanumeric or hexadecimal/binary vector packet, it inspects the message continued flag (C) in the first message packet:
   a) If this is not a fragmented message (C is clear and no fragmented messages are in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5013 with the DAF bit set. If the fragmented message was received on a temporary address, then the appropriate DTA bit should also be set in the AFM packet.
   b) If this is the first fragment of a fragmented message (C is set and no fragmented messages are in progress for this address and message number), then the host does not decrement the AFM counter and expects further fragments to be received for this address in subsequent frames.
   c) If this is the second or subsequent fragment of a fragmented message and further fragments will follow, (C is set and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5013 with the DAF bit set.
   d) If this is the last fragment of a fragmented message, (C is clear and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by 2, sending 2 AFM packets to the PCD5013 with the DAF bit set. If the fragmented message was received on a TA, then one of these AFM packets should also have the appropriate DTA bit set.
4. If, on receiving a status packet, the host determines that more than 32 or 128 frames have elapsed since the reception of a fragment for a fragmented message then the host decrements the AFM counter by sending an AFM packet to the PCD5013 with the DAF bit set. If the fragmented message was received on a TA, then the appropriate DTA bit should also be set in the AFM packet.
5. When no fragmented messages are in progress (the AFM counter = 0) and no TAs are pending (all TA counters = 0) and the FAF bit is clear in the AFM packet, the PCD5013 leaves AFM.

As an alternative to the above scheme, the host may choose to decrement the AFM counter at the end of the entire message by decrementing it once for each fragment received. This method is limited to a maximum of 127 fragments.

Tables 64 and 65 show examples of message reception with and without message fragmentation.

Table 64 Alphanumeric message without fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 0; no more fragments are expected
4th	AFM		0	host writes AFM packet to the PCD5013 with the DAF bit = 1

Table 65 Alphanumeric message with fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 1; message is fragmented, more expected
4th	status		1	end of frame indication (EOF = 1)
5th	address 1	B	1	address 1 is received
6th	vector 1	B	2	vector = alphanumeric type
7th	message	B	2	message word received; C bit = 1; message is fragmented, more expected
8th	AFM		1	host writes AFM packet to the PCD5013 with the DAF bit = 1
9th	status		1	end of frame indication (EOF = 1)
10th	address 1	A	1	address 1 is received
11th	vector 1	A	2	vector = alphanumeric type
12th	message	A	2	message word received; C bit = 0; no more fragments are expected
13th	AFM		1	host writes AFM packet to the PCD5013 with the DAF bit = 1
14th	AFM		0	host writes AFM packet to the PCD5013 with the DAF bit = 1

8.8.6.1 Fragmentation of non-7-bit character sets

FLEX™ alphanumeric messages can be used to send symbolic characters like Chinese, Kanji, etc. In this case several ASCII characters are used to represent each symbolic character. Enhanced fragmentation (EF) rules are provided by FLEX™ to allow character positions within a fragment to be determined in the event of missing fragments under poor signal conditions.

1. The pager must remove <NUL> characters from the end of fragments (where they are used as fill characters) so that the displayed message is not affected. To determine character boundaries, <NUL> (00H) characters in all other positions must be considered a result of channel errors. This allows each fragment to end with a complete character and does not disrupt pagers which do not follow all the EF rules.
2. The last fragment of a message containing symbolic characters is completed by filling unused character positions with <ETX> (03H) characters or <NUL> characters. When a message ends at exactly the last character position of the last BCH codeword, no additional <ETX> is required.
3. The U and V bits (Table 54) which aid decoding, are available in all fragments following the initial fragment. In the first fragment the message starts in the default character mode (U and V = 10). For subsequent fragments the definition of the U and V field is as shown in Table 66. When the U and V field is 00, characters may be split between fragments. When the U and V field is not 00, each fragment starts on a character boundary with the character mode defined as in Table 66.

8.8.7 MESSAGE CHECKSUMS

FLEX™ provides a message checksum facility for alphanumeric, numeric, hex/binary, and secure messages. The checksum is calculated by summing the information bits of each codeword in the message or message fragment (including control information and termination characters and bits in the last message codeword). Information bits of each codeword are broken into three groups as indicated in Table 67. Bits i_0, i_8 and i_{16} are the LSBs of each group and bit i_0 is the first bit of the codeword to be transmitted. The 3 groups are for each codeword are added to form a binary sum. The message checksum is the 1's complement of the LSBs of the binary sum, where the number of bits taken is determined by the message type (Section 8.7.8).

In the case of the 6-bit message checksum used in numeric messages, a binary sum is first calculated as described above. The binary sum is then truncated to its 8 LSBs, then the 2 MSBs are shifted right by 6 bits and added to the least significant 6 bits to form a new binary sum. The 6 LSBs of this new sum are taken and 1's complemented to form the 6-bit message checksum.

8.8.8 MESSAGE NUMBERING

FLEX™ messages may be numbered (Section 8.7.8), in this case the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in numerical order. The maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. When a message number is missed, the subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval.

Messages which can be received out of sequence are indicated by clearing the message retrieval flag R. Messages with R cleared number should not be included in the missed message calculation.

In case of fragmented messages, this number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

Table 66 Fragmentation control bit definitions

U_0	V_0	DEFINITION
0	0	EF not supported in controller
0	1	reserved (for a second alternate character mode)
1	0	default character mode start position 1
1	1	alternate character mode start position 1

Table 67 Bit groups for message checksums

i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
group 1								group 2								group 3				

8.8.9 Using the Receiver Shutdown Packet

8.8.9.1 Operation of Roaming features

A roaming pager scans channels in a frequency list to determine the channel or channels to monitor. The pager matches the Roaming IDs (SSIDs, NIDs or any IDs) transmitted on monitored channels against those contained in the pager's Roaming ID list. Each item in the Roaming ID list is assigned a priority to ensure determinative behaviour for roaming pagers.

Implementation of a Roaming Pager using the PCD5013 is greatly simplified using the FLEX™ software.

Items in the Roaming ID list are assigned priorities to arbitrate in the case where a pager is in a coverage in which there is more than one RF channel. In the case that a pager receives data from two channels both of Roaming Identifiers of the highest priority, it can enter one of two modes of operation (as determined by the pager programming).

Channel scanning is done to determine whether to switch channel because there is a channel of higher priority than the currently monitored channel.

- Global scanning: the scan of all RF channels after switch on. Once the global scan is completed, the pager starts to monitor all channels with a programmed priority which is equal to or higher than the highest priority channel on which a FLEX™ transmission was encountered. If no FLEX™ transmission is encountered the pager must restart the global scan after some battery saving period.
- Background scanning: scanning done to determine whether the pager one of the monitored RF channels carries a FLEX™ signal with higher priority than the currently monitored channel.

This can occur either because the pager has entered a new area or because the Roaming IDs or Traffic Management Flags change.

A pager can stop monitoring a channel either because the channel's Roaming ID changes or because no signal has been encountered on the channel for a given period. When all the monitored channels have been lost, the pager must start a global scan.

The PCD5013 sends information to the host in the Receiver Shutdown Packet (see Section 8.4.12) every time it shuts the receiver down. This allows the host to calculate whether it will have enough time to switch frequencies before the receiver next switches on (see Section 8.8.9.2).

The PCD5013 allows the identification of Roaming IDs by the support for the reception of SSID Block Information words and Short Messaging Vectors (see Sections 8.7.5 and 8.7.9)

8.8.9.2 Calculating time left

The receiver shutdown packet gives timing information to the host. Two times are of particular interest when implementing a roaming algorithm.

TimeToWarmUpStart: Defined as the amount of time there is before the receiver starts to warm-up (i.e. transition from the off state to the first warm-up state).

TimeToTasksDisabled: Defined as the amount of time the host has to complete any host initiated tasks (e.g. by setting SND or SAS in the roaming control packet).

The formulae for calculating these times are shown below and depend on whether the PCD5013 is in Synchronous mode or Asynchronous mode.

Synchronous mode:

$$\text{TimeToWarmupStart} \geq (\text{TNF} \times 80\ \text{ms}) + (\text{SkippedFrames} \times 1874.375\ \text{ms}) + (\text{ReceiverOffTime} - 167.5\ \text{ms})$$

$$\text{TimeToTasksDisabled} \geq (\text{TNF} \times 80\ \text{ms}) + (\text{SkippedFrames} \times 1874.375\ \text{ms}) + (\text{ReceiverOffTime} - 247.5\ \text{ms})$$

Asynchronous mode:

$$\text{TimeToWarmupStart} \geq [(\text{TNF} - 2) \times 80\ \text{ms}] + \text{ReceiverOffTime}$$

$$\text{TimeToTasksDisabled} \geq [(\text{TNF} - 3) \times 80\ \text{ms}]$$

Where:

TNF (Time to Next Frame): value from the receiver shutdown packet. SkippedFrames: the number of frames that will not be decoded. Calculated from the Current Frame (CF) and Next Needed Frame (NAF) fields in the receiver shutdown packet (e.g. if CF is 10 and NAF is 12, then SkippedFrames is 1). ReceiverOffTime: the time programmed in the receiver off setting packet.

8.8.9.3 Calculating how long tasks take

Since the TimeToTaskDisabled discussed in the previous section limits how much the host can do while the PCD5013 is battery saving, it is necessary for the host to know how long it can take the PCD5013 to perform a task.

The formulae below calculate how long the two types of host initiated tasks take to complete as measured from the last SPI clock of the packet that initiates the task to the time the receiver shutdown sequence starts. Note that the receiver shutdown sequence must start before tasks are disabled.The following definitions are used:

TotalWarmUpTime: The sum of the times programmed for the used warm-up steps plus the time programmed for the 3200 sps Sync Setting in the receiver control configuration packets

AST: The value configured using the timing control packet.

Equation (1) calculates how long it takes to complete a Noise Detect started by setting the SND bit in the roaming control packet. This formula assumes that:

- the noise detect was performed while in synchronous mode OR
- the noise detect was performed in asynchronous mode and did not find FLEX™ signal OR
- the noise detect found FLEX™ signal but the DAS bit of the roaming control packet was set.

Equation (2) calculates how long it will take to complete an A-word search initiated by setting the SAS bit in the roaming control packet. This formula assumes that the A-word search failed to find roaming FLEX™ channel.

Equation (3) calculates how long it will take to complete a Noise Detect/A-word search combination. This can occur when the noise detect is performed while in asynchronous mode, the noise detect finds FLEX™ signal, and the DAS bit of the roaming control packet is not set.

$$\text{TimeToPerformNoiseDetect} \leq \text{TotalWarmUpTime} + 82\ \text{ms} \quad (1)$$

$$\text{TimeToPerformAwordSearch} \leq \text{TotalWarmupTime} + \text{AST} + 47\ \text{ms} \quad (2)$$

$$\text{TimeToPerformBoth} \leq \text{TotalWarmUpTime} + \text{AST} + 127\ \text{ms} \quad (3)$$

9 LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	−0.5	4.0	V
I_{DD}	supply current		−	50	mA
I_I	DC input current (any input)		−10	+10	mA
I_O	DC output current (any output)		−10	+10	mA
V_I	input voltages (all inputs)	note 2	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		−	300	mW
P_O	power dissipation per output		−	10	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−65	+150	°C

Notes

1. V_{DD1} and V_{DD2} respectively and V_{SS1} and V_{SS2} must be connected at the same potential.
2. $V_{I(max)}$ = 4.0 V.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	90	K/W

12 DC CHARACTERISTICS

T_{amb} = −25 to +70 °C; V_{DD} = 2.2 V; f = 76.8 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	2.2	3.6	V
$I_{DD(stby)}$	standby supply current	on = 0; note 1	–	4.9	24	μA
I_{DD}	operating supply current	on = 1; note 2	–	6.0	–	μA
Digital inputs: OSCPD, TEST2, TEST3, $\overline{\text{RESET}}$, LOBAT, EXTS0, EXTS1, $\overline{\text{SS}}$ and MOSI						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_{LI}	LOW/HIGH-level input leakage current		–	–	1	μA
Digital outputs: MISO, $\overline{\text{READY}}$, CLKOUT, SYMCLK and S0 to S7						
V_{OL}	LOW-level output voltage	I_{sink} = 0.8 mA	–	0.1	0.4	V
V_{OH}	HIGH-level output voltage	I_{source} = −0.8 mA	V_{DD} − 0.4	V_{DD} − 0.1	–	V
I_{LO}	LOW/HIGH-level output leakage current	3-state outputs	–	–	1	μA

Notes

1. External clock signal (frequency = 76.8 kHz, amplitude = V_{SS} to V_{DD}) at pin EXTAL; OSCPD = HIGH; test inputs = LOW; other inputs = HIGH; outputs unconnected; SPI transmit enabled; COD bit set to logic 1 (see Section 8.4.4); to obtain the supply current of an application with a crystal connected as in Fig.19, a typical oscillator current of 2 μA needs to be added to this value (see Chapter 14); T_{amb} = 25 °C.
2. As note 1, but PCD5013 and synchronous to a typical FLEX™ data stream (collapse value = 4), T_{amb} = 25 °C.

13 AC CHARACTERISTICS

T_{amb} = −25 to +70 °C, V_{DD} = 1.8 to 3.6 V, f_{EXTAL} = 76.8 kHz, maximum load capacitance = 50 pF connected to any digital output; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset timing						
$t_{W(rst)}$	$\overline{\text{RESET}}$ pulse width		200	–	–	ns
$t_{LH(RESET-READY)}$	$\overline{\text{RESET}}$ LOW to $\overline{\text{READY}}$ HIGH		–	–	200	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	stable 76.8 kHz clock	–	1	–	s
Start-up timing						
$t_{strt(osc)}$	oscillator start-up time	see Fig.19	–	0.5	–	s
$t_{h(rst)}$	$\overline{\text{RESET}}$ hold time		200	–	–	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	note 1	–	76800	–	T
$t_{WUL(osc-READY)}$	oscillator warmed up to $\overline{\text{READY}}$ LOW	note 1	–	76800	–	T
SPI timing						
f_{SCK}	operating frequency		0	–	1	MHz
$T_{cy(SCK)}$	cycle time		1000	–	–	ns
t_{LEAD1}	select lead time		200	–	–	ns
t_{LAG1}	de-select lag time		200	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(SS\text{-}READY)}$	$\overline{SS}$-to-$\overline{READY}$ delay time	previous packet did not program an address word; note 2	–	–	80	µs
		previous packet programmed an address word; note 2	–	–	420	µs
t_{READYH}	$\overline{READY}$ HIGH time		50	–	–	µs
t_{LEAD2}	$\overline{READY}$ lead time		200	–	–	ns
t_{LAG2}	$\overline{READY}$ lag time		–	–	200	ns
$t_{su(i)(D)}$	MOSI data setup time		200	–	–	ns
$t_{h(i)(D)}$	MOSI data hold time		200	–	–	ns
$t_{ACC(o)}$	MISO access time		0	–	200	ns
$t_{o(dis)}$	MISO disable time		–	–	300	ns
t_{DOV}	MISO data valid time		–	–	200	ns
$t_{h(o)(D)}$	MISO data hold time		0	–	–	ns
t_{SSH}	$\overline{SS}$ HIGH time		200	–	–	ns
t_{SCKH}	SCK HIGH time		300	–	–	ns
t_{SCKL}	SCK LOW time		200	–	–	ns
t_r	SCK rise time	10% to 90% V_{DD}	–	–	1	µs
t_f	SCK fall time	10% to 90% V_{DD}	–	–	1	µs

Notes

1. T is one period of the clock source either generated by the internal oscillator, or applied at the input EXTAL. Note that from power-up, the oscillator start-up time can influence the availability and period of clock strobes. This can affect the $\overline{RESET}$ HIGH to $\overline{READY}$ LOW timing.
2. When the host re-programs an address word with a host-to-decoder packet ID > 7FH, there is an added delay before the PCD5013 is ready for another packet.

14 OSCILLATOR CHARACTERISTICS

T_{amb} = –25 to +70 °C; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_1	external capacitor at pin EXTAL	note 1	–	15	–	pF
C_2	external capacitor at pin XTAL	note 1	–	15	–	pF
R_f	external feedback resistor	note 1	–	10	–	MΩ
$g_{m(osc)}$	oscillator transconductance		9.4	27	70	µS
I_{osc}	oscillator operating supply current	V_{DD} = 2.2 V; note 2	–	2	–	µA

Notes

1. Designed for quartz crystal type: SEIKO VTC200 or equivalent; parameters: f = 76800Hz, R_S = 35 kΩ (max.), $C_L = C_1.C_2/(C_1 + C_2) + C_{stray}$ = 8 to 12 pF, C_0 = crystal shunt capacitance = 0.8 pF (typ.), C_f = typical parasitic pin capacitance = 2 pF; maximum overall frequency tolerance (including transmitter) is 300 ppm (Section 8.4.4).
2. Extracted from evaluations under conditions as in Fig.19; this value is strongly dependent on external conditions (load and parasitic capacitances).

15 TEST AND APPLICATION INFORMATION

15.1 FLEX™ protocol

The PCD5013 conveys a licence to manufacture Pagers using the *"FLEX™ Total Messaging Solution"* agreement. For the terms and conditions of this agreement please contact Philips Semiconductors.

Further details of the FLEX™ protocol are contained in the document *"FLEX™ Protocol and FLEX™ Encoding and Decoding Requirements"*.

Please note that the issuing of this document is not part of the *"FLEX™ Total Messaging Solution"* agreement. Enquiries about the FLEX™ protocol not covered by the *"FLEX™ Total Messaging Solution"* should be directed to:

Motorola Inc.
FLEX™ Licensing Manager,
Mail Stop 99,
1500 Gateway Boulevard,
Boynton Beach,
Florida 33426.
FAX: (561) 739-2519
Telephone: (561) 739-8281.

15.2 Example applications

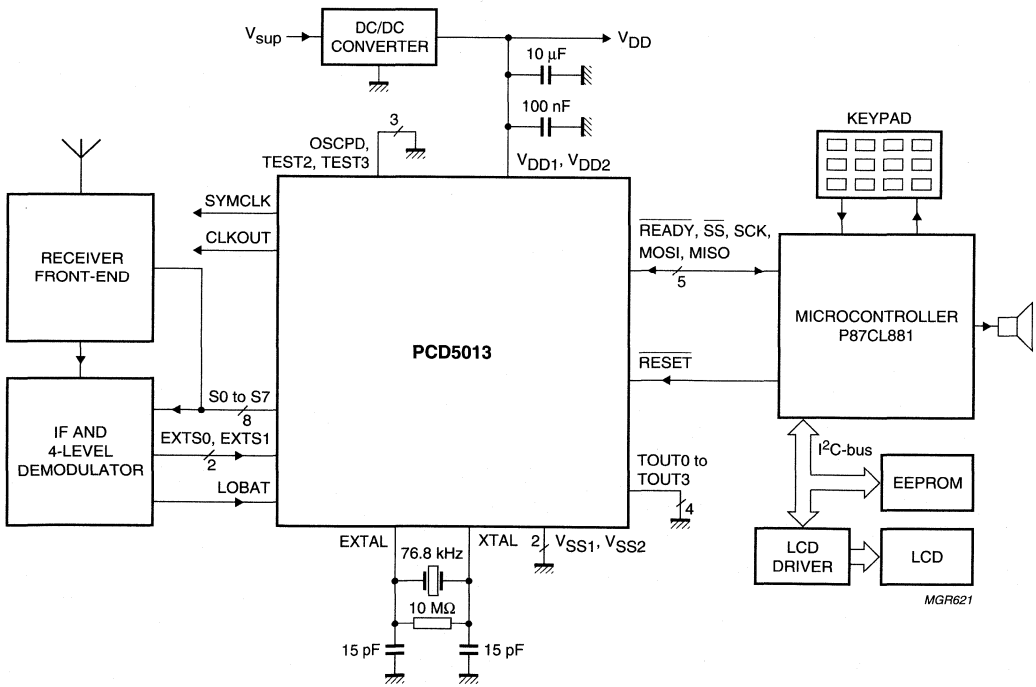


Fig.19 Example application using external demodulation.

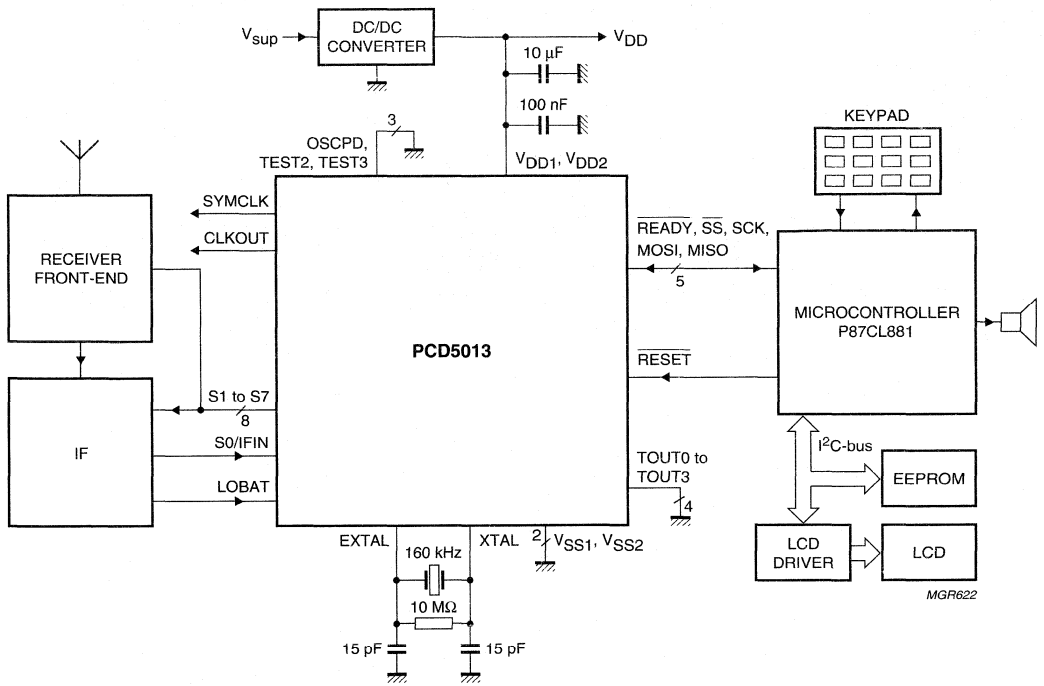


Fig.20 Example application using internal demodulator.

15.3 System block diagram

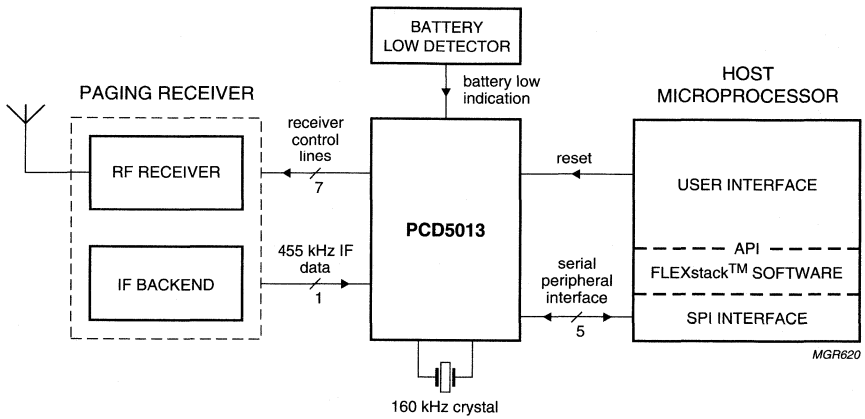


Fig.21 System block diagram.

CONTENTS

1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 and LQFP100 packages
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- Volume control
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Two tone (DTMF) generators
- Automatic gain control
- Hands-free operation

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5091 is designed for GAP-compliant handsets with speaker-phone option. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5091H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2
PCD5091HZ	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4 BLOCK DIAGRAM

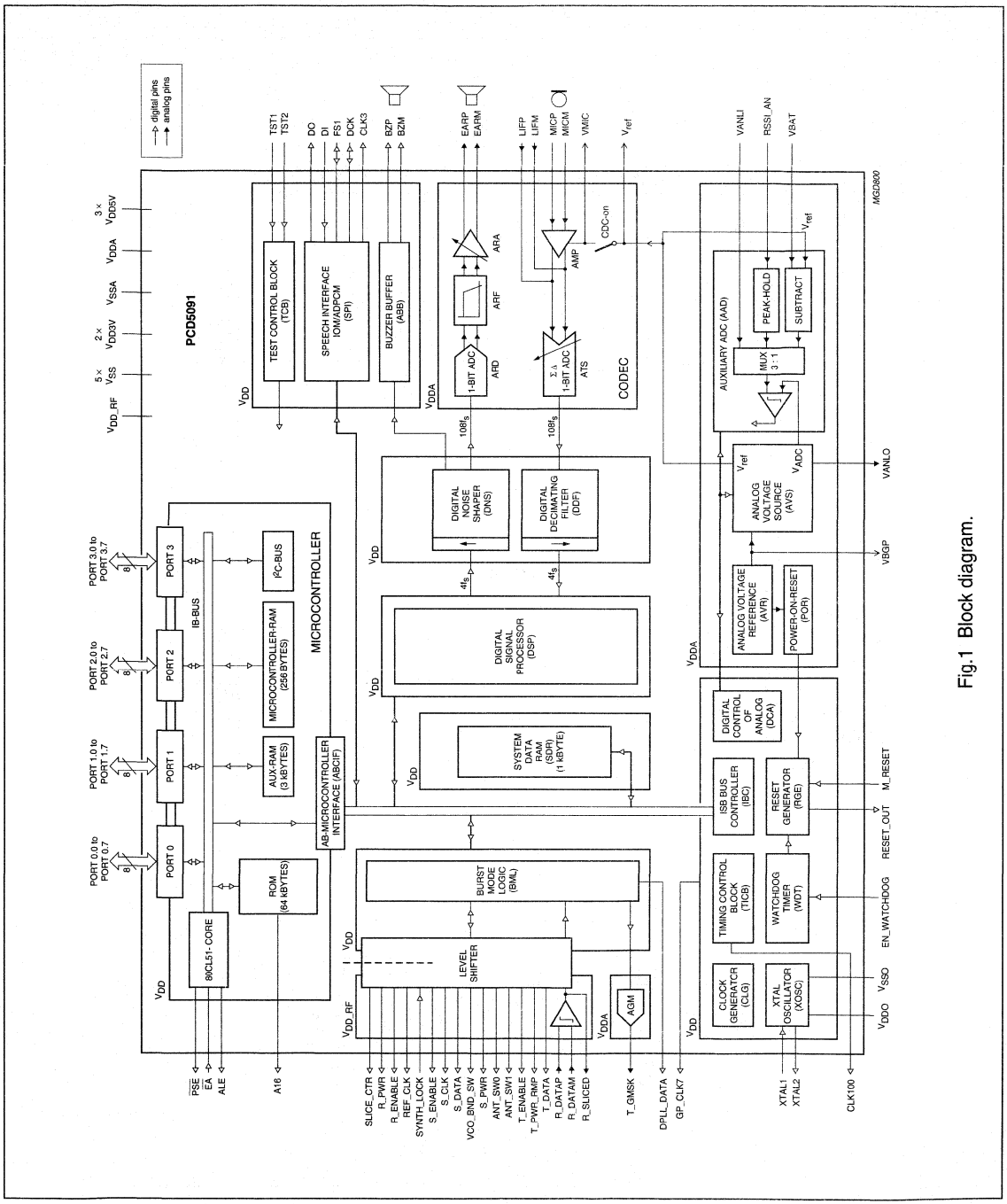


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

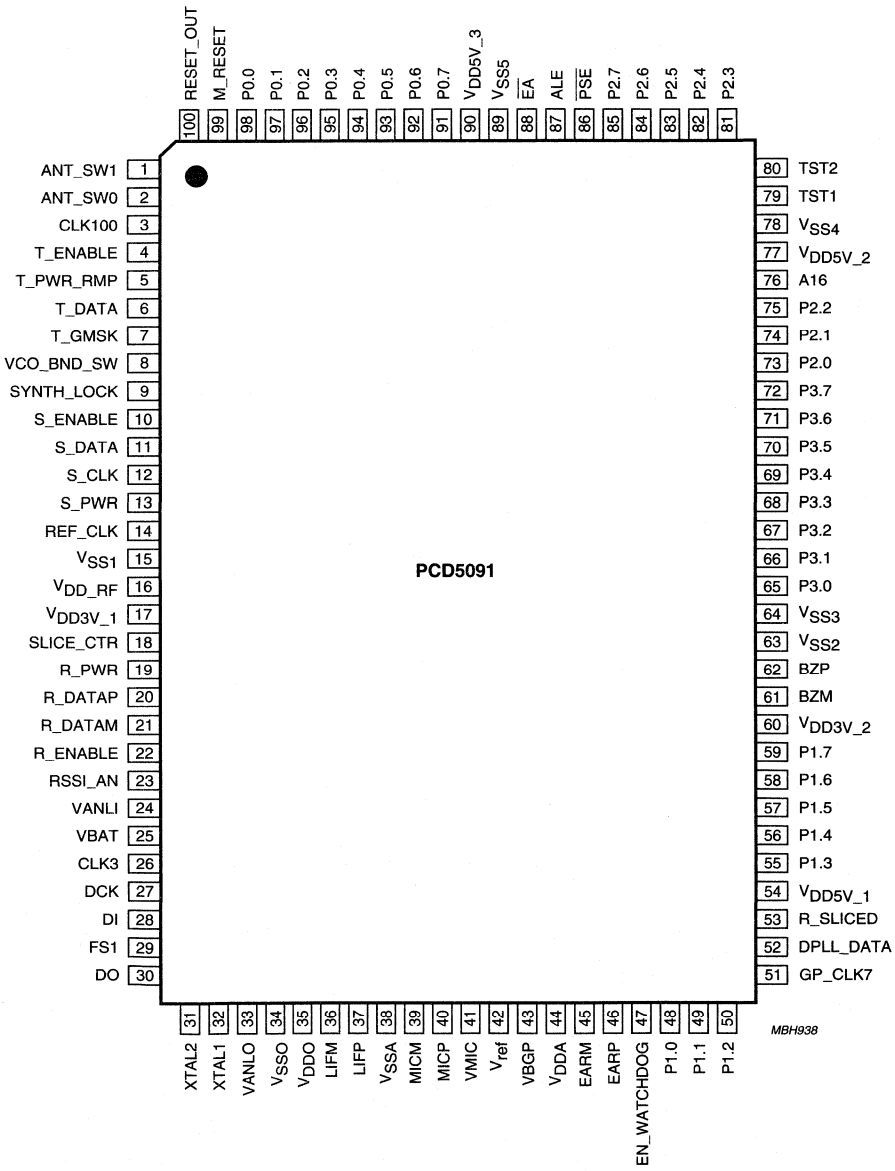


Fig.2 Pin configuration (QFP100).

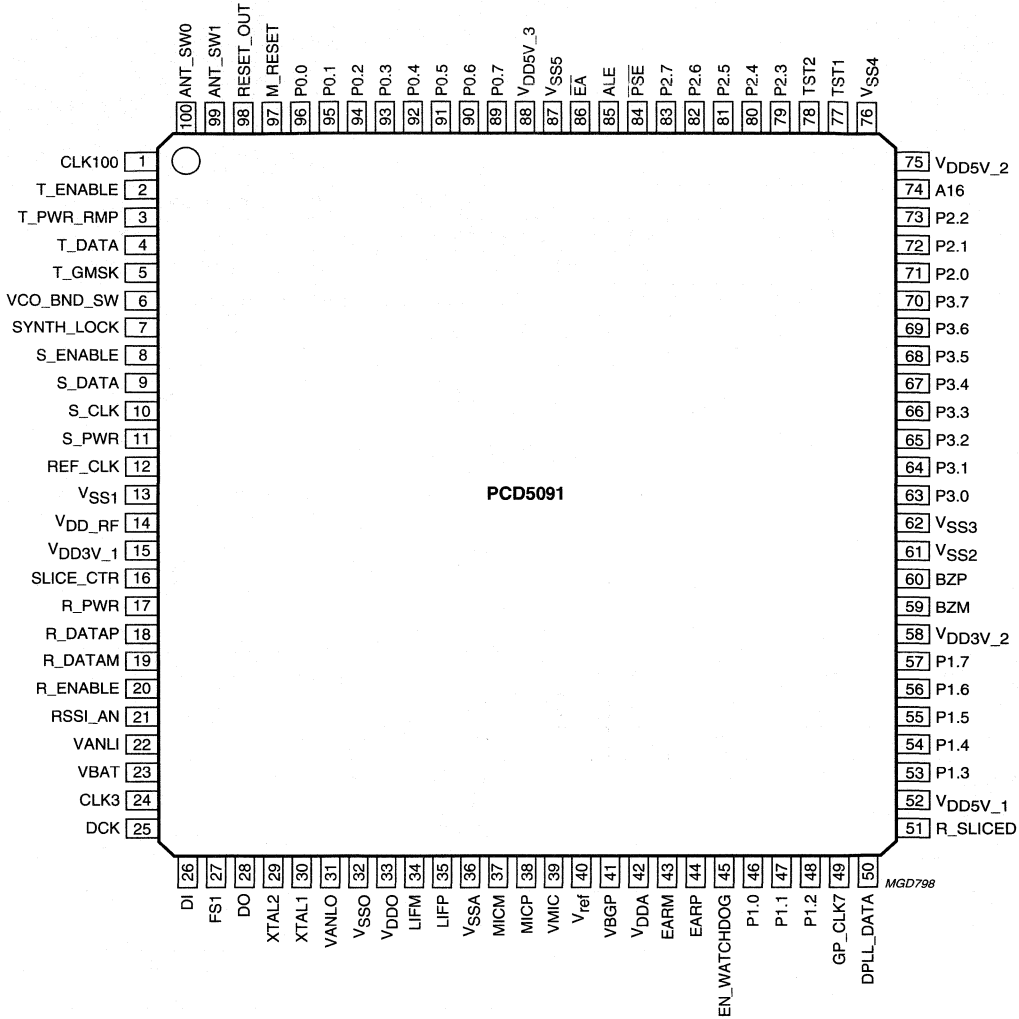


Fig.3 Pin configuration (LQFP100).

5.2 Pin description

Table 1 QFP100 and LQFP100 packages

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
ANT_SW1	1	99	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	100	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	1	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	2	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	3	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	4	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	5	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	6	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	7	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	8	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	9	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	10	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	11	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	12	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	13	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	14	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	15	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	16	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	17	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	18	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	19	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	20	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	21	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	22	I	–	ANAIOD1	analog input to ADC
VBAT	25	23	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	24	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec

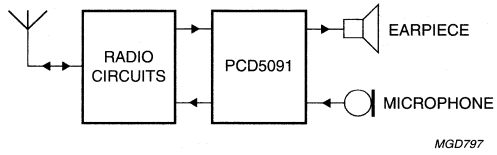
SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
DCK	27	25	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	26	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	27	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	28	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	29	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	30	I	–	ANAIOD1	crystal oscillator input
VANLO	33	31	O	1.0 V	ANAIOD1	analog output from D/A converter
V_{SSO}	34	32	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	33	–	–	supply	positive supply voltage for the oscillator
LIFM	36	34	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	35	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	36	–	–	supply	negative supply voltage for analog circuits
MICM	39	37	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	38	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	39	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	40	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	41	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	42	–	–	supply	positive supply voltage for analog circuits
EARM	45	43	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	44	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	45	I	–	DIUP0PES	watchdog enable input
P1.0	48	46	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	47	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	49	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	50	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	51	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	52	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	53	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	54	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P1.5	57	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	56	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	57	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	58	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	59	O	L	ANAIOD2	negative buzzer output
BZP	62	60	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	61	–	–	supply	negative supply voltage 2
V_{SS3}	64	62	–	–	supply	negative supply voltage 3
P3.0	65	63	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	64	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	74	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	75	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	76	–	–	supply	negative supply voltage 4
TST1	79	77	I	–	DIDP0PES	test input 1
TST2	80	78	I	–	DIDP0PES	test input 2
P2.3	81	79	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	80	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	84	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	85	O	H	ISQ4CPES	address latch enable (80C51)

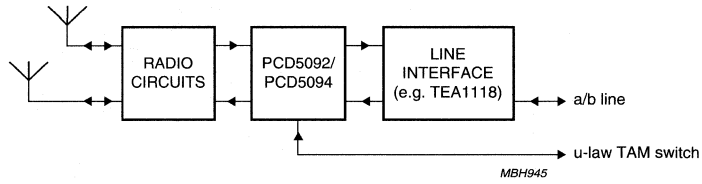
SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
$\overline{EA}$	88	86	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	87	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	88	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	89	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	90	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	97	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	98	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

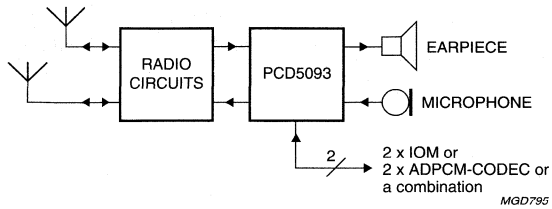
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I^2C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Base with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.4 Block diagrams of DECT systems with PCX509x.

CONTENTS

1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I^2C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot.
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- u-law encoding and decoding complying with G.711
- Echo cancellation and network echo suppressor
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Telephone Answering Machine (TAM) switch.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5092 is designed for GAP-compliant single a/b line basestations with answering machine switch. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5092H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

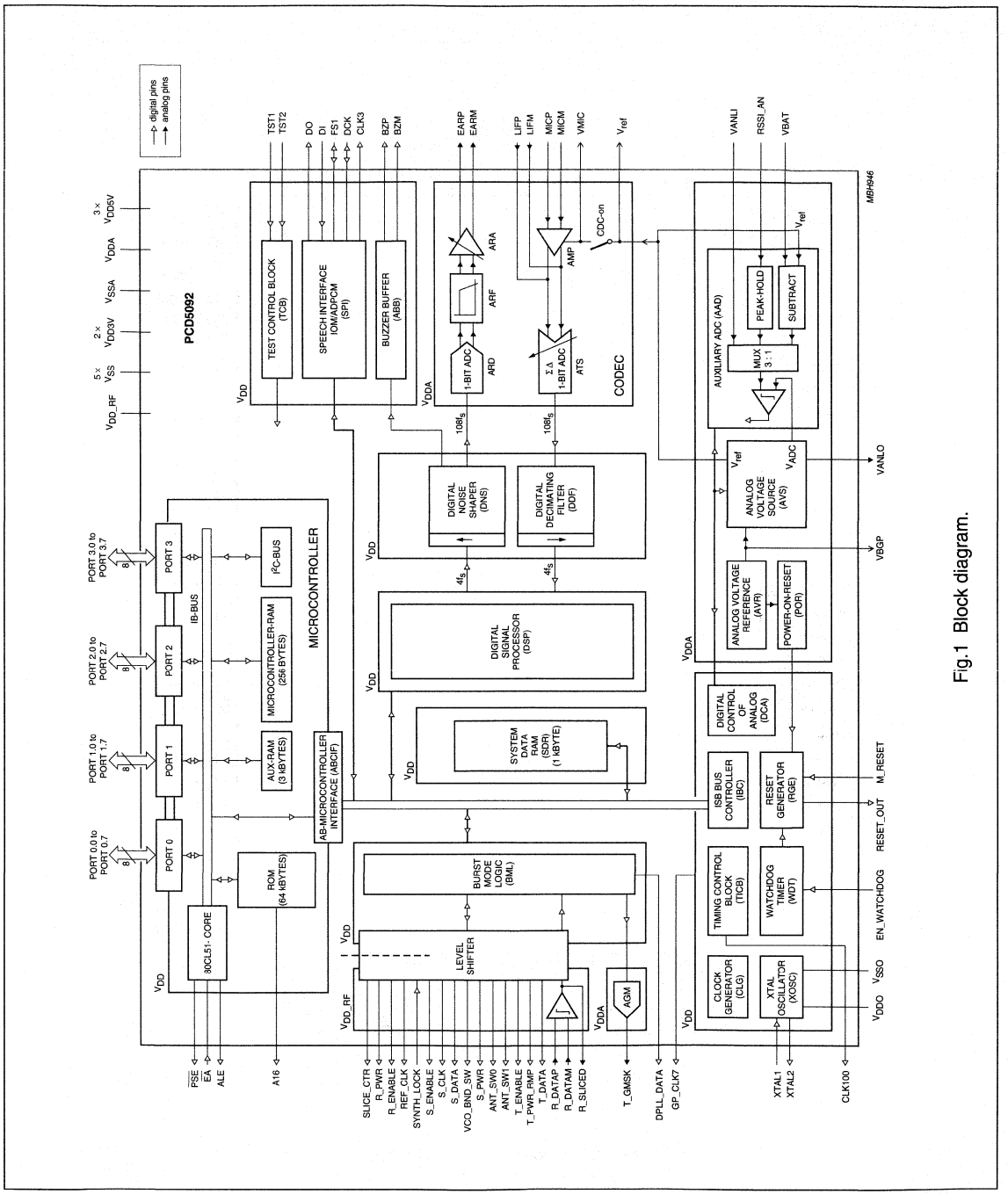


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

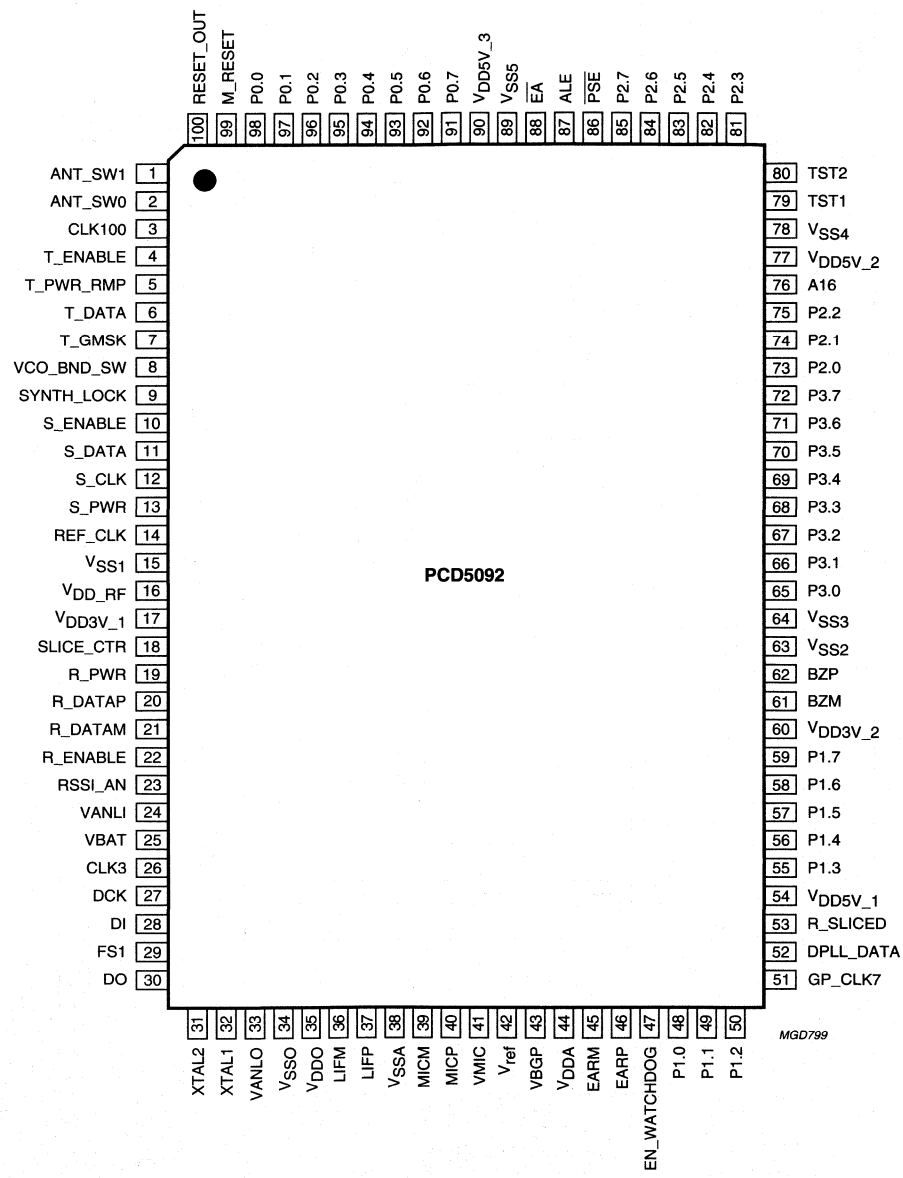


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

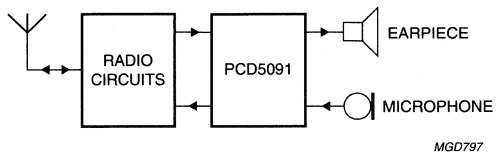
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

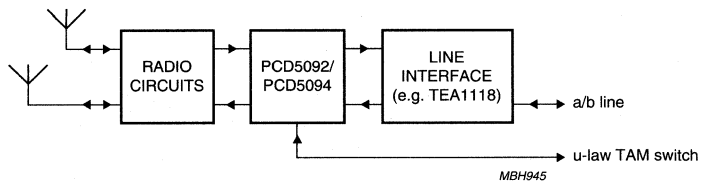
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

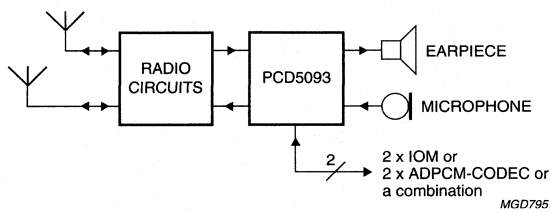
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation (PCD5092) with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.

CONTENTS

1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltages (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- Up to two A-law channels
- Network echo suppressor
- Support of local corded handset with handsfree feature
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Direct connection to universal codec PCD5096
- Conference between IOM-2 buffer(s) and two handsets.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5093 is designed as GAP-compliant basestation chip for ISDN or n lines (PCD5096) business systems. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5093H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

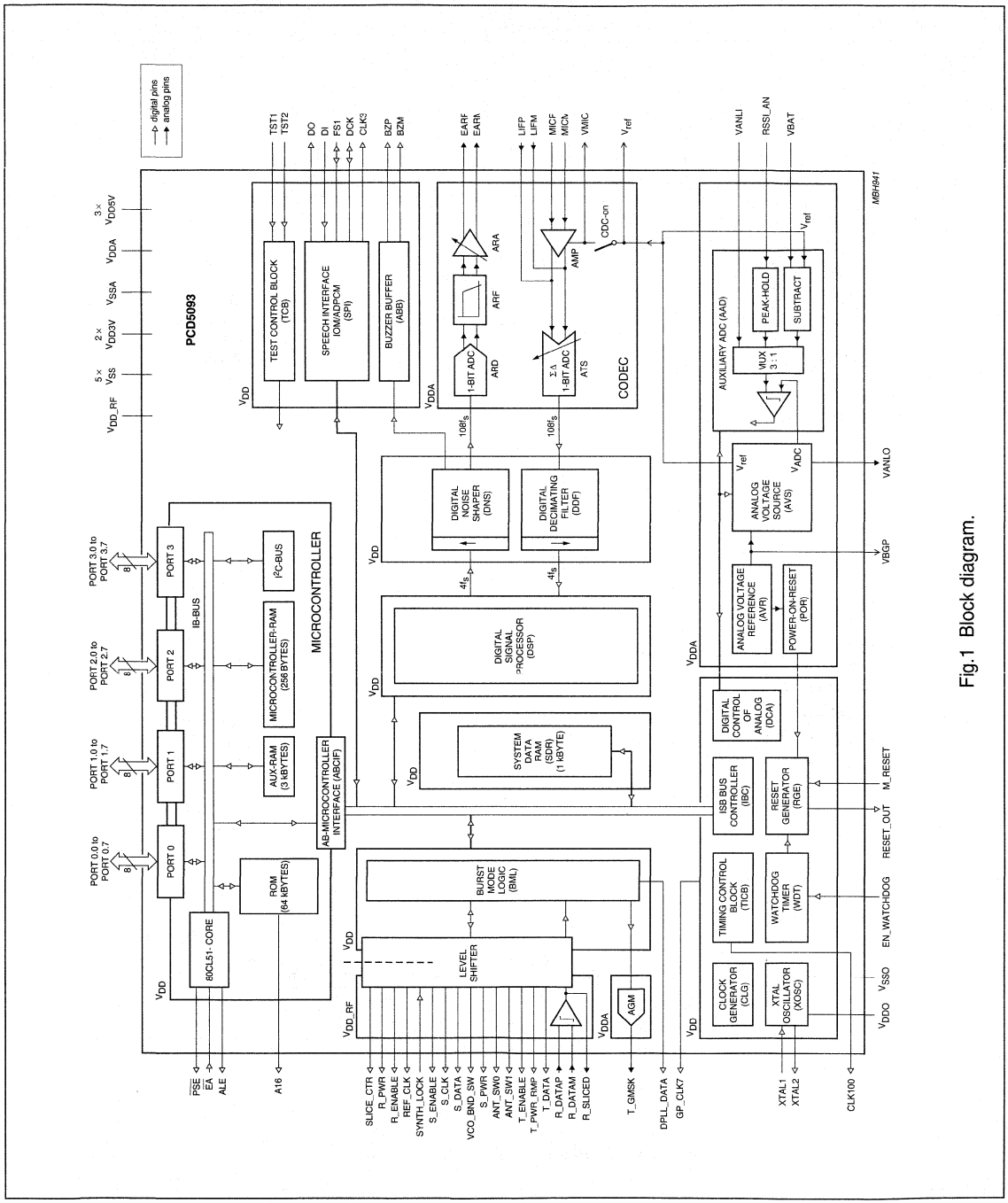


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

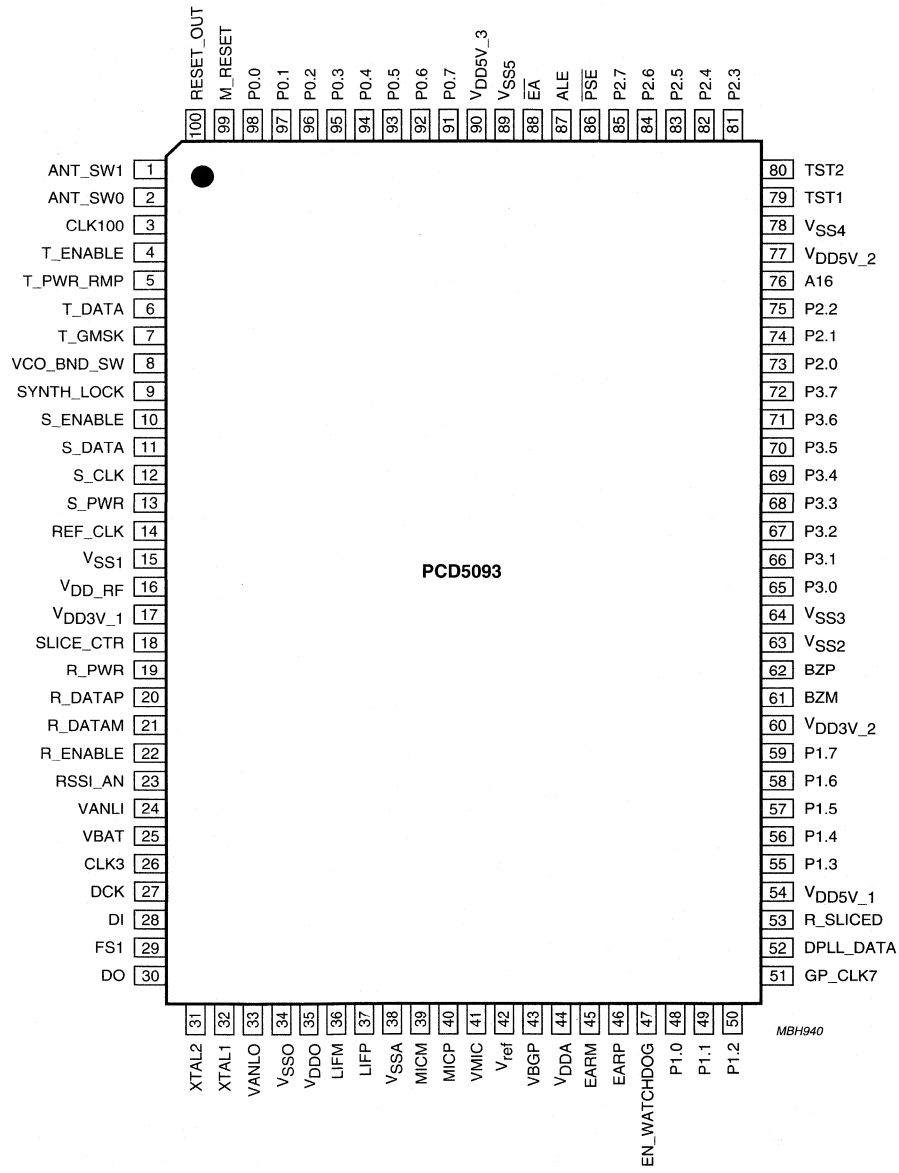


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

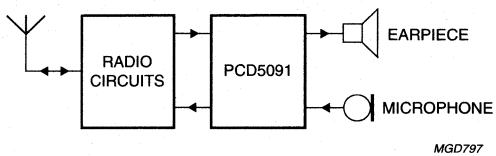
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

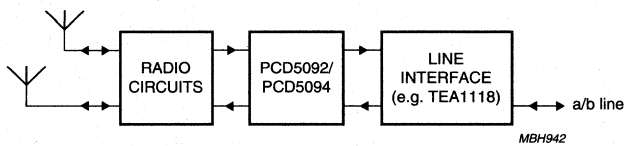
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

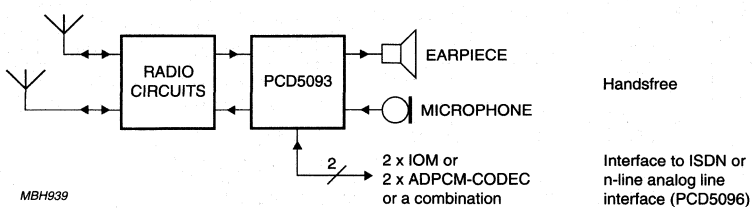
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base(PCD5093) with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.

CONTENTS

1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1kbyte System Data RAM. External program memory is addressable up to 128 kbytes
- +2.7 to 5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing, transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM®-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- On-chip comparator for use as data-slicer
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- Low-power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- 3x ADPCM transcoding complying with G.726
- A-Law encoding and decoding complying with G.711
- 4 Channel bidirectional ADPCM interface to the IOM®-2 and radio interface
- Programmable channel switching and buffers
- Channel mute.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5095 is designed for GAP-compliant business systems, PABX and WLL. Two modes can be selected: three channel ADPCM CODEC with conversion of ADPCM samples to linear PCM format and vice versa, the second mode copies four ADPCM samples into two IOM data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface. The performance of the embedded 80C51 microcontroller is twice the performance of the classic architecture. The PCD5095 has 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with the Burst Mode Logic (BML), the DSP and the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5095H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

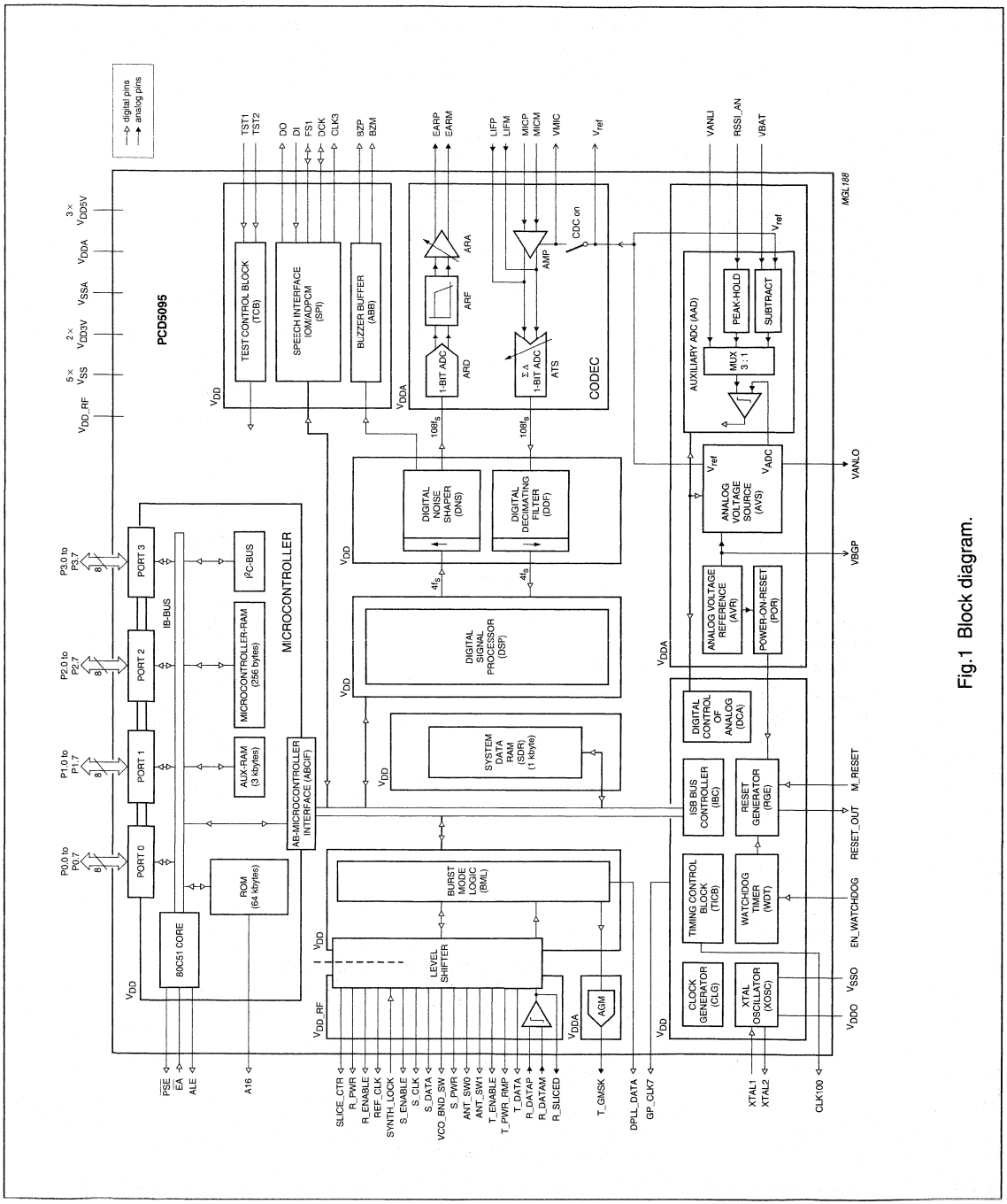


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

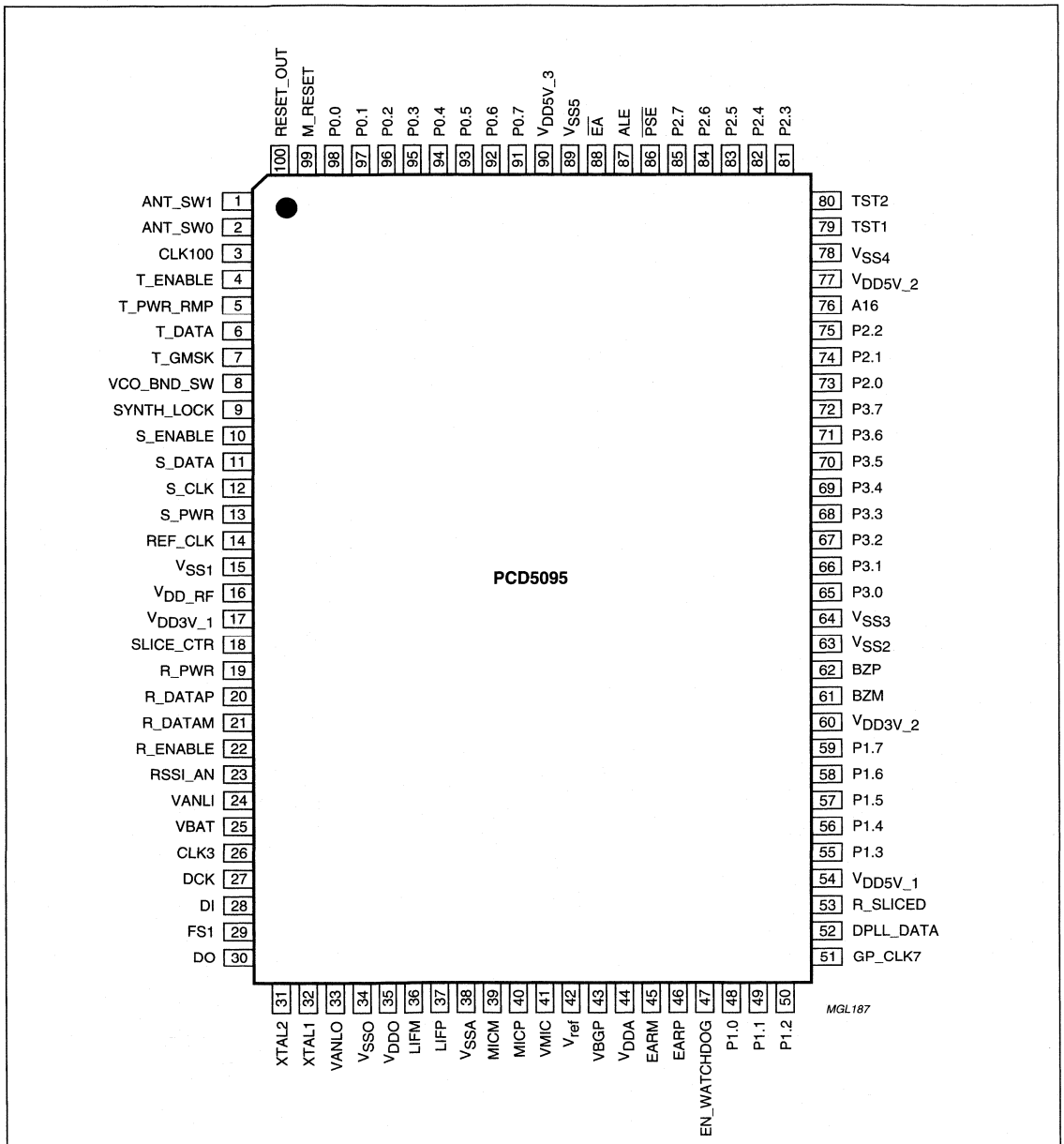


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM®-2 data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM®-2 data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM®-2 data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from DAC
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	Watchdog Timer enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I^2C-bus interface. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.

The PCD5095 is designed for business systems, PABX and WLL. Two modes can be selected: bidirectional conversion of three ADPCM channels based on linear PCM format, the second mode copies four ADPCM samples, without data processing, into two IOM®-2 data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface.

The data flow between radio, DSP and IOM®-2 is described in the *"PCD5095 DSP user manual"*. Basically the System Data RAM (SDR), the shared memory with inbound and outbound speech buffers, is the interface to the DSP and to the radio. Depending on the selected mode the DSP processes the data stored in the SDR. The speech buffers are 40 bytes long and each buffer can hold 80 ADPCM-coded speech samples.

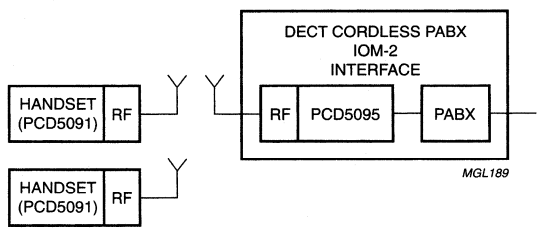
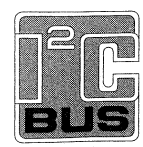


Fig.3 PCD5095 for PABX.

CONTENTS



1 FEATURES

- Applications in digital terminal equipment featuring line interface and/or voice functions
- Digital signal processor performing echo cancellation, codec functions and dial tone detection
- Two independent receive and transmit channels
- Independent programmable gain for all analog inputs and outputs
- Programmable filter correction functions
- Flexible configuration of all functions
- IOM-2 serial data interface (slave mode only)
- Serial data interface to DTAM speech compression ICs
- 400 kHz I^2C-bus slave interface (four I^2C-bus subaddresses)
- Codec compatible with G.714 CCITT specification
- PCM A-Law/u-Law (G.711 CCITT) and 16-bit linear data
- Dual differential inputs and outputs performing the following functions:
  - Line interface connection
  - Loudspeaker, speaker phone (hands-free)
  - Earpiece, microphone (handset)
- Peripheral interface: two I/O pins
- Separate ringer function
- Tone and ringer generator
- Conference call
- QFP44 package
- Low voltage (2.7 to 3.6 V)
- Low power consumption.

2 GENERAL DESCRIPTION

The universal codec combines two high resolution bidirectional analog channels with a DSP in a single chip. Besides the analog interfaces the PCD5096 includes two digital interfaces: an I^2C-bus interface allowing an external microcontroller to program the chip, and a 4-wire serial interface compatible with IOM-2 and with DTAM speech compression ICs. This programmable serial interface offers up to 14 channels and is capable of handling 8-bit (A-law) or 16-bit (linear PCM) data packages, or any combination of them. It opens the scope for a wide application area, for example in combination with the PCD5093H DECT baseband chip for digital cordless business applications.

Several PCD5096s can be connected together for small switching systems (PABX) offering a combination of corded and cordless functionality. Besides the basic functions like echo cancellation for two channels the on-chip DSP provides all necessary functions such as conference call and DTMF.

3 APPLICATIONS

The PCD5096 is designed for the telecommunications market and is targeting small business and residential systems offering a two-line interface or a one-line interface combined with hands-free speaker phone. Specific applications are detailed in Chapter 12.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5096H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

5 BLOCK DIAGRAM

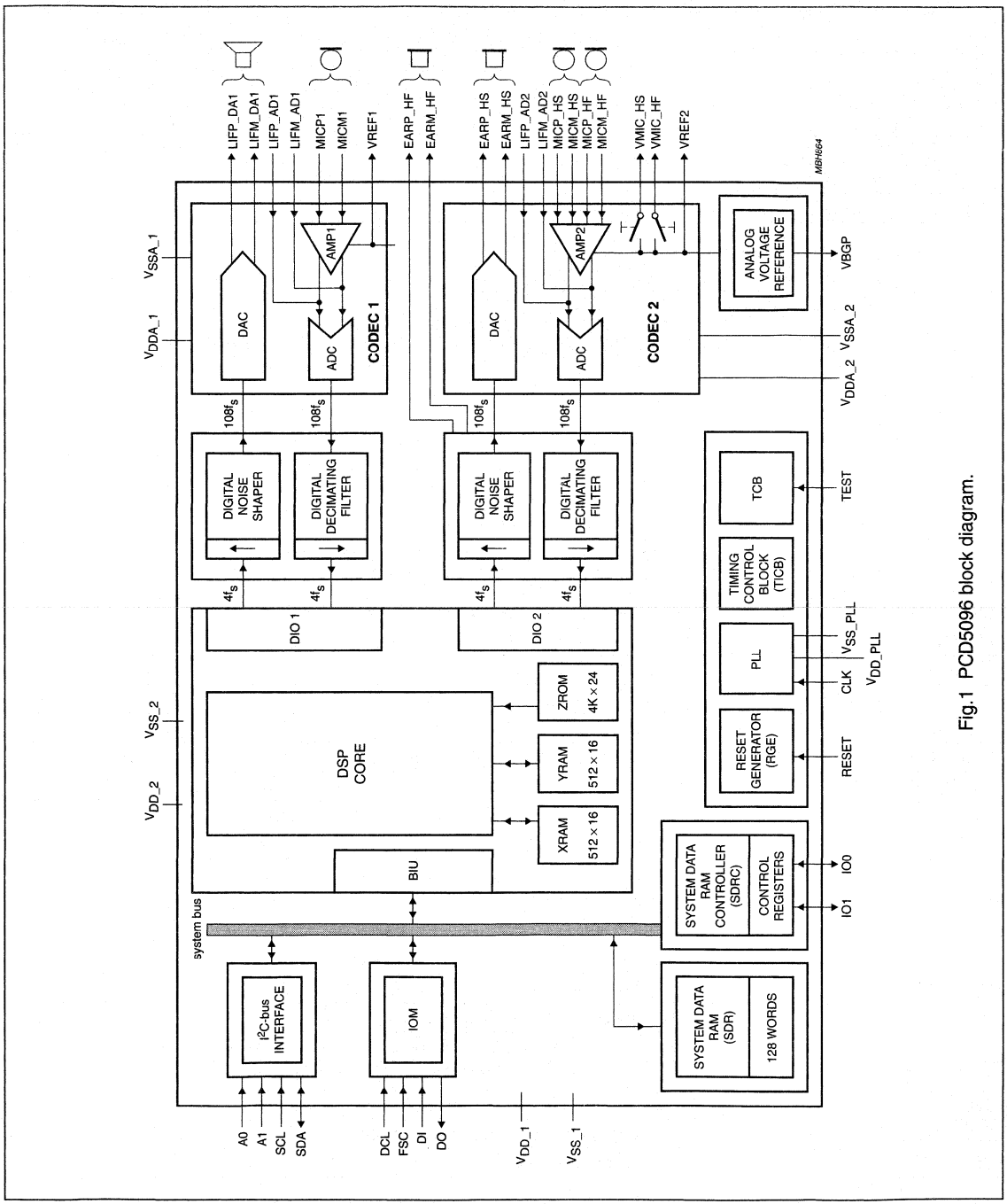


Fig.1 PCD5096 block diagram.

6 PINNING INFORMATION

6.1 Pin description

Table 1 QFP44 package

SYMBOL	PIN	I/O[1]	DESCRIPTION
IO0	1	I/O	programmable I/O pin 0 (Schmitt trigger input, pull-up output)
IO1	2	I/O	programmable I/O pin 1 (Schmitt trigger input, pull-up output)
CLK	3	I	clock input
V_{DD_PLL}	4	P	3 V analog supply for PLL
V_{SS_PLL}	5	P	analog ground supply for PLL
V_{SS_1}	6	P	peripheral ground supply
V_{DD_1}	7	P	3 to 5 V peripheral supply
SCL	8	I	I^2C-bus clock signal input (Schmitt trigger)
SDA	9	I/O	I^2C-bus data signal
A0	10	I	I^2C-bus subaddress
A1	11	I	I^2C-bus subaddress
LIFM_DA1	12	O	negative analog output from Codec 1 to line interface
LIFP_DA1	13	O	positive analog output from Codec 1 to line interface
V_{DDA_1}	14	P	3 V analog supply for Codec 1
LIFM_AD1	15	I	negative analog input to Codec 1 from line interface
LIFP_AD1	16	I	positive analog input to Codec 1 from line interface
V_{SSA_1}	17	P	analog ground supply for Codec 1
MICM1	18	I	negative analog input to Codec 1 from microphone
MICP1	19	I	positive analog input to Codec 1 from microphone
VREF1	20	O	Codec 1 analog reference voltage
VBGP	21	O	bandgap analog output voltage
VREF2	22	O	Codec 2 analog reference voltage
VMIC_HS	23	O	positive analog supply voltage from Codec 2 for handset microphone
MICP_HS	24	I	positive analog input to Codec 2 from handset microphone
MICM_HS	25	I	negative analog input to Codec 2 from handset microphone
VMIC_HF	26	O	positive analog supply voltage from Codec 2 for hands-free microphone
MICP_HF	27	I	positive analog input to Codec 2 from hands-free microphone
MICM_HF	28	I	negative analog input to Codec 2 from hands-free microphone
V_{SSA_2}	29	P	analog ground supply for Codec 2
LIFP_AD2	30	I	positive analog input to Codec 2 from line interface
LIFM_AD2	31	I	negative analog input to Codec 2 from line interface
V_{DDA_2}	32	P	3 V analog supply for Codec 2
EARP_HS	33	O	positive analog output from Codec 2 to handset earpiece
EARM_HS	34	O	negative analog output from Codec 2 to handset earpiece
EARP_HF	35	O	positive output to hands-free earpiece
EARM_HF	36	O	negative output to hands-free earpiece
TEST	37	I	test input; pull-down

SYMBOL	PIN	I/O[1]	DESCRIPTION
RESET	38	I	reset input (Schmitt trigger)
V_{SS_2}	39	P	digital core ground supply
V_{DD_2}	40	P	3 V digital core supply
DI	41	I	IOM-2 interface serial data input
DO	42	O	IOM-2 interface serial data output (open-drain)
FSC	43	I/O	IOM-2 interface 8 kHz frame synchronization clock (Schmitt trigger input); note 2
DCL	44	I/O	IOM-2 interface data clock (Schmitt trigger input); note 2

Note

1. 'P' denotes power line.
2. FSC and DCL are outputs only in test modes.

6.2 Pinning

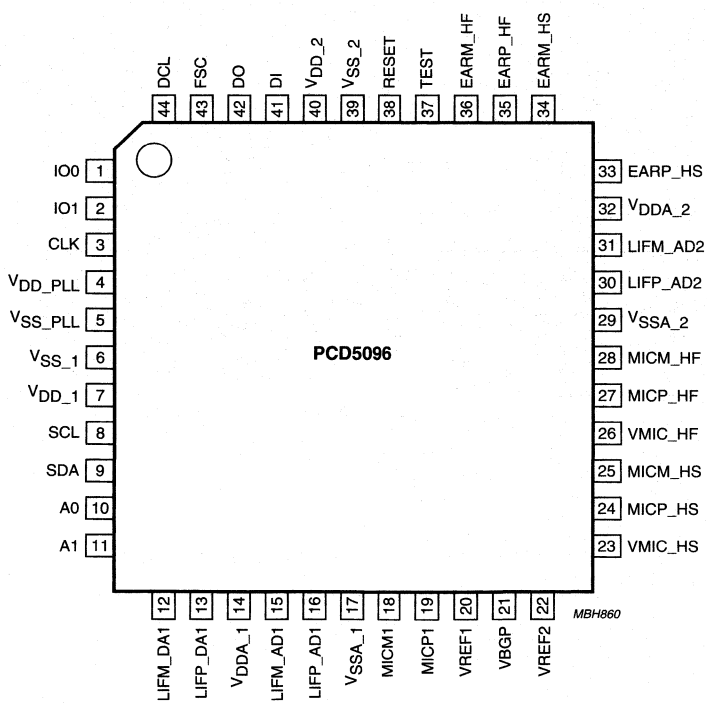


Fig.2 Pin configuration.

6.3 Supply concept

The universal codec is designed for 3 V systems with a voltage range of 2.7 to 3.6 V. To allow connection to 5 V systems the digital I/Os include level shifters. The core must run on 3.3 V and the peripheral supply on 5 V.

The five power supplies are listed in Table 2. Codec 1 and Codec 2 have their own power supplies: V_{DDA_1} and V_{DDA_2} respectively. V_{DD_PLL} is the power supply dedicated to the PLL. The digital core and the memories are powered by V_{DD_2} and the digital peripherals by V_{DD_1}. All digital pins (EARP_HF, EARM_HF, TEST, RESET, DI, DO, FSC, DCL, IO0, IO1, CLK, SCL, SDA, A0 and A1) have internal level shifters, allowing the chip to be used in a 3 to 5 V environment.

Table 2 PCD5096 power supply

SUPPLY PAIR	ASSOCIATED DEVICE
V_{DD_1} and V_{SS_1}	3 to 5 V peripheral supply
V_{DD_2} and V_{SS_2}	3 V digital core supply
V_{DD_PLL} and V_{SS_PLL}	3 V PLL supply
V_{DDA_1} and V_{SSA_1}	3 V Codec 1 supply
V_{DDA_2} and V_{SSA_2}	3 V Codec 2 supply

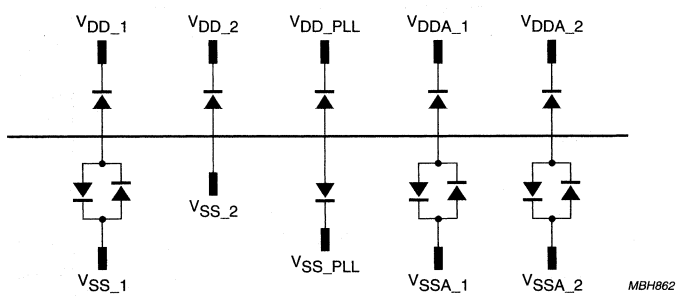


Fig.3 PCx5096 supply rails with protection diodes.

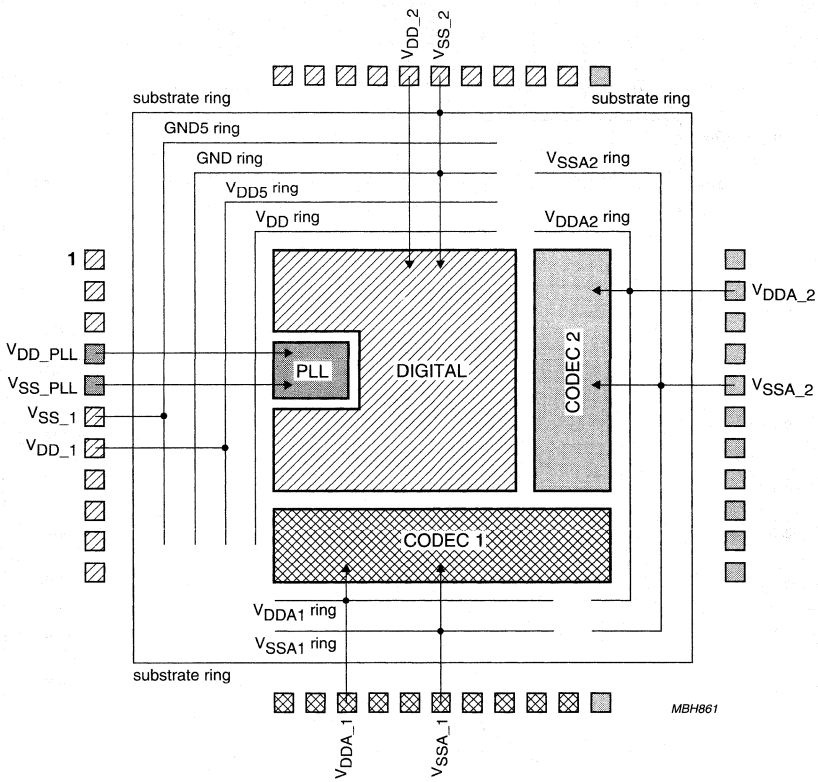


Fig.4 PCD5096 power supply.

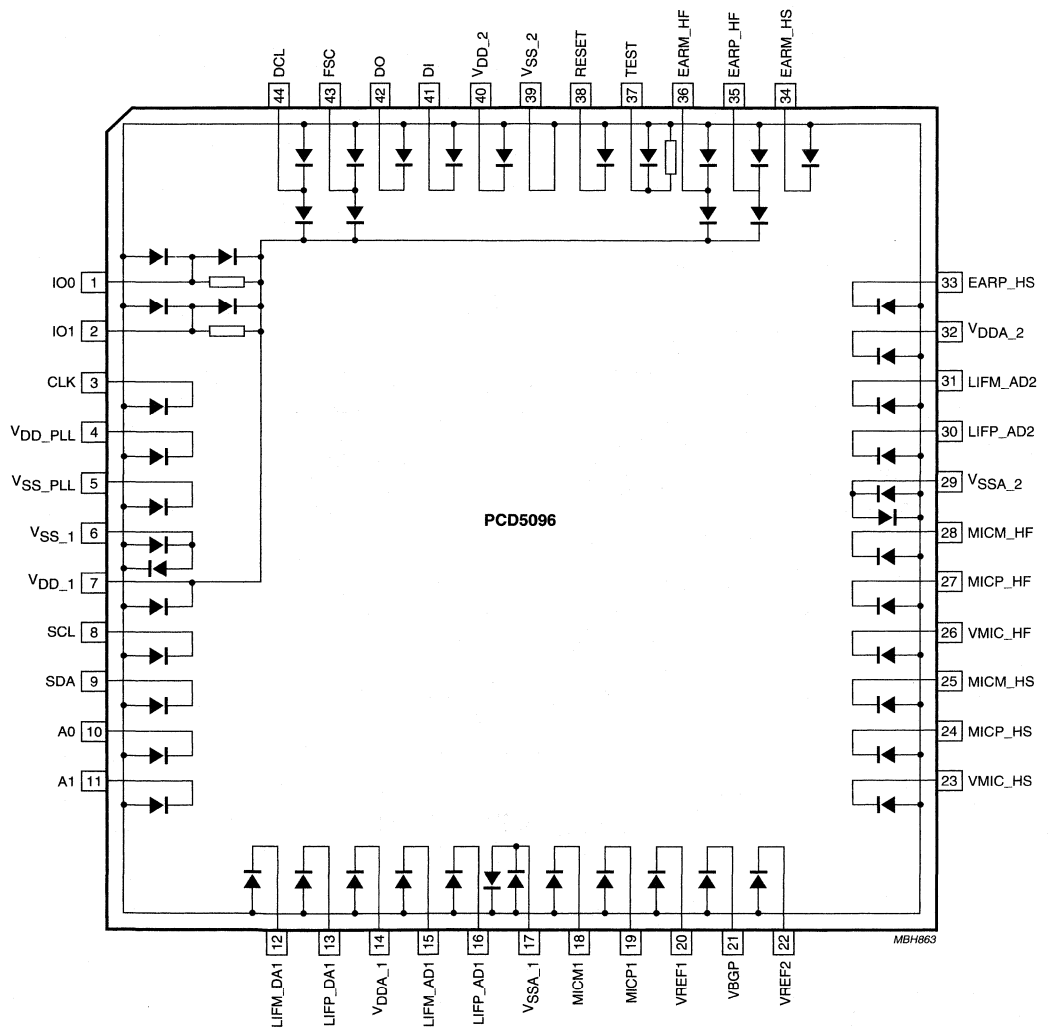


Fig.5 Open/short diagram.

7 FUNCTIONAL DESCRIPTION

7.1 General

The PCD5096 is a universal codec designed for use in digital terminal equipment. It connects two PSTN lines to a digital interface (IOM-2), thus covering a wide application area. Echo cancellation is performed on both PSTN lines by an on-chip DSP. Hands-free speaker phone functionality is also provided by sacrificing one PSTN line connection. The chip is controlled by an external microcontroller via a high bit rate I²C-bus interface.

Figure 1 shows the block diagram of the PCD5096. The different functional blocks operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Each block has access to the SDR via an internal system bus. Access to this bus is controlled by the System Data RAM Controller (SDRC).

The IOM block connects to a n × 256 kbits/s digital interface (IOM-2 interface) and also supports interfacing to DTAM speech compression ICs. The IOM block stores and fetches speech data into/from the SDR using internal addressing logic.

The DSP block is the link between the data in the SDR stored/fetched by the IOM block on one hand, and the analog front-end on the other hand. The basic functions of the DSP are data filtering, local echo cancelling, network echo suppressing, A-law coding and decoding according to the G.711 CCITT recommendations, dial tone detection and generation, DTMF generation, side-tone, automatic volume control, automatic gain control, double talk detection and conference call.

Data processed by the DSP goes to and comes from two independent codecs interfacing to the PSTN lines. The codecs comply with the G.714 specifications and handle the PCM coding and decoding of speech signals. They perform the analog and high speed digital speech processing functions: analog bitstream A/D and D/A conversion, analog filtering and amplification, digital decimation filtering and noise shaping. Both codecs should be connected to a local line or to a PSTN line, but one codec also supports a corded handset and hands-free speaker and microphone.

The control of the entire chip is done via the I²C-bus block by writing to the SDR or to special control registers. In this way the DSP and the IOM operation modes can be set, as well as some analog parameters in the two codecs.

The PCD5096 has two general purpose programmable I/O pins controlled by two special registers (direction and state). These two special registers are accessible via the I²C-bus interface or by the on-chip DSP. A typical application is the generation of interrupts by the DSP, indicating that DTMF tones were detected.

The timing for the whole chip is generated in the Timing Control Block (TICB). The system clock (20.736 MHz) is delivered by a PLL which triples the input clock frequency.

7.2 Clocking

The universal codec is designed to operate in a digital cordless telephone system, for example together with a PCD5093 baseband controller. To save the expense of having to provide each universal codec with a separate crystal, a common clock is provided by the master controller. In the current generation of the Philips DECT baseband controllers this clock is GP_CLK7, a 6.912 MHz clock output derived from the 13.824 MHz crystal oscillator. GP_CLK7 must therefore be used as the input clock for the universal codec. GP_CLK7 is enabled during a reset of the PCD5093 and when either the Burst Mode Logic or codec are turned on (see PCD5093 data sheet).

In order to meet the DSP processing requirements for the various applications an on-chip PLL is used to generate a system clock which is triple the input clock frequency (20.736 MHz).

7.3 Reset and power-down strategy

The universal codec must be reset at power-up. The RESET input must remain HIGH until the CLK input is active (toggling) and stable. After releasing the RESET input, an additional 1024 CLK periods (≈150 μs at 6.912 MHz) must elapse before starting to program the chip via the I²C-bus interface. This must be done after every RESET pulse. The minimum duration of a RESET pulse is one CLK period. During reset, the I²C-bus and the IOM-2 interface are inactive.

Entering the Power-down mode is achieved by resetting the chip and holding the RESET input HIGH. This resets the on-chip PLL and stops the system clock. The user must ensure that the IOM-2 interface is deactivated and the I²C-bus idle before resetting the chip in order not to interrupt any transaction on these two interfaces. Note that stopping the CLK input is only allowed while the RESET input is HIGH. To exit the Power-down mode the RESET input is set LOW and after 1024 CLK periods (≈150 μs at 6.912 MHz) have elapsed normal operation can be resumed.

After reset, all the flip-flops are in a defined state, and the IOM, DSP and codecs are in inactive mode. In typical applications the universal codec is used with the PCD5093, which provides a clock (GP_CLK7) and a reset signal to the universal codec. The reset signal must be generated by a microcontroller port bit. The RESET_OUT pin of the PCD5093 cannot be used for this purpose, because GP_CLK7 is stopped while RESET_OUT is LOW after a Power-on-reset.

8 MEMORY AND CONTROL REGISTERS

8.1 DSP memories

The DSP in the PCD5096 has access to a 4k × 24-bit DSP program ROM, a 512 × 16-bit XRAM and a 512 × 16-bit YRAM.

8.2 Data memory and control register map

The PCD5096 contains a 128 word (128 × 16-bit) System Data RAM (SDR) and a group of 7 control registers mapped onto the upper addresses of the SDR.
The registers and the SDR are byte and word accessible externally, via the I²C-bus interface and internally via the internal system bus.

The memory map is shown in Fig.6. The lower 32 words contain the DSP parameter table. The next 32 words are reserved for the IOM control table, which is used to control the activity on the IOM-2 interface (maximum 32 slots per 8 kHz speech frame). The rest of the SDR addressable space (40H to 77H) is free RAM and can be used to store up to 14 IOM data buffer pairs. In cases where not all 14 IOM buffer pairs are needed this memory space can be used for other applications via the I²C-bus. The same holds for the unused part of the IOM control table.

The upper addresses of the SDR (78H to 7EH) are mapped onto 7 control registers (CR0 to CR6) that control the entire chip (DSP mode, data rate on the IOM-2 interface, control of the two codecs).

Note that the uppermost address of the SDR (7FH) is not mapped to any hardware register and is addressable as a normal RAM word.

The contents of the IOM control table and the IOM data buffers are described in Chapter 9. For further details about the DSP parameter table, see the *"PCD5096 DSP user manual"*.

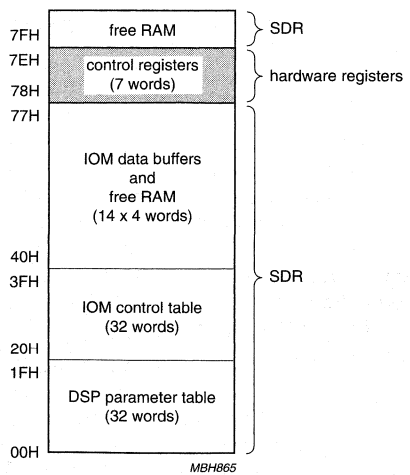


Fig.6 PCD5096 Memory map.

8.3 Control registers organization

8.3.1 CONTROL REGISTER ASSIGNMENT

The control register address assignment in the PCD5096 is shown in Table 3.

Table 3 Control register map

REGISTER	REGISTER MNEMONIC	SIZE (BITS)	ADDRESS (HEX)	RESET STATE (HEX)	FUNCTION
Control Register 0	CR0	16	78	0000	control signals for codecs, codec test modes, Power-down control and disable phase correction
Control Register 1	CR1	3	79	00	IOM control
Control Register 2	CR2	16	7A	0000	gain setting of analog-to-digital (A/D) and digital-to-analog (D/A) paths
Control Register 3	CR3	16	7B	A0A0	reference voltage setting of Codec 1 and Codec 2
Control Register 4	CR4	16	7C	0000	selection of the DSP modes
Control Register 5	CR5	2	7D	02	control of I/O pin IO0
Control Register 6	CR6	2	7E	02	control of I/O pin IO1

8.3.2 Control Register 0 (CR0)

Table 4 Control Register 0 (address 78H)

15	14	13	12	11	10	9	8
–	DISPC	CDC2TM2	CDC2TM1	CDC2TM0	CDC1TM2	CDC1TM1	CDC1TM0

Table 5 Control Register 0 (continued)

7	6	5	4	3	2	1	0
HFMICON	HSMICON	LHFEN	EHSEN	CDC2ON	ADD_DC	LIF1_EN	CDC1ON

Table 6 Description of CR0 bits

BIT	SYMBOL	DESCRIPTION
15	–	reserved, not used
14	DISPC	**Disable Phase Correction.** If DISPC = 1, phase correction is disabled.
13	CDC2TM2	**Functional test modes of Codec 2.** These 3 bits select the functional test modes of Codec 2; see Table 7.
12	CDC2TM1	
11	CDC2TM0	
10	CDC1TM2	**Functional test modes of Codec 1.** These 3 bits select the functional test modes of Codec 1; see Table 7.
9	CDC1TM1	
8	CDC1TM0	
7	HFMICON	**Hands-free Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HF (supply pad for the external hands-free microphone).
6	HSMICON	**Handset Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HS (supply pad for the external handset microphone).
5	LHFEN	**Loudspeaker Enable for hands-free.** This bit enables the Noise Shaper data in Codec 2 to the hands-free pads EARP_HF and EARM_HF.
4	EHSEN	**Earpiece Enable for Handset.** This bit enables the Noise Shaper data to the DAC in Codec 2.
3	CDC2ON	**Codec 2 ON.** When CDC2ON = 1, Codec 2 is ON.
2	ADD_DAC	**Add a DC offset in the microphone amplifier of Codec 1.**
1	LIF1_EN	**Line Interface Enable for Codec 1.** This bit enables the Noise Shaper data to the DAC in Codec 1.
0	CDC1ON	**Codec 1 ON.** When CDC1ON = 1, Codec 1 is ON.

Table 7 Selection of functional test modes for Codec 1 and Codec 2

CDC2TM2	CDC2TM1	CDC2TM0	FUNCTIONAL TEST MODE
CDC1TM2	CDC1TM1	CDC1TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

8.3.3 CONTROL REGISTER 1 (CR1)

Table 8 Control Register 1 (address 79H)

2	1	0
IOM2	IOM1	IOM0

Table 9 Description of CR1 bits

BIT	SYMBOL	DESCRIPTION
2	IOM2	These 3 bits select the IOM mode; see Table 10.
1	IOM1	
0	IOM0	

Table 10 Selection of IOM mode

IOM2	IOM1	IOM0	IOM MODE
0	0	0	inactive
0	0	1	not used
0	1	0	IOM slave 256 kbits/s in 4 speech-slots/speech-frame
0	1	1	IOM slave 512 kbits/s in 8 speech-slots/speech-frame
1	0	0	IOM slave 768 kbits/s in 12 speech-slots/speech-frame
1	0	1	IOM slave 1024 kbits/s in 16 speech-slots/speech-frame
1	1	0	SpeechPro slave 2048 kbits/s in 32 speech-slots/speech-frame; note 1
1	1	1	IOM slave 2048 kbits/s in 32 speech-slots/speech-frame

Note

1. The SpeechPro mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.

8.3.4 Control Register 2 (CR2)

CR2 contains the gain setting values of the analog Codec 1 and Codec 2 section. The state of CR2 after reset is 0000H. This sets the A/D path and the D/A path gain to their minimum values of +9 dB and −13 dB respectively.

The D/A path gain is defined as the relationship between the level of the analog output signal, differentially seen at EARP_HS - EARM_HS or LIFP_DA1 - LIFM_DA1, expressed in dBm (0 dBm0 is 1 mW in 600 Ω), and the level of the digital input signal at the PCM interface, expressed in dBm0 according to CCITT Recommendation G.711. This D/A path gain definition assumes that the volume control in the DSP is set to the default value of 0 dB.

The A/D path gain is defined as the relationship between the level of the digital output signal at the PCM interface, expressed in dBm0, and the level of the analog input signal at the LIF interface, differentially seen at LIFP_AD2 - LIFM_AD2 or LIFP_AD1 - LIFM_AD1, expressed in dBm.

Table 11 Control Register 2 (address 7AH)

15	14	13	12	11	10	9	8
DA2.3	DA2.2	DA2.1	DA2.0	AD2.3	AD2.2	AD2.1	AD2.0

Table 12 Control Register 2 (continued)

7	6	5	4	3	2	1	0
DA1.3	DA1.2	DA1.1	DA1.0	AD1.3	AD1.2	AD1.1	AD1.0

Table 13 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	DA2.3	These 4 bits select the D/A path gain for Codec 2; see Table 14.
14	DA2.2	
13	DA2.1	
12	DA2.0	
11	AD2.3	These 4 bits select the A/D path gain for Codec 2; see Table 15.
10	AD2.2	
9	AD2.1	
8	AD2.0	
7	DA1.3	These 4 bits select the D/A path gain for Codec 1; see Table 14.
6	DA1.2	
5	DA1.1	
4	DA1.0	
3	AD1.3	These 4 bits select the A/D path gain for Codec 1; see Table 15.
2	AD1.2	
1	AD1.1	
0	AD1.0	

Table 14 Selection of D/A path gain for Codec 1 and Codec 2

DA1.3	DA1.2	DA1.1	DA1.0	D/A PATH GAIN (dB)
DA2.3	DA2.2	DA2.1	DA2.0	
0	0	0	0	−13
0	0	0	1	−12
0	0	1	0	−11
0	0	1	1	−10
0	1	0	0	−9
0	1	0	1	−8
0	1	1	0	−7
0	1	1	1	−6
1	0	0	0	−5
1	0	0	1	−4
1	0	1	0	−3
1	0	1	1	−2
1	1	0	0	−1
1	1	0	1	0
1	1	1	0	+1
1	1	1	1	+2

Table 15 Selection of A/D path gain for Codec 1 and Codec 2

AD1.3	AD1.2	AD1.1	AD1.0	A/D PATH GAIN (FROM LIF TO PCM) (dB)
AD2.3	AD2.2	AD2.1	AD2.0	
0	0	0	0	+9
0	0	0	1	+10
0	0	1	0	+11
0	0	1	1	+12
0	1	0	0	+13
0	1	0	1	+14
0	1	1	0	+15
0	1	1	1	+16
1	0	0	0	+17
1	0	0	1	+18
1	0	1	0	+19
1	0	1	1	+20
1	1	0	0	+21
1	1	0	1	+22
1	1	1	0	+23
1	1	1	1	+24

8.3.5 Control Register 3 (CR3)

This 16-bit register is used to adjust the reference voltage of Codec 1 and Codec 2 to 2000 mV. An accuracy of 12 mV is guaranteed. The equation for determining the reference voltage (VREFn) for each codec is given below:

$$VREFn = \frac{256 \times VBGP}{RVnREF}$$

Where 'n' is the codec number and can take a value of '1' or '2'. The default value for VBGP is 1.25 V but this may vary due to process spread (see Chapter 16). Note that increasing RVnREF reduces VREFn.

For correct function of the analog blocks, care must be taken to have sensible values in CR3. For example, bits (15:14), as well as (7:6) must be '10'. The state of this register after reset is A0A0H.

Table 16 Control Register 3 (address 78H)

15	14	13	12	11	10	9	8
1	0	RV2REF5	RV2REF4	RV2REF3	RV2REF2	RV2REF1	RV2REF0

Table 17 Control Register 3 (continued)

7	6	5	4	3	2	1	0
1	0	RV1REF5	RV1REF4	RV1REF3	RV1REF2	RV1REF1	RV1REF0

Table 18 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	–	This bit must be set to a logic 1.
14	–	This bit must be set to a logic 0.
13	RV2REF5	These 5 bits are used to select the reference voltage of Codec 2.
12	RV2REF4	
11	RV2REF3	
10	RV2REF2	
9	RV2REF1	
8	RV2REF0	
7	–	This bit must be set to a logic 1.
6	–	This bit must be set to a logic 0.
5	RV1REF5	These 5 bits are used to select the reference voltage of Codec 1.
4	RV1REF4	
3	RV1REF3	
2	RV1REF2	
1	RV1REF1	
0	RV1REF0	

8.3.6 Control Register 4 (CR4)

CR4 is used to select the DSP modes. For further information see the *"PCD5096 DSP user manual"*. Its state after reset is 0000H.

Table 19 Control Register 4 (address 7CH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–	LLb2	LLb1	LLb0	LLa2	LLa1	LLa0	OPM1	OPM0

Table 20 Description of CR4 bits

BIT	SYMBOL	DESCRIPTION
15 to 8	–	These 8 bits are not used.
7	LLb2	These 3 bits select the connection mode for channel LLb; see Table 21.
6	LLb1	
5	LLb0	
4	LLa2	These 3 bits select the connection mode for channel LLa; see Table 21.
3	LLa1	
2	LLa0	
1	OPM1	These 2 bits select the operation mode, see Table 22.
0	OPM0	

Table 21 Selection of the connection mode for channels LLb and LLa

LLb2	LLb1	LLb0	CONNECTION MODES
LLa2	LLa1	LLa0	
0	0	0	Idle mode with reset of LEC coefficients
0	0	1	Idle mode without reset of LEC coefficients
0	1	0	speech and tone
0	1	1	tone generation
1	0	0	dial tone detection
1	0	1	not allowed
1	1	0	not allowed
1	1	1	not allowed

Table 22 Selection of the operation mode

OPM1	OPM0	OPERATION MODE
0	0	connection mode
0	1	read/write RAM mode
1	0	software reset
1	1	not allowed

8.3.7 Control Register 5 (CR5)

CR5 controls the general purpose I/O pin IO0.

Table 23 Control Register 5 (address 7DH)

1	0
IODIR0	IO0

Table 24 Description of CR5 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR0	Direction control for IO0. If IODIR0 = 1, then IO0 is an input. If IODIR0 = 0, then IO0 is an output. Input during and after reset; see note 1.
0	IO0	State of IO0

Note

1. Depending on the DSP program, the contents of CR5 might be overwritten by the DSP as soon as the reset is inactive.

8.3.8 Control Register 6 (CR6)

CR6 controls the general purpose I/O pin IO1.

Table 25 Control Register 6 (address 7EH)

1	0
IODIR1	IO1

Table 26 Description of CR6 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR1	Direction control for IO1. If IODIR1 = 1, then IO1 is an input. If IODIR1 = 0, then IO1 is an output. Input during and after reset; see note 1.
0	IO1	State of IO1

Note

1. Depending on the DSP program, the contents CR6 might be overwritten by the DSP as soon as the reset is inactive.

9 IOM

9.1 Features

The IOM block in the PCD5096 is a 4-wire serial interface performing the following functions:

- Digital interface with up to fourteen 64 kbits/s channels at a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8), complying with the IOM-2 specifications (IOM-2 is a registered trademark of Siemens AG)
- Digital interface with 32 slots/frame and non-doubled data clock, compatible with the digital interface of some DTAM speech compression ICs
- Autonomous storing/fetching of data to/from the system data memory (SDR) using internal addressing logic
- Byte or word (16 bits) transfer
- 14 data buffers (byte or word)
- Muting of speech data
- Local call.

9.2 Pin description

The following pins are used by the IOM-2 interface:

- **DI**: serial data input with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8)
- **DO**: serial data output with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8). DO is an open-drain pin, as many devices must be able to write on the same data line in a time-multiplexed mode. Therefore, DO must be externally pulled-up.
- **FSC**: 8 kHz frame synchronization input
- **DCL**: data clock input. Twice the data transmission frequency on DI and DO, except in the non-doubled data clock mode (see Section 9.3).

9.3 Functional description

The digital interface of the PCD5096 can work at several bit rates; these are specified Table 27. The bit rate is selected by writing the appropriate 3 bit code, given in Table 27, into Control Register 1 (address 79H).

The PCD5096 is always a slave on the IOM interface, which means that both FSC and DCL are inputs. This is valid for both the IOM modes and the Speech mode.

FSC is an 8 kHz framing signal for synchronizing data transmission on DI and DO. The rising edge of FSC gives the time reference for the first bit transmitted in the first slot of a speech frame. The number of slots per speech frame depends on the selected data rate. Each slot contains 8 data bits.

DCL is a data clock. Its frequency is twice the selected data rate in IOM mode. In Speech mode, the DCL frequency is equal to the data rate (2048 kHz for 2048 kbits/s).

DI is the serial data input. Data coming on DI in packets of 8 bits (A-law PCM encoded data) or 16 bits (linear PCM data) is stored temporarily in an IOM data buffer, from where it is processed by the on-chip DSP. On the other hand, data written into the IOM data buffers by the DSP is shifted out on pin DO.

There are 14 IOM data buffers, allowing the use of 14 different channels. One channel is 64 kbits/s for A-law PCM encoded data and 128 kbits/s if linear PCM data is transferred, in which case two consecutive slots are used.

The Speech mode was implemented to support the codec interface of some speech compression ICs. This mode is very similar to the IOM 32 slots mode, the main difference being the non-doubled data clock. See Section 9.4 for timing information.

Table 27 IOM modes

IOM2	IOM1	IOM0	MODE
0	0	0	These codes deactivate the IOM-2 interface and stop all the transactions on the IOM bus. This is the default state after reset.
0	0	1	
0	1	0	IOM slave mode, 256 kbits/s in 4 slots/speech-frame
0	1	1	IOM slave mode, 512 kbits/s in 8 slots/speech-frame
1	0	0	IOM slave mode, 768 kbits/s in 12 slots/speech-frame
1	0	1	IOM slave mode, 1024 kbits/s in 16 slots/speech-frame
1	1	0	Speech mode, 2048 kbits/s in 32 slots/speech-frame. The Speech mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.
1	1	1	IOM slave mode, 2048 kbits/s in 32 slots/speech-frame

9.4 Timing

The timing on the 4-wire interface for the IOM mode is shown in Fig.7 and specified in Table 28. The timing for the Speech mode is shown Fig.8 and specified in Table 29.

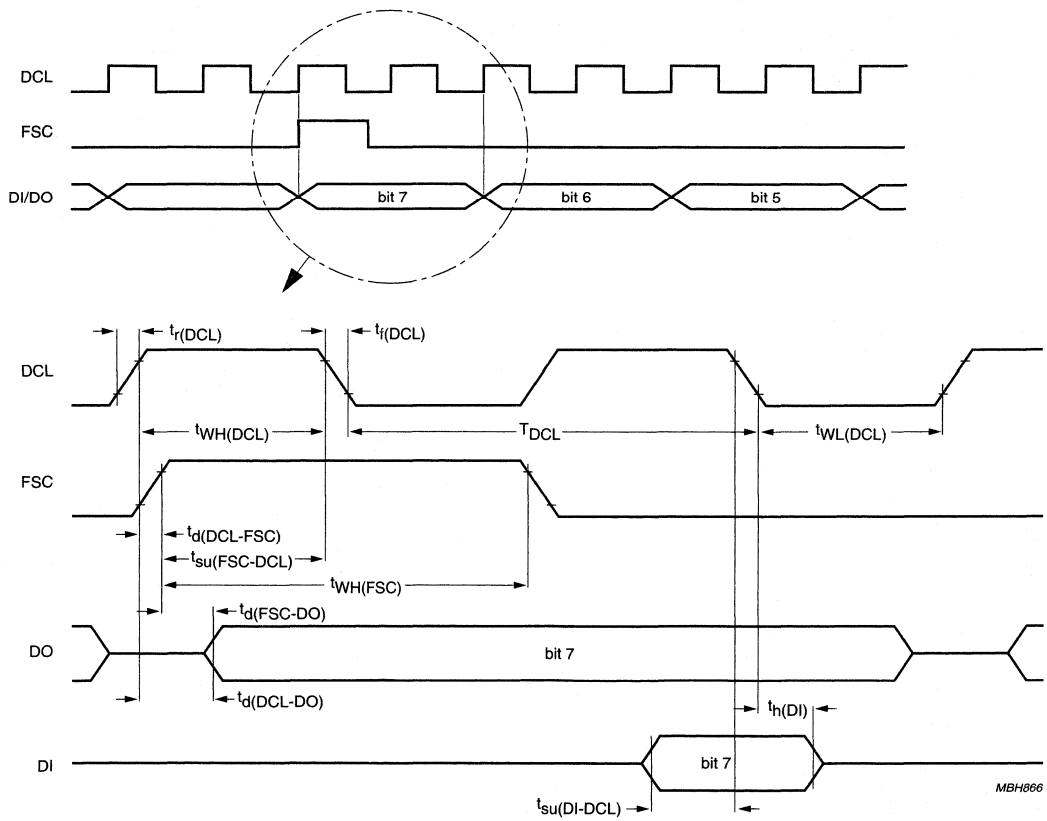


Fig.7 4-wire interface timing in IOM mode.

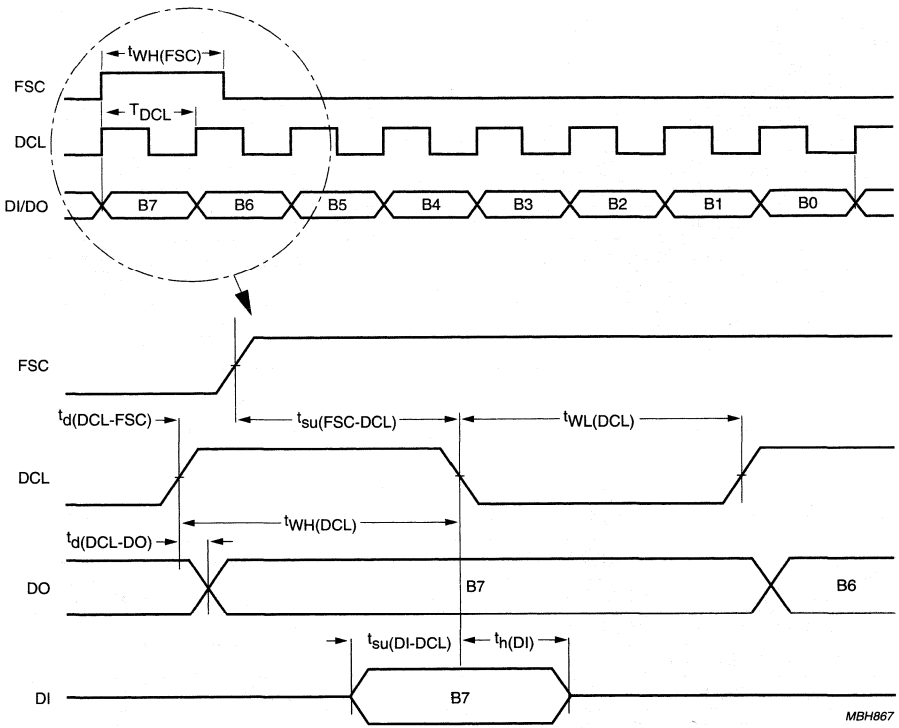


Fig.8 4-wire interface timing in Speech mode.

Table 28 Timing parameters in IOM mode; see Fig.7

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{r(DCL)}$	data clock rise time	–	60	ns
$t_{f(DCL)}$	data clock fall time	–	60	ns
T_{DCL}	data clock period	220[1]	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	80	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	80	–	ns
$t_{r(FSC)}$	frame sync rise time	–	60	ns
$t_{f(FSC)}$	frame sync fall time	–	60	ns
$t_{d(DCL-FSC)}$	frame delay DCL to FSC	$-t_{WL(DCL)}$	60	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
$t_{d(DLC-DO)}$	data delay from data clock	–	100[2]	ns
$t_{d(FSC-DO)}$	data delay from frame	–	150[2]	ns
$t_{su(DI-DCL)}$	set-up time DI to DCL	$t_{WH(DCL)}$	–	ns
$t_{h(DI)}$	data hold time	50	–	ns

Notes

1. Corresponds to the highest DCL frequency allowed (4.096 MHz) with a 10% margin.
2. C_L = 150 pF.

Table 29 Timing parameters in Speech mode; see Fig.8

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{d(DCL-FSC)}$	frame delay time DCL to FSC	$-t_{WL(DCL)}$	100	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
T_{DCL}	data clock period	440[1]	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	150	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	150	–	ns
$t_{d(DCL-DO)}$	data delay from clock	–	100[2]	ns
$t_{su(DI-DCL))}$	set-up time DI to DCL	60	–	ns
$t_{h(DI)}$	data hold time	60	–	ns

Notes

1. Corresponds to the DCL frequency (2.048 MHz) with a 10% margin.
2. C_L = 150 pF.

9.5 IOM control table

The selection of active slots in the IOM-2 interface and the logic connection between an IOM slot and an IOM data buffer is defined in the IOM control table located at addresses 20H to 3FH of the SDR. The IOM control table is 'n' words long. The number 'n' is the number of slots resulting from the IOM mode selection in Control Register 1. Speech slot 0 is defined by word 0 (address 20H) in the IOM control table, and speech slot 'n' by word 'n' (address 20H + n). The IOM interface block reads all words in the IOM control table once every speech frame (125 μs). In every IOM slot in a speech frame the IOM-2 interface block reads the corresponding word in the IOM control table. The function of the bits within each word is shown in Table 30. Depending on the IOM mode selected, only part of the IOM control table address space is used. The unused space is free for extra IOM data buffers or for other applications.

Table 30 Word definition in the IOM control table

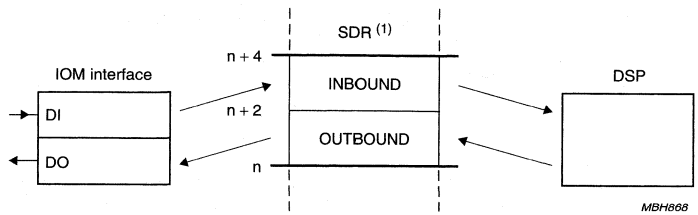
BIT	FUNCTION
B15 to B10	not used
B9	**Mute.** If B9 = 1, data on the DO output is forced to zero regardless of the contents of the IOM data buffer. The input data on DI is not affected. If B9 = 0, then normal operation is selected.
B8	**Local.** If B8 = 1, swap in/out buffers. If B8 = 0, then normal operation is selected. See Section 9.7.
B7	**Select byte.** When byte transfer is selected (B6 = 1); B7 = 1, selects the high byte and B7 = 0 selects the low byte.
B6	**Byte/word transfer.** If B6 = 1, then byte transfer is selected. If B6 = 0, then word transfer is selected and two consecutive slots are activated.
B5	**Active slot.** If B5 = 1, the slot is active. If B5 = 0, the slot is idle.
B4 to B0	**IOM data buffer assigned to the slot.** These 4 bits select the locations in SDR where the IOM data buffer will reside. The allowed values are 10000 to 11101; see Table 31.

Table 31 IOM data buffers location in SDR

IOM BUFFER CODE					ADDRESS IN SDR (HEX)
B4	B3	B2	B1	B0	
1	0	0	0	0	40 to 43
1	0	0	0	1	44 to 47
1	0	0	1	0	48 to 4B
1	0	0	1	1	4C to 4F
1	0	1	0	0	50 to 53
1	0	1	0	1	54 to 57
1	0	1	1	0	58 to 5B
1	0	1	1	1	5C to 5F
1	1	0	0	0	60 to 63
1	1	0	0	1	64 to 67
1	1	0	1	0	68 to 6B
1	1	0	1	1	6C to 6F
1	1	1	0	0	70 to 73
1	1	1	0	1	74 to 77

9.6 IOM data buffers

The address space 40H to 77H in the SDR is reserved for up to 14 IOM data buffers. These buffers are used to exchange data between the IOM-2 interface and the on-chip DSP. Each IOM data buffer consists of four 16-bit words: two words for storing inbound data and two words for outbound data; this is shown in Fig.9



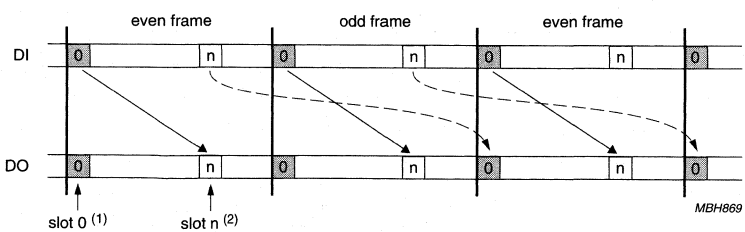
(1) IOM data buffers location is SDR: n = S × 4 with S = B4 to B0 of the corresponding word in the IOM control table.

Fig.9 Data flow between the IOM-2 interface and the DSP.

9.7 Local loop

A local call is implemented in order to loop-back data from one codec to another codec and vice-versa, as illustrated in Fig.10. The inbound and outbound buffer are simply swapped. This is done by setting bit 8 in the correct IOM control table word (see Section 9.5).

A local call is created by assigning one IOM data buffer to 2 codecs, whereby in one IOM control word bit 8 is set, and in the other IOM control word bit 8 is reset.



(1) Bit 8 is set in slot 0 control word.
(2) Bit 8 is reset in slot n control word.

Fig.10 Local call switching on the IOM interface.

10 I²C-BUS INTERFACE

The PCD5096 is programmed by writing to the control registers (CR0 to CR6) and loading the SDR using the I²C-bus interface. The master on the I²C-bus is either a PCD509x DECT processor or an external microcontroller.

The memory map of the PCD5096 is given in Chapter 8. It consists of 128 words (16 bits wide) of system data IOM buffers, IOM control data and DSP parameters) and 7 words (16 bits wide) of control registers mapped at addresses 78H to 7EH.

The I²C-bus interface uses word and byte access to the RAM and to the control registers. For byte access the address is not incremented automatically. For word access the address is incremented after two data bytes (low, high byte) in order to be able to fill the memory without a full I²C-bus protocol (start, slave address, stop bits).

The protocol is shown in Figs 12 to 15. I2C_BYTE = 1, for byte access and I2C_BYTE = 0, for word access. I2C_BSEL = 1 for selecting the high byte and I2C_BSEL = 0 for selecting the low byte. For control registers with less than 8 bits, there is no difference between word access, high byte access and low byte access.

The PCD5096 has two pins (A1 and A0) for programming the slave address. This means that a maximum of four devices can be located on a board without glue logic. The I²C-bus slave address allocated for the PCD5096 is shown in Fig.11.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	1	1	0	A1	A0	

MBH870

Fig.11 PCD5096 I²C-bus slave address.

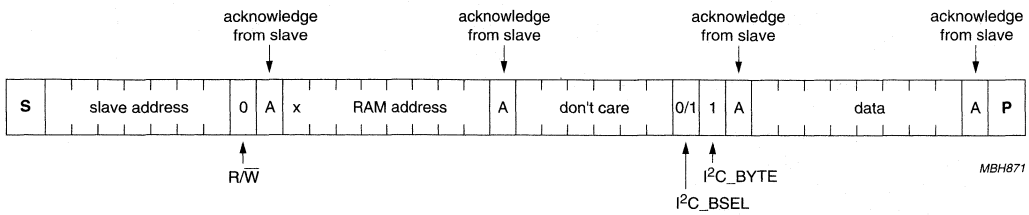


Fig.12 I²C-bus write byte.

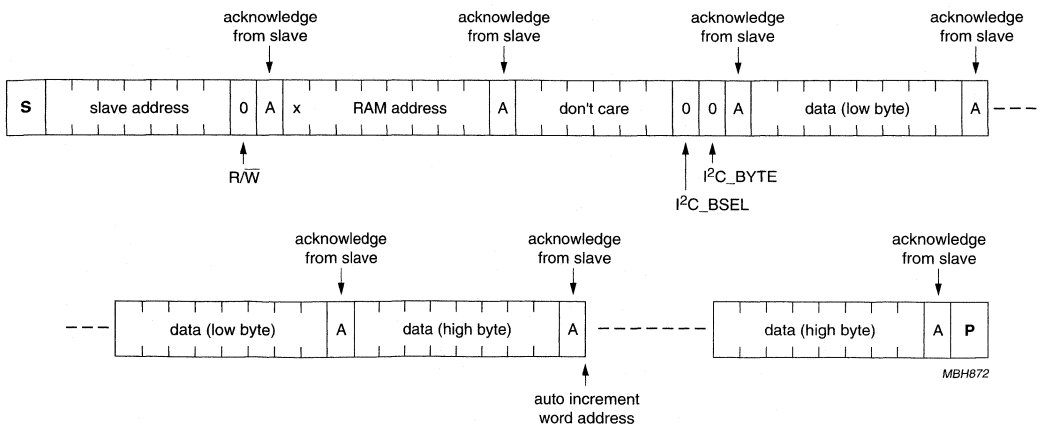


Fig.13 I²C-bus write word.

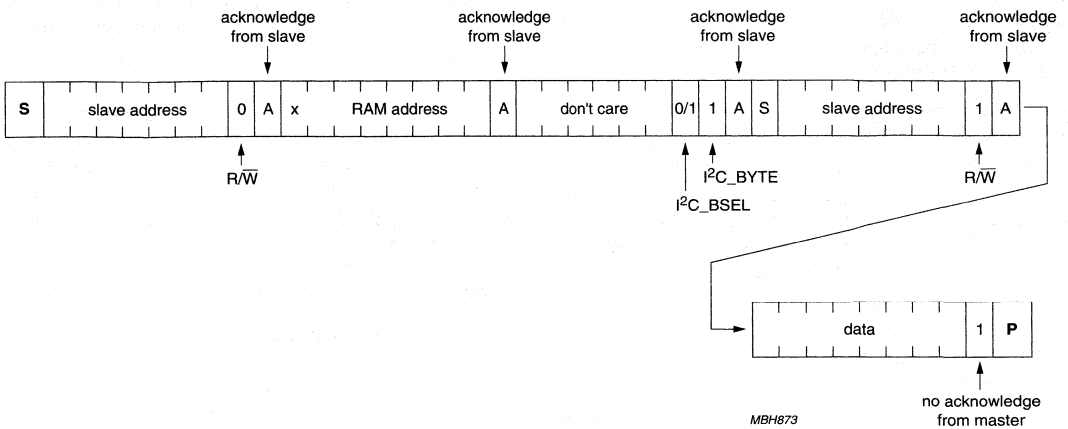


Fig.14 I²C-bus read byte.

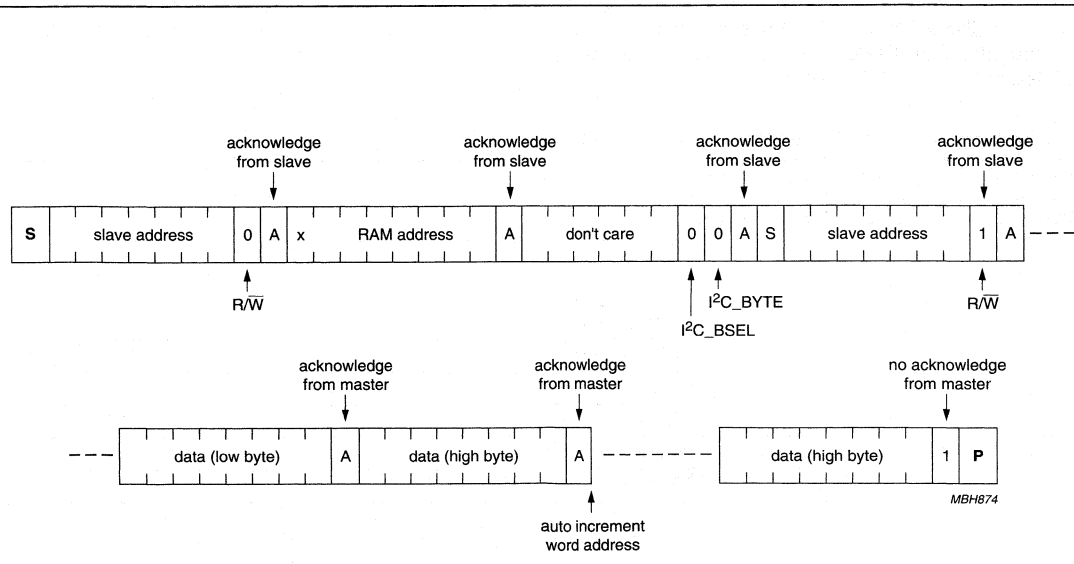


Fig.15 I²C-bus read word.

11 CODEC TEST LOOPS

11.1 Test modes definition

For debug and evaluation purposes some test loops are implemented in the speech codecs. These test loops are activated by setting bits 13 to 8 in Control Register 0; see Table 32. The signal flow in the test loops is shown in Fig.16 and is described as follows:

- **Normal operation**: the codec is not in any of its test loop modes; used for a normal application.
- **1 bit analog**: this loop is intended for a separate evaluation of the analog parts of the codec. A bitstream interface ($108f_s$) is available. Via TEST_INPUT bitstream data is fed to the DAC and bitstream data from the ADC is present on TEST_OUTPUT.
- **1 bit digital**: this loop allows the evaluation of DDF and DNS at the $108f_s$ interface. Bitstream data from TEST_INPUT is led to DDF and bitstream data from DNS is available on TEST_OUTPUT.
- **1 bit closed loop**: a connection between the bitstream output of the ADC and the bitstream input of the DAC is made. The bitstream data is also made available on TEST_OUTPUT.
- **$4f_s$ codec**: the $4f_s$ codec loop gives access to the $4f_s$ interface for evaluation of DDF and DNS. 16-bit input data is serially shifted in (two's complement, MSB first) on TEST_INPUT and the 14 MSBs are used by DNS. On the other side 16 bits DDF output data is serially shifted out on TEST_OUTPUT.
- **$4f_s$ DSP**: this loop allows evaluation of the DSP software. On TEST_INPUT and TEST_OUTPUT, data can be exchanged with the DSP (16 bits serially, 2's complement, MSB first).
- **$4f_s$ closed loop**: a connection between the parallel output of DDF and the input of DNS is made. The loop data at $4f_s$ can be monitored by shifting out bits serially via TEST_OUTPUT.
- **PCM probe**: this special test loop allows the evaluation of DSP software. The DSP software however, must include a test mode in which any 16-bit data at a sample rate of f_s or 8 kHz (normally only present as numbers within the DSP algorithm) is written to the output line that is connected to DNS. While normally the data on this line has a $4f_s$ (32 kHz) sample rate, up to four (interleaved) PCM signals can be monitored via TEST_OUTPUT.

Next to these hardware codec test loops there also may be software DSP test loops, depending on the DSP software version. For more information about the DSP software the DSP manuals must be consulted.

In all codec test loop modes (except the normal operation mode) the signals lines TEST_INPUT_x and TEST_OUTPUT_x (x = 1 for Codec 1, x = 2 for Codec 2) are mapped onto pins that normally have a different function. Next to these data signals some timing signals (FS4 and CLK3) are presented on pins. Table 33 shows which pins are used in the codec test loop modes.

Table 32 Selection of functional test modes for Codec 1 and Codec 2

CDC1TM2	CDC1TM1	CDC1TM0	FUNCTIONAL TEST MODE
CDC2TM2	CDC2TM1	CDC2TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

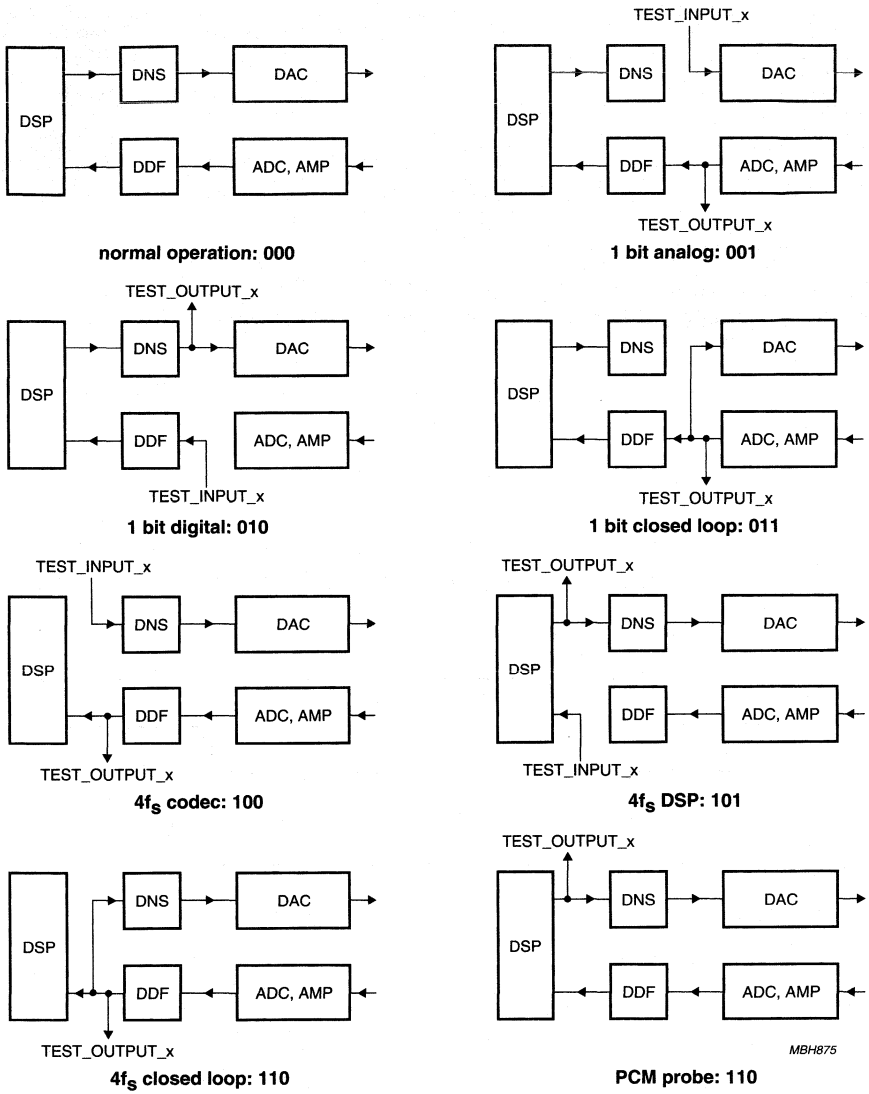


Fig.16 Speech codec test loops.

Table 33 Pin redefinition in Codec test loop mode

NORMAL MODE	CODEC TEST LOOP MODE		
PIN NAME	**SIGNAL NAME**	**I/O**	**DESCRIPTION**
DI	TEST_INPUT_1	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 1
DO	TEST_OUTPUT_1	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 1
A1	TEST_INPUT_2	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 2
IO1	TEST_OUTPUT_2	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 2
DCL	CLK3	O	3456 kHz bit clock signal ($4 \times 108f_s$) with 50% duty cycle
IO0	FS4	O	32 kHz word synchronization signal ($4f_s$), duty cycle = 12/108

11.2 Codec test loop signal timing

The TEST_OUTPUT_x signal changes at the falling edge of CLK3, and the signal presented on TEST_INPUT_x is sampled just before the falling edge of CLK3. Note that the $4f_s$ serial PCM data shifted in via TEST_INPUT_x is only used during the next FS4 HIGH period.

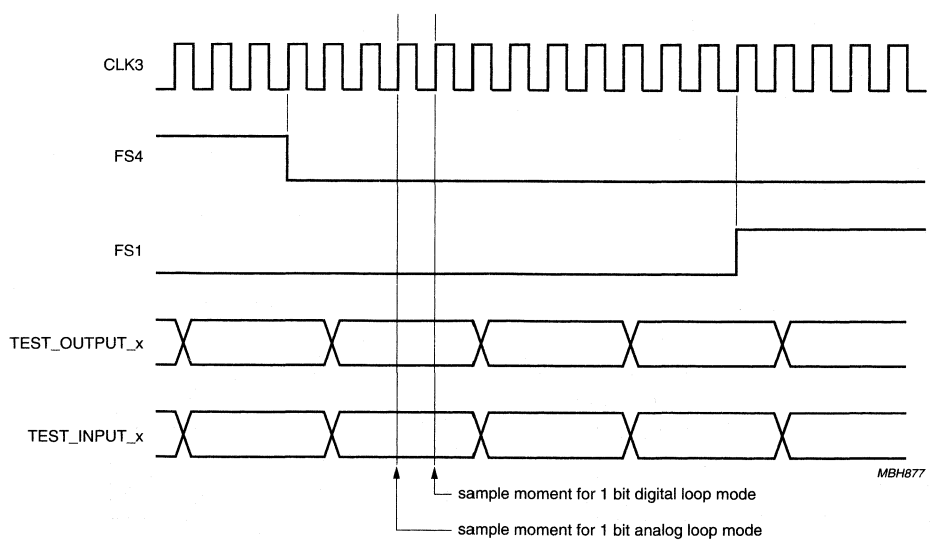


Fig.17 Codec test loop signal timing for $108f_s$ 1-bit bitstream signals.

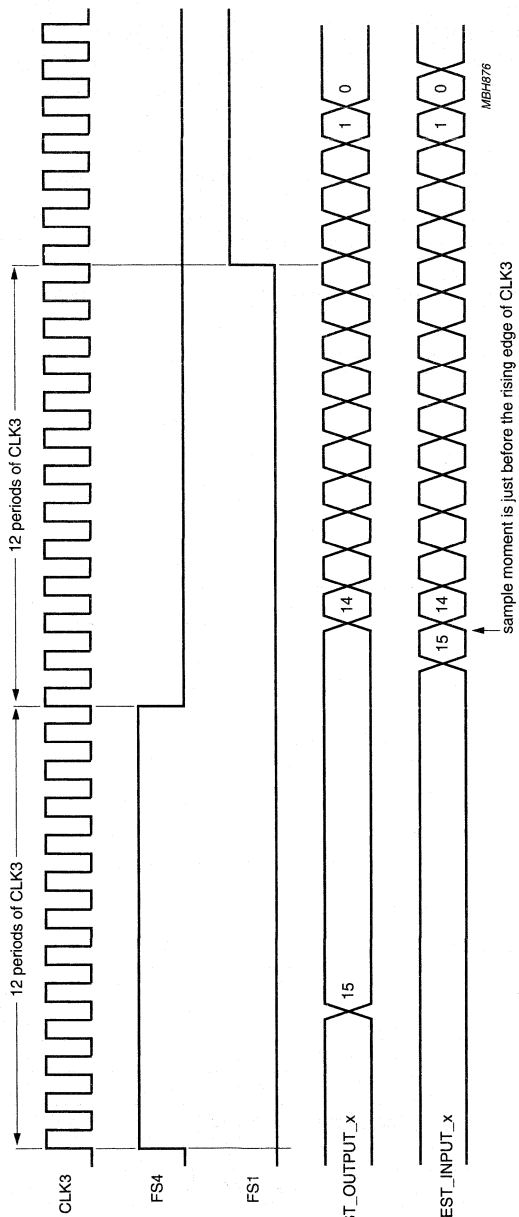


Fig.18 Codec test loop signal timing for $4f_s$ 16-bit serial signals.

12 APPLICATION INFORMATION

12.1 Small business systems

The PCD5096 is designed for business and residential phone systems. In combination with a processor like the PCD5093, two simultaneous calls on 2 PSTN lines (Ba, Bb) can be processed. To realize single line systems with hands-free functionality one analog interface port can be connected to a speaker phone and the other to the line interface. A typical small business system consists of a PCD5093 DECT processor with radio interface and a single universal codec (see Fig.19).

The possible configurations for speech connections in the universal codec are listed in Table 34.

A real hands-free solution can also be implemented by using one PSTN line port and connecting a corded handset, a hands-free microphone and a loudspeaker to the second analog interface port of the universal codec.

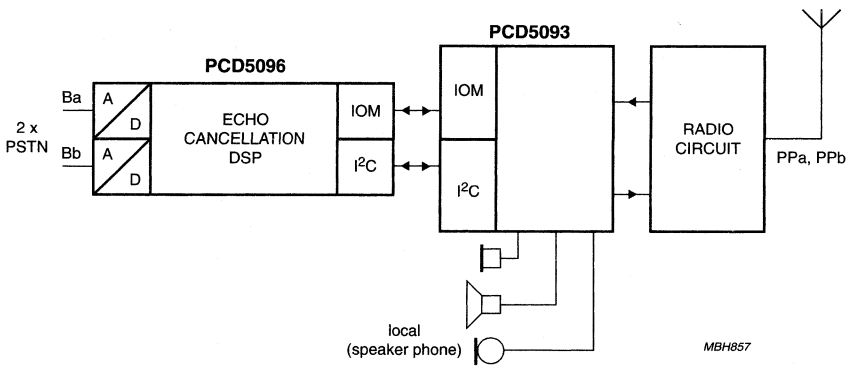


Fig.19 Small business system.

Table 34 Possible speech connections in a small business system

SINGLE CONNECTIONS	DUAL CONNECTIONS	
LOCAL ↔ Ba	(LOCAL ↔ Ba) + (Bb ↔ PPa)	(LOCAL ↔ Ba) + (Bb ↔ PPb)
LOCAL ↔ Bb	(LOCAL ↔ Bb) + (Ba ↔ PPa)	(LOCAL ↔ Bb) + (Ba ↔ PPb)
LOCAL ↔ PPa	(LOCAL ↔ PPa) + (Ba ↔ PPb)	(LOCAL ↔ PPa) + (Bb ↔ PPb)
LOCAL ↔ PPb	(LOCAL ↔ PPb) + (Ba ↔ PPa)	(LOCAL ↔ PPb) + (Bb ↔ PPa)
Ba ↔ PPa	(Ba ↔ PPa) + (Bb ↔ PPb)	–
Ba ↔ PPb	(Ba ↔ PPb) + (Bb ↔ PPa)	–
Bb ↔ PPa	–	–
Bb ↔ PPb	–	–

12.2 Large business systems

For large business systems, local loop and public access systems, several PCD5096 codecs can be connected together utilizing the serial bus system. A digital cordless base station for large business systems typically consists of a baseband processor, radio interface and a number of universal codecs interfacing to local lines, PSTN lines and to the local corded handset/hands-free interface. A diagram of this configuration is shown in Fig.20.

The universal codec can connect to different applications in a typical large business system. They are as follows:

1. PSTN Line Interface
2. Speaker phone with hands-free feature
3. Local Line Interface.

In these applications the additional processing required for conference calling is performed either in the host baseband processor, or in the universal codecs.

For further details about these three applications consult the *"PCD5096 DSP user manual"*.

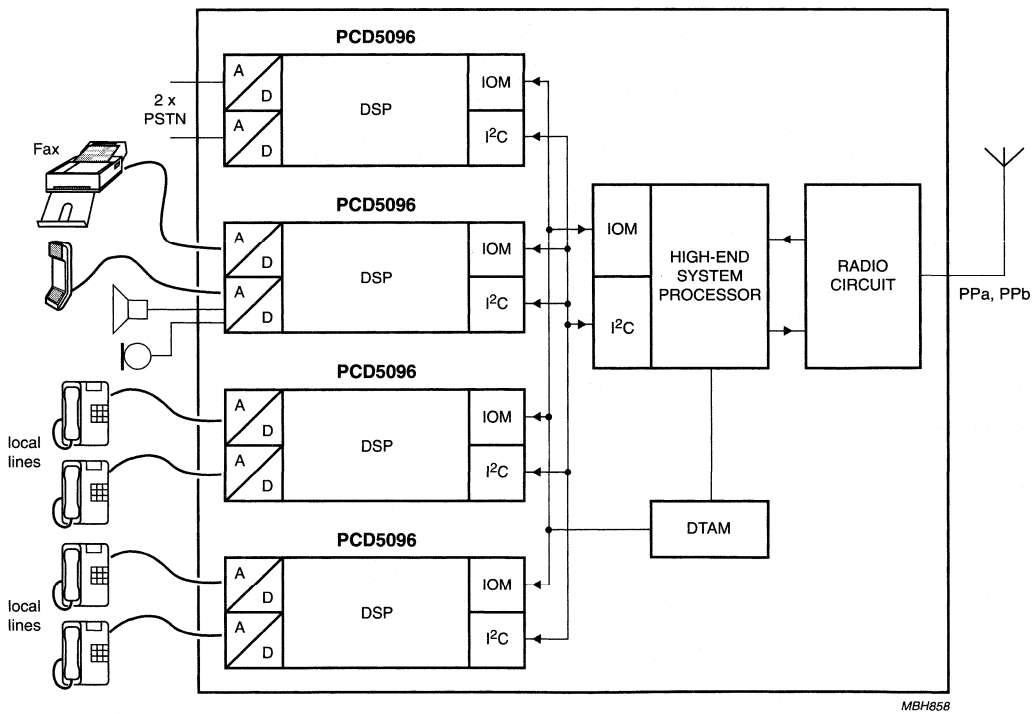


Fig.20 Large business system.

12.3 DECT and ISDN

The PCD5096 is perfectly suited to extend an ISDN-based DECT base station with analog extension lines. The IOM-2 interface communicates with the S0 interface chip. The host controller can connect via IOM-2 or I^2C-bus to the PCD5096. The two analog interfaces of the PCD5096 can either be used to connect to analog phones/Fax machines, or combine hands-free and one analog extension.

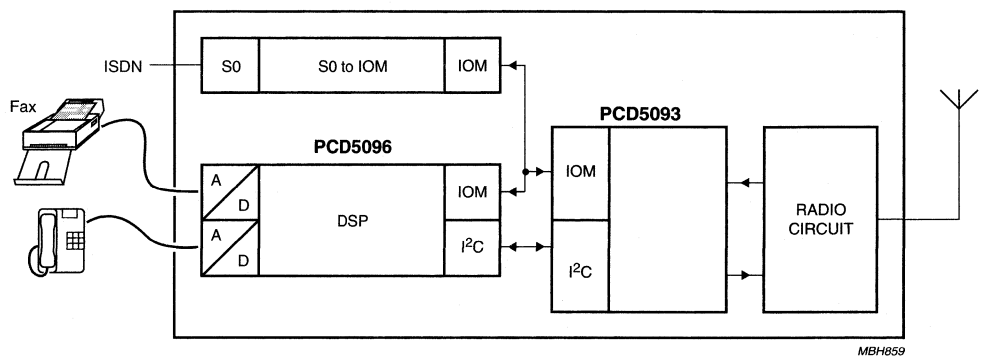


Fig.21 DECT and ISDN.

13 APPLICATION EXAMPLES

In this chapter some application examples are given to assist users with the programming of the PCD5096 (DSP parameter settings, control register settings and IOM-2 interface programming). Three examples are considered: a two channel application, a conference call application between one PSTN line and two IOM buffers, and a conference call application between two PSTN lines and one IOM buffer.

13.1 PCD5096 with two active channels

A typical application for the PCD5096 is depicted in Fig.22. Two handsets (PPa and PPb) are connected through a PCD5093 and a PCD5096 to two PSTN lines. Tables 35, 36 and 37 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the chosen values for the IOM pointers, the volume parameters and the frequency parameters depend on the application. This means that they can differ from the values that are given in this example.

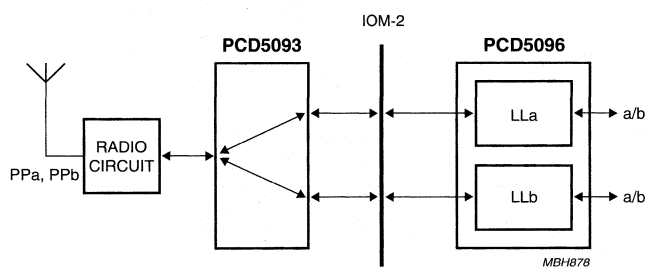


Fig.22 Typical PCD5096 application with two channels.

Table 35 DSP parameters for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	484C	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	4044	Codec 1 uses IOM buffer at address 40H
				Codec 2 uses IOM buffer at address 44H
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0000	no conference call (CCa_IOMx not used)
14	CCa_IOM3	CCa_IOM4	5054	not used
15	CCa_SMU3	CCa_SMU4	0000	not used

Table 36 IOM control table for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2-slot 32	0000	slots 2 to 32 inactive

Table 37 Control registers for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	005B	Codec 1 ON, Codec 2 ON
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

13.2 Conference call between one PSTN line and two IOM buffers

The PCD5096 is able to perform a 3 party conference call. Figure 23 shows a typical configuration, with two handsets in conference call with an PSTN line. Tables 38, 39 and 40 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the LLb block of the PCD5096 could be used in parallel to connect a second PSTN line to another IOM buffer. This is not covered in this example.

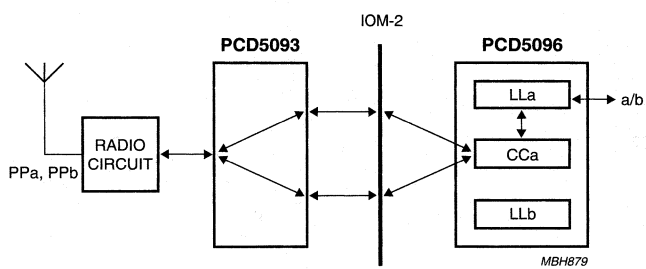


Fig.23 Conference call between one PSTN line and two IOM buffers.

Table 38 DSP parameters for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FF00	LLa analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FF00	Local Echo Canceller ON in Codec 1
03	LLa_NES	LLb_NES	2D00	Network Echo Suppressor (9 dB attenuation) in Codec 1
04	LLa_AGC	LLb_AGC	FF00	Automatic Gain Control ON in Codec 1
05	LLa_TXV	LLb_TXV	2000	Transmit Volume set to 0 dB in Codec 1
06	LLa_ISW	LLb_ISW	0000	8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2000	Receive Volume set to 0 dB in Codec 1
0B	LLa_PST	LLb_PST	0000	Site Tone OFF
0C	LLa_TST	LLb_TST	0000	Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0900	conference call between Codec 1 and Codec 2 IOM buffers (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call IOM buffer 1 at address 40H
				conference call IOM buffer 2 at address 44H
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 39 IOM control table for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2 to slot 32	0000	slots 2 to 32 inactive

Table 40 Control registers for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	0003	Codec 1 ON, Codec 2 OFF
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	00D0	A/D gain = +9 dB, D/A gain = 0 dB in Codec 1
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0008	channel a in speech and tone mode

13.3 Conference call between two PSTN lines and one IOM buffer

Another configuration for conference call is between two PSTN lines and one IOM buffer, as shown in Fig.24. Tables 41, 42 and 43 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

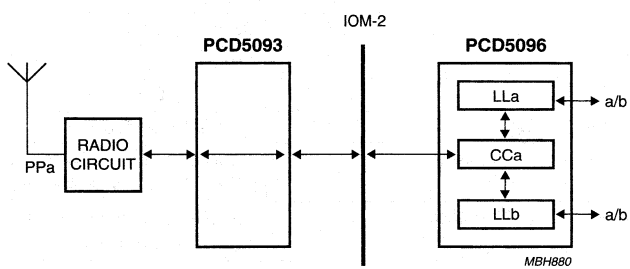


Fig.24 Conference call between two PSTN lines and one IOM buffer.

Table 41 DSP parameters for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0100	conference call between Codec 1, Codec 2 and one IOM buffer (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call with IOM buffer at address 40H CCa_IOM4 not used
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 42 IOM control table for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21 to 3F	slot 1 to slot 32	0000	slots 1 to 32 inactive

Table 43 Control registers for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	00FB	Codec 1 ON, Codec 2 ON with hands-free
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

14 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD_1}	supply voltage V_{DD_1} with respect to V_{SS_1}	−0.5	+6.0	V
V_{DD_2}	supply voltage V_{DD_2} with respect to V_{SS_2}	−0.5	+5.0	V
V_{DDA_1}	analog supply voltage V_{DDA_1} with respect to V_{SSA_1}	−0.5	+5.0	V
V_{DDA_2}	analog supply voltage V_{DDA_2} with respect to V_{SSA_2}	−0.5	+5.0	V
V_{DD_PLL}	supply voltage V_{DD_PLL} with respect to V_{SS_PLL}	−0.5	+5.0	V
I_{DC}	DC current through pins			
	supply pins	−	150	mA
	other pins	−	10	mA
P_{tot}	total power dissipation	−	500	mW
T_{amb}	operating ambient temperature	−25	+70	°C
T_{stg}	storage temperature	−65	+150	°C

15 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 2 kV. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

16 ELECTRICAL SPECIFICATIONS

Table 44 General parameters

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency		–	6.912	–	MHz
T_{amb}	ambient temperature		–25	+25	+70	°C
V_{DD_1}	supply voltage	note 1	2.7	3.3	5.5	V
$I_{DD\_1(act)}$	active supply current	note 2	–	–	–	mA
$I_{DD\_1(off)}$	power off supply current	note 3	–	0.1	–	µA
V_{DD_2}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_2(act)}$	active supply current	note 5	–	18	28	mA
$I_{DD\_2(off)}$	power off supply current	note 3	–	4	–	µA
V_{DDA_1}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_1(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_1(off)}$	power off supply current	note 3	–	33	–	µA
V_{DDA_2}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_2(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_2(off)}$	power off supply current	note 3	–	2	–	µA
V_{DD_PLL}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_PLL(act)}$	active supply current	note 5	–	0.1	1	mA
$I_{DD\_PLL(off)}$	power off supply current	note 3	–	1	–	µA
$I_{DD(tot)(off)}$	total power off supply current	note 3	–	40	70	µA

Notes

1. V_{DD_1} supplies all digital I/Os to ensure 5 V interfacing. V_{DD_1} may vary over its range independent of the value of V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL}. If V_{DD_1} is 5.5 V, V_{DD_2} cannot be lower than 3.0 V.
2. $I_{DD\_1(act)}$ is application dependent.
3. Power off at 25 °C and 3.3 V, RESET pin HIGH, clock not running. The pins IO0 and IO1 are then inputs and must be kept HIGH (internal pull-ups).
4. V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL} will have the same value. Internally they are NOT connected.
5. Active mode at 25 °C and 3.3 V, clock running. DSP parameter table, IOM control table and control registers set according to Section 13.1 (application example with two active channels). A sine wave signal (1031.25 Hz) at a level of –25 dBm is applied to the microphone input of both codecs. DI is tied to DO to simulate activity on the IOM-2 interface.
6. No load on LIFM_DA1, LIFP_DA1, EARM_HS, EARP_HS, VBGP, VREF1, VREF2, VMIC_HS and VMIC_HF.

Table 45 Digital I/Os

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	leakage current input pins		–	–	1	μA
V_{IH}	HIGH-level input voltage		$0.7V_{DD\_1}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD\_1}$	V
V_{OH}	HIGH-level output voltage	note 1	$0.8V_{DD\_1}$	–	–	V
V_{OL}	LOW-level output voltage	notes 2 and 4	–	–	0.4	V
R_{pd}	equivalent pull-down resistor	note 3	–	50	–	kΩ
R_{pu}	equivalent pull-up resistor	note 3	–	100	–	kΩ
$t_{o(f)}$	SDA output fall time	notes 4 and 5	–	–	250	ns

Notes

1. I_{OH} = −8 mA for pins EARM_HF and EARP_HF. I_{OH} = −2 mA for pins IO0 and IO1.
2. I_{OL} = 8 mA for pins EARM_HF, EARP_HF and DO. I_{OL} = 2 mA for pins IO0 and IO1.
3. Pull-down resistor present at pin TEST. Pull-up resistor present at pins IO0 and IO1.
4. For SDA pin, I_{OL} = 3 mA at 5 V, 1 mA at 3.3 V and 0.7 mA at 2.7 V.
5. Output fall time of SDA measured from $V_{IH(min)}$ to $V_{IL(max)}$.

Table 46 Analog supplies

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{bgp}	bandgap voltage	note 1	1	1.2	1.5	V
V_{ref}	reference voltage	notes 2 and 3	1.975	2.000	2.025	V
R_{vmic}	microphone supply output resistance	note 4	–	75	150	Ω

Notes

1. VBGP output current is zero. Decoupling capacitance between pins VBGP and V_{SSA_1} is 100 nF at 25 °C. The bandgap has a temperature coefficient between −0.2 and +0.2 mV/°C.
2. V_{ref} stands for VREF1 or VREF2. V_{ref} output current is zero. Decoupling capacitance between VREF1 and V_{SSA_1}, or between VREF2 and V_{SSA_2} is between 1 μF and 100 μF, with a 100 nF capacitance in parallel. The voltage is programmed by setting the appropriate value (80H to BFH) for each codec, in Control Register 3. VMIC_HS and VMIC_HF output current is zero (e.g. by setting bits 6 and 7 in Control Register 3 to a logic 0. The output can only source current (i.e. not sink).
3. Pins VMIC_HS and VMIC_HF (called VMIC below) are internally connected to VREF2 via two switches. The VMIC_HS switch is closed by setting the HSMICON bit in Control Register 0 to a logic 1. The VMIC_HF switch is closed by setting the HFMICON bit in Control Register 0 to a logic 1. The VMIC DC output current is 400 μA maximum, and VREF2 must be programmed to its typical value. Use a low pass filter (resistor + capacitor) between VMIC and V_{SSA_2} of 100 Ω + 10 μF, with a 100 nF capacitance in parallel. VMIC adjustment can only be done by adjusting VREF2.
4. Valid for both VMIC_HS and VMIC_HF pins.

Table 47 Speech codec

V_{ref1} and V_{ref2} are tuned to 2.0 V. Typical values for the A/D and D/A filter characteristics conform to the G.712 specification.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(MIC1)}$	MIC input level (Codec 1)	note 1	–	–	–22	dBm
$V_{i(MIC\_HS)}$	handset MIC input level (Codec 2)	note 1	–	–	–22	dBm
$V_{i(MIC\_HF)}$	hands-free MIC input level (Codec 2)	note 1	–	–	–22	dBm
$R_{i(MIC1)(dm)}$	MIC input resistance differential mode seen across MICP1 and MICM1		–	200	–	kΩ
$R_{i(MIC\_HS)(dm)}$	handset MIC input resistance differential mode seen across MICP_HS and MICM_HS		–	200	–	kΩ
$R_{i(MIC\_HF)(dm)}$	hands-free MIC input resistance differential mode seen across MICP_HF and MICM_HF		–	200	–	kΩ
$R_{i(MIC1)(cm)}$	MIC input resistance common mode seen between MICP1 (or MICM1) and V_{SSA_1}		–	500	–	kΩ
$R_{i(MIC\_HS)(cm)}$	handset MIC input resistance common mode seen between MICP_HS (or MICM_HS) and V_{SSA_2}		–	500	–	kΩ
$R_{i(MIC\text{-}HF)(cm)}$	hands-free MIC input resistance common mode seen between MICP_HF (or MICM_HF) and V_{SSA_2}		–	500	–	kΩ
$V_{i(LIF\_AD1)}$	LIF input level (Codec 1)	note 2	–	–	–6	dBm
$V_{i(LIF\_AD2)}$	LIF input level (Codec 2)	note 2	–	–	–6	dBm
$R_{i(LIF\_AD1)(dm)}$	LIF input resistance differential mode seen across LIFP_AD1 and LIFM_AD1		–	30	–	kΩ
$R_{i(LIF\_AD2)(dm)}$	LIF input resistance differential mode seen across LIFP_AD2 and LIFM_AD2		–	30	–	kΩ
$R_{i(LIF\_AD1)(cm)}$	LIF input resistance common mode seen between LIFP_AD1 (or LIFM_AD1) and V_{SSA_1}		–	15	–	kΩ
$R_{i(LIF\_AD2)(cm)}$	input resistance common mode seen between LIFP_AD2 (or LIFM_AD2) and V_{SSA_2}		–	15	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$F_{(A/D)(idle)}$	A/D idle channel noise	note 3	–	–85	–72	dBm0p
$S/(N + THD)_{(A/D)(65)}$	A/D signal-to-noise plus total harmonic distortion ratio (–65 dBm input level)	note 4	32	40	–	dBp
$S/(N + THD)_{(A/D)(25)}$	A/D signal-to-noise plus total harmonic distortion ratio (–25 dBm input level)	note 4	40	60	–	dBp
$t_{d(g)(A/D)}$	A/D path group delay		–	500	–	µs
$G_{(MIC1)}$	Codec 1 MIC gain from MICP1 - MICM1 to LIFP_AD1 - LIFM_AD1		12	15	18	dB
$G_{(MIC\_HS)}$	Codec 2 handset MIC gain from MICP_HS - MICM_HS to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(MIC\_HF)}$	Codec 2 hands-free MIC gain from MICP_HF - MICM_HF to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(A/D)}$	gain A/D path from LIF to PCM	note 5	$G_{AD} - 1.5$	G_{AD}	$G_{AD} + 1.5$	dB
$G_{step(A/D)}$	gain difference between adjacent steps (A/D path)	note 6	+0.1	+1.0	+1.9	dB
$G_{(D/A)}$	gain D/A path from PCM to LIF	note 7	$G_{DA} - 1$	G_{DA}	$G_{DA} + 1$	dB
$G_{step(D/A)}$	gain difference between adjacent steps (D/A path)	note 6	+0.5	+1.0	+1.5	dB
$V_{o(D/A)}$	D/A path output level	note 8	–	1350	–	mV
$R_{o(D/A\_1)}$	D/A path output resistance seen between LIFP_DA1 and LIFM_DA1		–	10	20	Ω
$R_{o(D/A\_2)}$	D/A path output resistance seen between EARP_HS and EARM_HS		–	10	20	Ω
$F_{(D/A)(idle)}$	D/A idle channel noise	note 9	–	–85	–72	dBmp
$S/(N + THD)_{(D/A)(40)}$	D/A signal-to-noise plus total harmonic distortion ratio (–40 dBm0 input level)	note 10	32	40	–	dBp
$S/(N + THD)_{(D/A)(0)}$	D/A signal-to-noise plus total harmonic distortion ratio (0 dBm0 input level)	notes 10 and 11	40	70	–	dBp
$t_{d(g)(D/A)}$	D/A-path group delay		–	500	–	µs

Notes

1. A sine wave rms level applied differentially between the microphone pins. The A/D path gain in Control Register 2 is set to +9 dB. For larger input levels the output signal will saturate.
2. A sine wave rms level applied differentially between pins LIFP_ADn and LIFM_ADn (n = 1 for Codec 1; n = 2 for Codec 2). The A/D path gain is set to +9 dB using Control Register 2. For larger input levels the output signal will saturate.
3. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. The microphone pins are shorted together. The value is psophometrically weighted.
4. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. A sine wave of 1030 Hz is applied between the microphone input pins. The value is psophometrically weighted and includes harmonic distortion.
5. Valid for Codec 1 and Codec 2. G_{AD} is the A/D gain value selected in Control Register 2. The gain is measured at 1030 Hz from the LIF interface (pins LIFP_ADn and LIFM_ADn, where n = 1 for Codec 1 and n = 2 for Codec 2) to the PCM interface.
6. The difference between two adjacent gain settings as specified in Control Register 2. Valid for Codec 1 and Codec 2.
7. Valid for Codec 1 and Codec 2. G_{DA} is the D/A gain value selected in Control Register 2. The gain is measured at 970 Hz, from the PCM interface to the LIF interface (pins LIFP_DA1 and LIFM_DA1, for Codec 1 and pins EARP_HS and EARM_HS for Codec 2).
8. Valid for Codec 1 and Codec 2. Sine wave rms level differentially seen between pins LIFP_DA1 and LIFM_DA1 (Codec 1) or EARP_HS and EARM_HS (Codec 2), with an input signal of 970 Hz and a level of +3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω. The D/A path gain in Control Register 2 is set to +2 dB.
9. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2). The D/A path gain in Control Register 2 is set to 0 dB and the DSP is set to idle mode. The value is psophometrically weighted.
10. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2).The D/A path gain in Control Register 2 is set to 0 dB. A sine wave of 970 Hz is applied. The value is psophometrically weighted and includes harmonic distortion.
11. The D/A path is loaded with (150 Ω + 800 μF)//100 pF.

Low cost; low power DECT baseband controllers (ABC-PRO)

PCD509x2/zuu/v family

CONTENTS

Low cost; low power DECT baseband controllers (ABC-PRO)

PCD509x2/zuu/v family

1 FEATURES

- The PCD50912 is designed for GAP compatible DECT handsets
- The PCD50922 is designed for GAP compatible DECT base stations serving up to six handsets
- Fully static 80C51 microcontroller
- Emulation supported for 80C51 program development
- Four 8-bit ports (P0, P1, P2 and P3), 32 I/O lines
- Dedicated port pins for keyboard, I²C-bus, interrupt sources and/or external memory
- Fifteen interrupt sources (including those from TICB, BML and DSP) with two priority levels
- I²C-bus interface
- UART with IrDA-compatible Data Transmission Mode
- 256 bytes of microcontroller main RAM
- 3 kbytes of microcontroller AUX RAM
- 1 kbyte of shared System Data RAM
- 64 kbytes of mask programmable ROM
- 128 kbyte address space for external ROM access, maximum 192 kbytes together with internal ROM
- 128 kbytes of external RAM addressable
- Embedded DSP with 6.912, 13.824 or 27.648 Mips
- Speech and IOM-2 interface
- BML for TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation, protected B-fields
- Local call and B-field loop-back
- Automatic receiver delay adjustment programmable per slot to correct for terminal mobility
- Phase error measurement and phase error correction by hardware
- Serial interface to synthesizer for frequency programming
- Programmable timing and polarity of radio-control signals
- Easy interfacing with radio circuits, operating at different supply voltages
- GMSK pulse shaper with two different pulse shapes (BT = 0.5 and BT = 0.8)
- Comparator for use as bit-slicer
- 3 channel time-multiplexed 8-bit ADC for RSSI, battery and general input voltage measurement
- Battery management supported by programmable current source for temperature or charge current measurement
- On-chip 8-bit DAC for various purposes
- Low power crystal oscillator at 13.824 MHz
- Programmable on-chip capacitors for frequency adjustment to 13.824 MHz with large pulling range
- High performance DAC and ADC for dynamic earpiece and dynamic or electret microphone
- Analog-to-digital path switchable sensitivity for microphone or line interface input
- On-chip reference voltage and supply for electret microphone
- Very low ohmic buzzer output
- Pulse density modulated or pulse width modulated buzzer output signal
- Power-on-reset
- Low power operation optimized for 2 battery cells in handset
- Long standby time due to reduced digital supply voltage and reduced activity in idle-locked mode
- Flexible supply voltage concept due to use of level shifters between each supply voltage domain
- Eight independent supply voltage domains:
  - 1.8 to 3.6 V for digital core, microcontroller ports P0 and P2, and also P1 and P3
  - 1.8 to 3.6 V for buzzer, oscillator and battery
  - 2.7 to 3.6 V for RF interface and analog circuits
- CMOS technology
- Small and flat LQFP80 package.

2 GENERAL DESCRIPTION

The PCD509x2 family is designed for low power GAP compatible DECT handset (PP) and base station (FP) applications. The circuit includes the audio interface, the DSP, the microcontroller and the Burst Mode Logic, and contains all functionality to convert speech and data signals from/to the analog side (microphone and earpiece or line interface circuit) to/from the radio side (1.152 Mbits/s data).

This circuit is a member of the ABC family, where A stands for 'ADPCM codec', B for 'Burst Mode Logic' and C for 'microController'. The name ABC-PRO stands for PROfessional ABC.

The PCD509x2/zuu/v contains on-chip ROM for the embedded DSP code and on-chip ROM for the embedded microcontroller code. It is these ROM codes that differentiate between various chip derivatives. For each DSP code a separate DSP user manual is published. Please contact Philips Semiconductors for more information.

This family specification contains the hardware description that is independent of the used ROM codes.

The numerical digit 'x' in PCD509x2 determines the intended application area (e.g. PCD50912 for use in handsets or PCD50922 for use in simple base stations, etc.). The last numerical digit '2' is used to denote hardware derivatives. The extension digits 'z' (A to Z) and 'uu' (00 to 99) denote the DSP and the microcontroller software version, respectively. The extension 'v' denotes the hardware version updates of the circuit.

Although the microcontroller ROM code is present on-chip, an external program memory for the microcontroller code can be used. This is not the case for the DSP ROM code which is fixed by the chip version.

Throughout this family specification the term PCD509x2 is used to cover all sub types and versions. If any specific feature or parameter is connected to a certain sub type or version this will be specifically written. Until otherwise stated this family specification is valid for hardware version 1 (v = 1).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD50912H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
PCD50922H			

4 BLOCK DIAGRAM

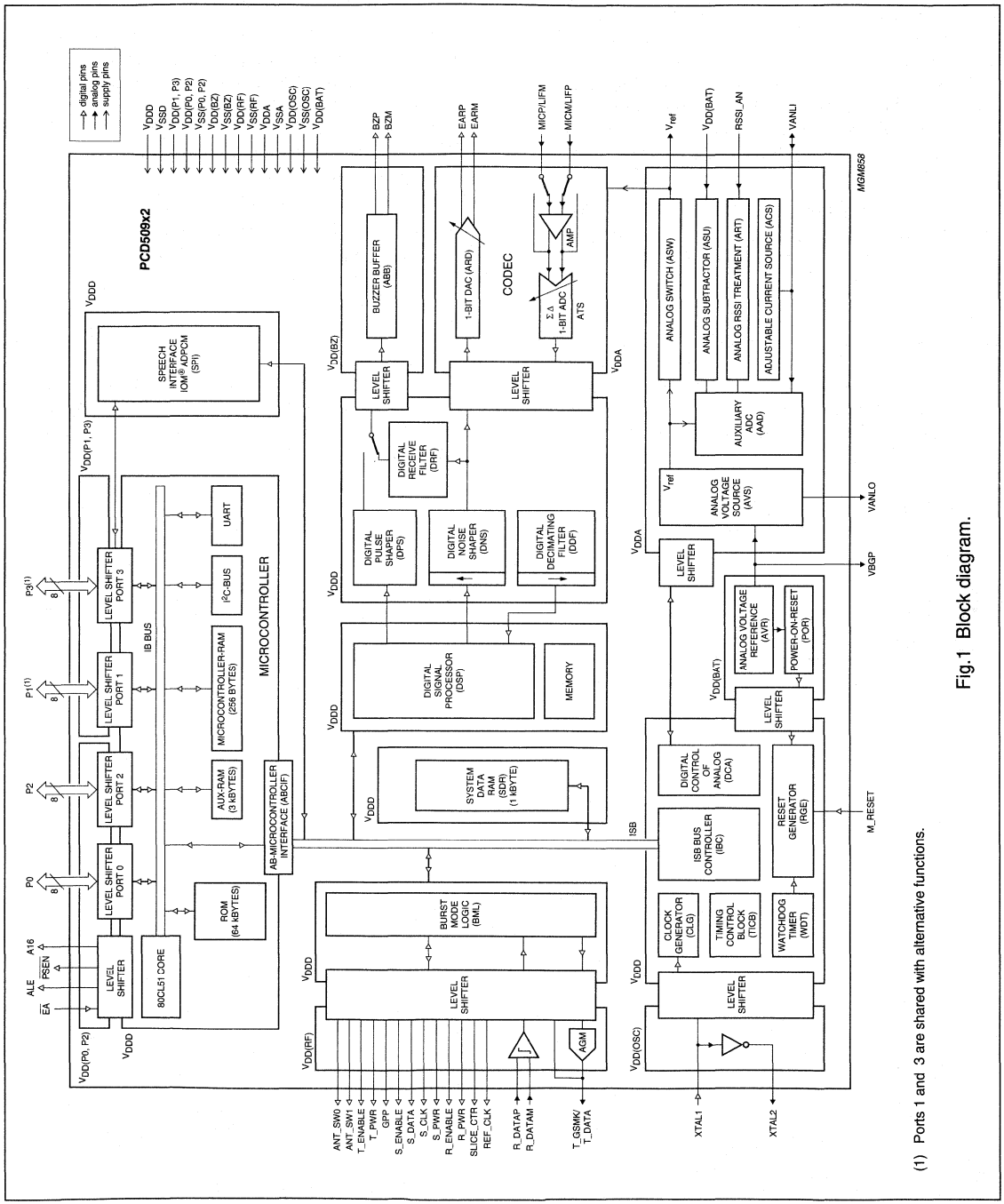


Fig.1 Block diagram.

(1) Ports 1 and 3 are shared with alternative functions.

5 PINNING INFORMATION

5.1 Pinning

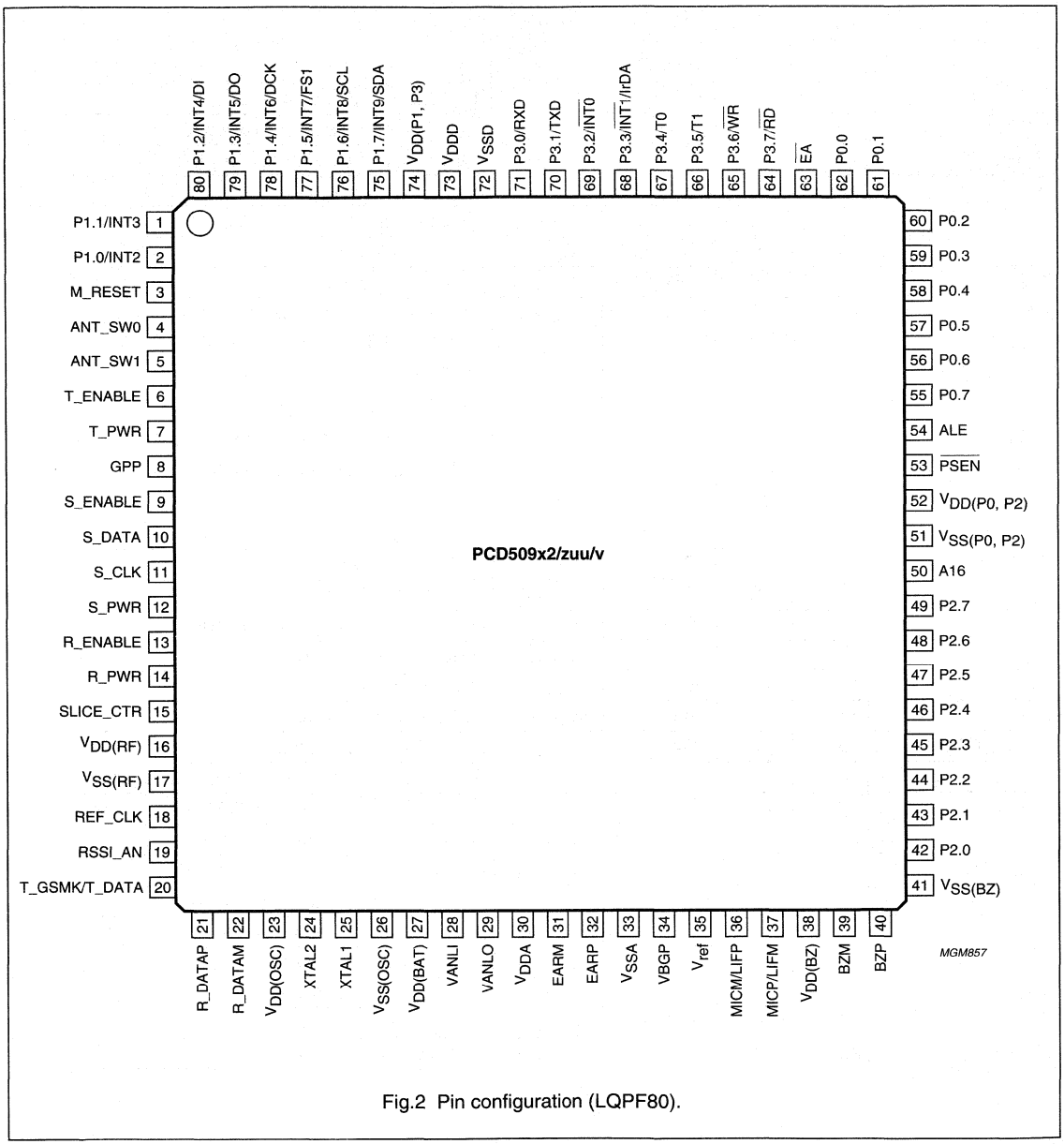


Fig.2 Pin configuration (LQPF80).

5.2 Pin description

Table 1 LQFP80 package

SYMBOL	PIN	I/O	STATE AFTER RESET[1]	SUPPLY DOMAIN	DESCRIPTION
P1.1/INT3	1	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 3
P1.0/INT2	2	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 2
M_RESET	3	I	–	V_{DDD}	master reset input (Schmitt trigger)
ANT_SW0	4	O	HIGH	$V_{DD(RF)}$	antenna switch 0
ANT_SW1	5	O	HIGH	$V_{DD(RF)}$	antenna switch 1
T_ENABLE	6	O	HIGH	$V_{DD(RF)}$	enable transmitter
T_PWR	7	O	LOW	$V_{DD(RF)}$	switch transmitter power
GPP CLK100 VCO_BND_SW GP_CLK7 GP_CLK3 GP_CLK05 R_SLICED on/of	8	O	LOW	$V_{DD(RF)}$	general purpose pin used for the following: 100 Hz signal related to DECT frame timing VCO band switch 6.912 MHz general purpose clock 3.456 MHz general purpose clock 576 kHz general purpose clock ABS bitslice comparator output static high/low.
S_ENABLE	9	O	LOW	$V_{DD(RF)}$	synthesizer enable
S_DATA	10	O	LOW	$V_{DD(RF)}$	serial synthesizer data
S_CLK	11	O	LOW	$V_{DD(RF)}$	clock for serial synthesizer interface
S_PWR	12	O	LOW	$V_{DD(RF)}$	switch synthesizer power
R_ENABLE	13	O	HIGH	$V_{DD(RF)}$	enable receiver
R_PWR	14	O	HIGH	$V_{DD(RF)}$	switch receiver power
SLICE_CTR	15	O	LOW	$V_{DD(RF)}$	switch slicer time constant
$V_{DD(RF)}$	16	–	–	–	positive supply voltage for RF interface pins
$V_{SS(RF)}$	17	–	–	–	negative supply voltage for RF interface pins
REF_CLK	18	O	running	$V_{DD(RF)}$	programmable reference clock for synthesizer
RSSI_AN	19	I	–	$V_{DD(RF)}$	analog input for RSSI measurement
T_GMSK/T_DATA	20	O	off	$V_{DD(RF)}$	transmitter data output, filtered/digital
R_DATAP	21	I	–	$V_{DD(RF)}$	positive input for receiver data
R_DATAM	22	I	–	$V_{DD(RF)}$	negative input for receiver data
$V_{DD(OSC)}$	23	–	–	–	positive supply for crystal oscillator
XTAL2	24	O	running	$V_{DD(OSC)}$	crystal oscillator output
XTAL1	25	I	–	$V_{DD(OSC)}$	crystal oscillator input

SYMBOL	PIN	I/O	STATE AFTER RESET[1]	SUPPLY DOMAIN	DESCRIPTION
$V_{SS(OSC)}$	26	–	–	–	negative supply for crystal oscillator
$V_{DD(BAT)}$	27	I	–	–	positive battery supply voltage
VANLI	28	I/O	–	V_{DDA}	analog input to ADC, current output
VANLO	29	O	off	V_{DDA}	analog output from DAC
V_{DDA}	30	–	–	–	positive supply voltage for analog circuits
EARM	31	O	off	V_{DDA}	negative output to earpiece
EARP	32	O	off	V_{DDA}	positive output to earpiece
V_{SSA}	33	–	–	–	negative supply voltage for analog circuits
VBGP	34	O	1.2 V	$V_{DD(BAT)}$	bandgap output voltage (+1.2 V)
V_{ref}	35	O	off	V_{DDA}	reference voltage, microphone supply (+2 V)
MICM/LIFP	36	I	off	V_{DDA}	negative/positive input from microphone/line
MICP/LIFM	37	I	off	V_{DDA}	positive/negative input from microphone/line
$V_{DD(BZ)}$	38	–	–	–	positive supply voltage for buzzer
BZM	39	O	LOW	$V_{DD(BZ)}$	negative buzzer output
BZP	40	O	LOW	$V_{DD(BZ)}$	positive buzzer output
$V_{SS(BZ)}$	41	–	–	–	negative supply voltage for buzzer
P2.0	42	I/O	HIGH	$V_{DD(P0,P2)}$	bidirectional Port 3 pins (80C51)
P2.1	43	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.2	44	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.3	45	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.4	46	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.5	47	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.6	48	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.7	49	I/O	HIGH	$V_{DD(P0,P2)}$	
A16	50	O	LOW	$V_{DD(P0,P2)}$	A16 address select
$V_{SS(P0,P2)}$	51	–	–	–	negative supply voltage
$V_{DD(P0,P2)}$	52	–	–	–	positive supply voltage for periphery pins
$\overline{PSEN}$	53	O	HIGH	$V_{DD(P0,P2)}$	program store enable (80C51), active LOW
ALE	54	O	HIGH	$V_{DD(P0,P2)}$	address latch enable (80C51)
P0.7	55	I/O	HIGH	$V_{DD(P0,P2)}$	bidirectional Port 0 pins (80C51)
P0.6	56	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.5	57	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.4	58	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.3	59	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.2	60	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.1	61	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.0	62	I/O	HIGH	$V_{DD(P0,P2)}$	

SYMBOL	PIN	I/O	STATE AFTER RESET[1]	SUPPLY DOMAIN	DESCRIPTION
$\overline{EA}$	63	I	–	$V_{DD(P0,P2)}$	external access (80C51), active LOW
P3.7/$\overline{RD}$	64	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Read data, active LOW
P3.6/$\overline{WR}$	65	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Write data, active LOW
P3.5/T1	66	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Timer 1 input
P3.4/T0	67	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Timer 0 input
P3.3/$\overline{INT1}$/IrDA	68	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 1/IrDA clock
P3.2/$\overline{INT0}$	69	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 0
P3.1/TXD	70	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/UART transmit data
P3.0/RXD	71	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/UART receive data
V_{SSD}	72	–	–	–	negative supply voltage for digital core
V_{DDD}	73	–	–	–	positive supply voltage for digital core
$V_{DD(P1,P3)}$	74	–	–	–	positive supply voltage for periphery pins
P1.7/INT9/SDA	75	I/O	off	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 9/I^2C-bus data
P1.6/INT8/SCL	76	I/O	off	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 8/I^2C-bus clock
P1.5/INT7/FS1	77	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 7/SPI Frame Sync
P1.4/INT6/DCK	78	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 6/SPI Data Clock
P1.3/INT5/DO	79	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 5/SPI Data Out
P1.2/INT4/DI	80	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 4/SPI Data In

Note

1. In the 'State After Reset' column the following symbols are used:
   a) HIGH means active HIGH, for BUPxSW pin types this means weak pull-up
   b) LOW means active LOW
   c) 'running' means the clock signal is active
   d) 'off' means the high-impedance state.

6 FUNCTIONAL DESCRIPTION

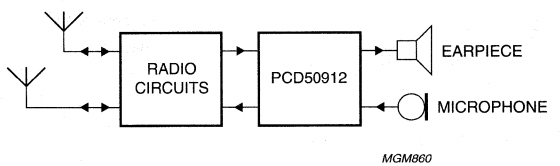
6.1 DECT baseband controller system

The PCD509x2 is a family of baseband controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimal component-count and minimal power consumption for very long standby times. All baseband controllers include an embedded 80C51 microcontroller with on-chip memory, including an IrDA (Infrared Data Association) compatible UART and I^2C-bus. The Burst Mode Logic performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The implemented RF Interface is compatible with the Philips Burst Mode Controller PCD504x. The ADPCM transcoding is in compliance with the CCITT Recommendation G.726. Also included is an on-chip codec with receive and transmit filters, complying with CCITT Recommendation G.712. Power-on-reset logic and power management functions further reduce power consumption and external components.

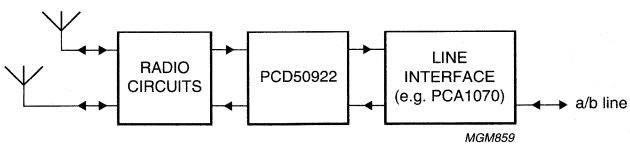
The chip is intended to support stand-alone systems only (see Fig.3). There are no provisions to build clusters of base stations. There are no provisions for external controllers to exert control over the embedded 80C51. There are no provisions for external controllers to have direct access to the on-chip data memories. There are no provisions to allow handsets to receive from two unsynchronised base stations simultaneously, but a handset can operate in a multi base station environment as long as they are synchronous base stations.

Refer to the block diagram in Fig.1. The DECT Controller consists of a number of functional blocks that operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Blocks have access to SDR via the Internal System Bus (ISB). The ISB consists of an 8-bit data bus, a 10-bit address bus and a number of bus-request/bus-grant signals. Access to the ISB is controlled by ISB Bus Controller (IBC). The IBC acknowledges bus requests on the basis of a priority scheme. The embedded 80C51 controller is to be programmed by the user. It must contain DECT software from Man-Machine Interface (MMI) to the DECT protocols TBC, CBC and DBC (refer to *"Figures 10 to 13, in Section 6 of prETS 300 175-3: June* 1996"). Software is available from Philips Semiconductors.

Hardware state machines in the Burst Mode Logic (BML) and the Speech Interface (SPI) execute the lower blocks in the TBC, CBC and DBC. The 80C51 has control over the BML and the SPI via tables in SDR. The BML saves serial data, received via R_DATAP/M, in buffer areas in SDR. The position of the buffers in SDR is fixed by the 80C51 software by means of the tables previously mentioned. A-fields and B-fields are stored in separate buffers. In this way, two traffic bearers, each with their private A-fields, can share the same B-field buffer as is required in case of bearer hand-over or local call. The DSP and Codec support speech processing functions like analog-to-digital and digital-to-analog conversion, filtering, ADPCM encoding and decoding, 8-bit μ-law PCM to 14-bit linear PCM conversion and its reverse, echo cancelling, tone generation etc.



a. Handset.



b. Base station.

Fig.3 Block diagram examples of DECT systems with PCD509xy.

CONTENTS

Digital telephone answering machine chip PCD6002

1 FEATURES

- Excellent speech quality at average 2.6, 3.2 or 5.2 kbits/s compression rate
- Excellent background noise suppression for speech quality improvement
- Speech compression rate selection: 2.6, 3.2 or 5.2 kbits/s
- Speech decompression rate selection: 2.6, 3.2 or 5.2 kbits/s
- Variable playback speed: 50%, 100% and 200% of real time
- Voice prompt playback
- Philips International Language Library (PILL) support tools available; coding at 2.6, 3.2 or 5.2 kbits/s
- Voice operated start message recording (VOX)
- Call progress detection by busy tone detection and programmable silence detection
- Recording time of minimum 20 minutes in 4-Mbit flash memory (at 3.2 kbits/s)
- Excellent true full-duplex handsfree performance provided by Philips 'Phlux' algorithm
- On-hook caller ID detection according to Bell 202 and V.23 standards, as well as DTMF caller ID support
- Caller Alerting Signal (CAS); caller ID level 2
- Dual tone generation for DTMF, melody tones and information tones
- Optional dial tone detection and optional ringing detection using hardware Caller Identification (CID) interface
- DTMF detection (for remote control function) with local echo canceller for high reliability
- Digital volume control
- Mixed digital/analog adaptive limit and/or level control of audio input signals
- Programmable analog CODEC gain for easy interfacing
- Built-in 32-kbyte OTP (with in-system programming capabilities)
- Internal 80C51 microcontroller can operate as system controller, with selectable operating frequencies between 1 and 21 MHz
- Internal 80C51 microcontroller emergency operation down to 2.7 V eliminates the need for external diallers in telephone answering machine applications
- Standard 80C51 development tools allow fast design of Man-Machine Interface (MMI) features
- On-board Minimum Shift Keying (MSK) modem for CT0 or CT1 applications
- Two integrated differential bitstream Analog-to-Digital Converters (ADCs) for high quality audio input
- Two integrated differential bitstream Digital-to-Analog Converters (DACs) for high quality audio output
- Software selectable auxiliary CODEC input channel

- 34 general purpose digital I/O lines including I²C-bus, available for connection to keyboard, display, line interface, etc.
- On-chip 2-channel time multiplexed 8-bit general purpose ADC for e.g. parallel set detection and battery voltage measurement
- On-chip 8-bit general purpose DAC for e.g. speaker amplifier volume control
- Day and time stamp possibility using built-in real-time clock
- Flexible speech memory interface for connection of several types of speech flash memory (serial, CAD or parallel)
- I²C-bus master/slave bus for peripheral control or I²C-bus speech memory access
- Extensive power management support for battery and emergency operation, also allowing portable (voice memo) applications
- Digital Input/Output Module (IOM) A/μ-law interface for slave or master mode operation at various bit rates.
- Emergency operation from telephone line power only; microcontroller and DTMF generator continue to operate in this mode (<3 mA)
- On-chip Power-on reset circuitry
- On-chip software switchable supply voltage for electret microphone
- Single low supply voltage (2.7 to 3.3 V)
- Built-in single low-frequency, low-power, crystal or ceramic resonator oscillator and on-chip PLL to reduce ElectroMagnetic Interference (EMI)
- Stand-alone operation with low cost PAL, NTSC and DTMF crystals
- Application Programming Interface (API) providing flash memory management functions such as speech, telephone or CID data storage.

2 APPLICATION SUMMARY

The PCD6002 can be used in various applications, some of which are listed below. The corresponding outline application diagrams are given in Chapter 19.

- Stand-alone digital answering machine, with handsfree
- Feature phone with integrated digital answering machine and full-duplex handsfree
- Dual-line digital answering machines
- Analog cordless applications such as CT0 or CT1 base stations, with handsfree, and MSK modem function for RF digital data transmission
- Portable voice memo recorders
- Automotive applications, for example car status announcements
- Low-cost desktop video conferencing
- IOM master/slave interface to connect directly to digital systems such as ISDN and DECT.

2.1 Metalink emulation

Metalink emulation is possible with an OTP-less PCD6002. References to metalink emulation in this data sheet assume this condition.

2.2 OTP programming

Ceibo tools provide parallel programming by customers of application specific parameters into the OTP.

Additionally in-system programming of the OTP memory is possible during production.

3 GENERAL DESCRIPTION

The PCD6002 integrates all the digital and analog speech management and processing functions required for a feature-phone with integrated digital answering machine, or a stand-alone digital answering machine into a single low-cost chip.

Key hardware features giving the chip distinct advantages in performance and application over competitive solutions include:

- The flexibility to change the Man-Machine Interface (MMI)
- An easy-to-program standard 80C51 microcontroller with 32-kbyte internal OTP memory
- High 80C51 microcontroller power for system controller functions of CT0 or CT1 systems
- 34 general purpose I/O lines for peripheral control
- I^2C-bus interface
- Flexible flash memory control to interface to several types of serial and parallel flash memories
- Two integrated 16-bit bitstream audio CODECs for true full-duplex handsfree operation or dual-line stand-alone answering machine operation
- Internal Digital Speech Processor (DSP) for excellent 'HARMONY' sinusoidal speech compression, decompression and variable playback speed
- Embedded DTMF detection, call progress detection and voice operated recording (VOX)
- High quality caller ID FSK demodulation and Caller Alerting Signal (CAS) detection for CID level 2
- 2-channel telephone line input for caller ID FSK and audio interfacing.

Philips provides a sophisticated API running on the internal 80C51, allowing product developers to design their MMIs quickly to suit particular applications. The API takes care of all flash memory and DSP management tasks and can be enhanced on request.

For the pre-recorded voice prompts, the Philips International Language Library (PILL) tools are available for a standard multimedia PC platform under Windows 95. These tools provide a way to compile a range of multi-lingual voice prompts for efficient storage in the speech (flash) memory. The PILL tools support various languages and their grammatical adaptations.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD6002H/2[1]	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

Note

1. Contact sales organization for ordering information.

5 BLOCK DIAGRAM

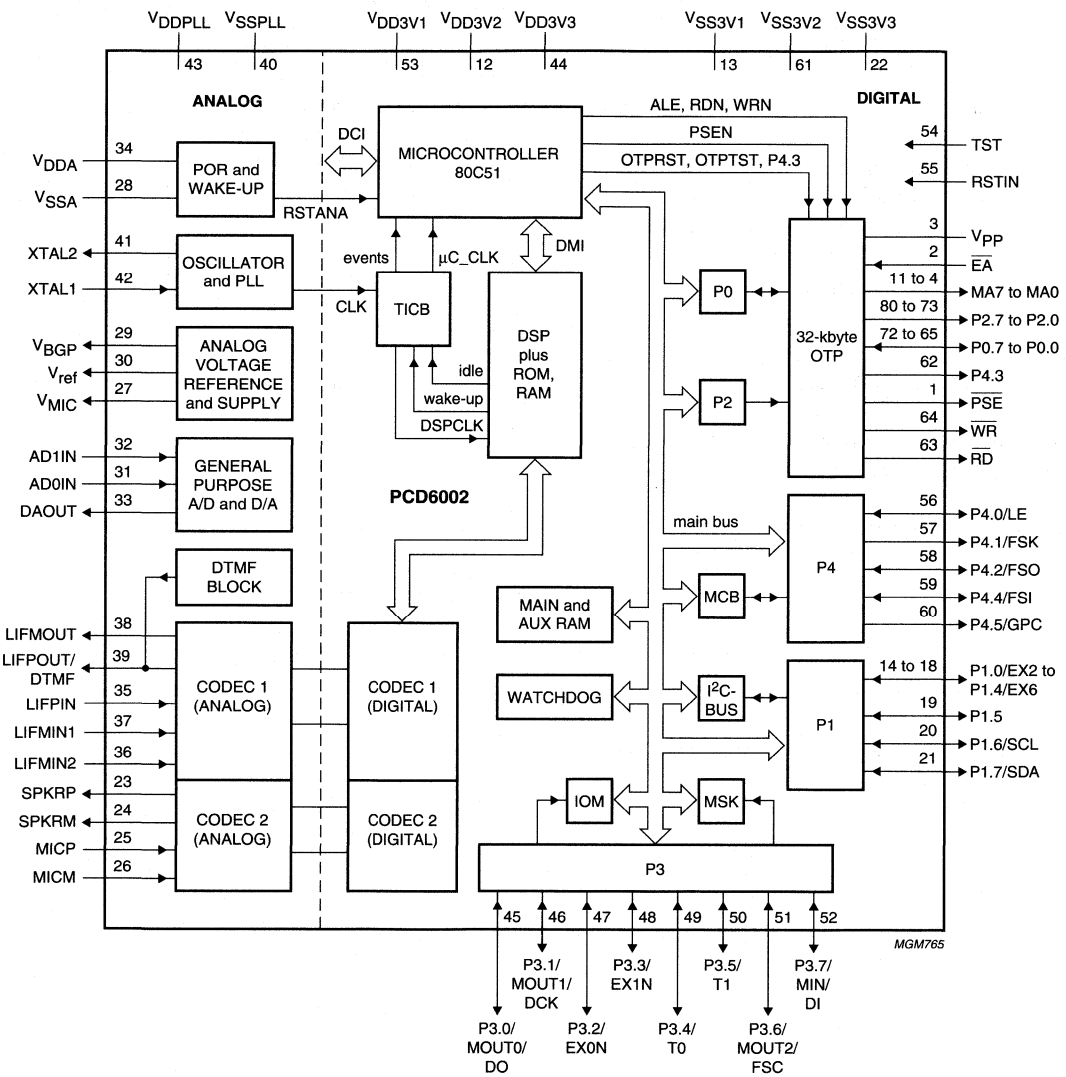


Fig.1 Block diagram.

6 PINNING INFORMATION

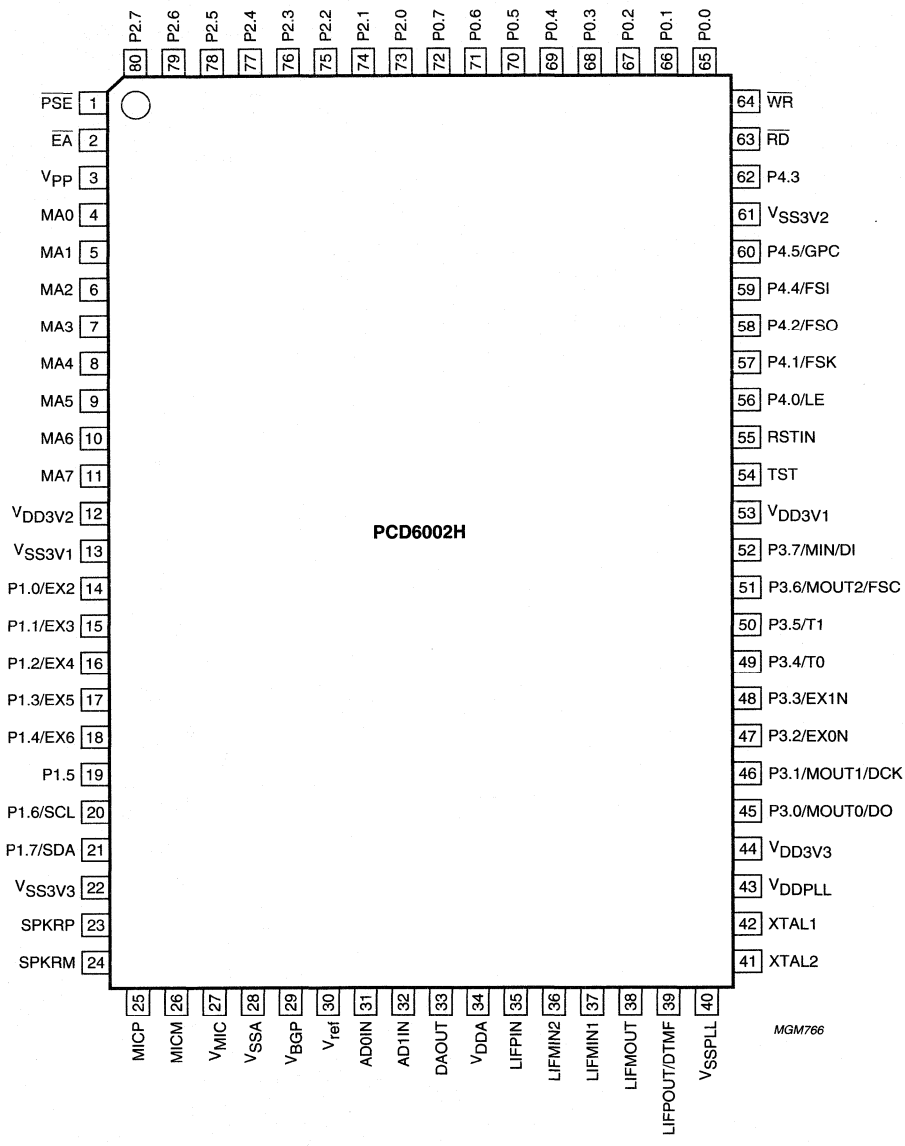


Fig.2 Pin configuration.

Table 1

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE[1]	DESCRIPTION
$\overline{PSE}$	1	O	H	B4	program store enable (80C51) (active LOW)
$\overline{EA}$	2	I		IBUF	80C51 external access (active LOW)
V_{PP}	3	Power supply			programming voltage for OTP
MA0	4	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA1	5	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA2	6	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA3	7	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA4	8	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA5	9	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA6	10	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
MA7	11	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_low, $\overline{EA}$ = 0
V_{DD3V2}	12	power supply			digital supply voltage 2 (3 V)
V_{SS3V1}	13	power supply			digital negative supply voltage 1 (ground)
P1.0/EX2	14	I/O	H	BUP4SW	80C51 port pin/EX2 input
P1.1/EX3	15	I/O	H	BUP4SW	80C51 port pin/EX3 input
P1.2/EX4	16	I/O	H	BUP4SW	80C51 port pin/EX4 input
P1.3/EX5	17	I/O	H	BUP4SW	80C51 port pin/EX5 input
P1.4/EX6	18	I/O	H	BUP4SW	80C51 port pin/EX6 input
P1.5	19	I/O	H	BUP4SW	80C51 port pin
P1.6/SCL	20	I/O	Z	BD4SCI4	80C51 port pin/I²C-bus clock
P1.7/SDA	21	I/O	Z	BD4SCI4	80C51 port pin/I²C-bus data
V_{SS3V3}	22	power supply			digital negative supply voltage 3 (ground)
SPKRP	23	O	1.4 V	ANA	positive output to speaker
SPKRM	24	O	0.7 V	ANA	negative output to speaker
MICP	25	I	0.7 V	ANA	positive input from microphone
MICM	26	I	0.7 V	ANA	negative input from microphone
V_{MIC}	27	O	Off	ANA	positive microphone supply voltage (2 V)
V_{SSA}	28	power supply			analog negative supply voltage
V_{BGP}	29	O	1.2 V	ANA	band gap output voltage (1.2 V)
V_{ref}	30	O	2.0 V	ANA	reference voltage (2 V)
AD0IN	31	I	–	ANAD	analog input channel 1 for general purpose ADC
AD1IN	32	I	–	ANAD	analog input channel 2 for general purpose ADC
DAOUT	33	O	1.0 V	ANAD	analog output channel for general purpose DAC
V_{DDA}	34	power supply			analog supply voltage (3 V)
LIFPIN	35	I	–	ANA	positive analog input of LI CODEC
LIFMIN2	36	I	–	ANA	negative analog input 2 of LI CODEC
LIFMIN1	37	I	–	ANA	negative analog input 1 of LI CODEC
LIFMOUT	38	O	–	ANA	negative analog output of LI CODEC
LIFPOUT/ DTMF	39	O	–	ANA	positive analog output of LI CODEC/DTMF output

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE(1)	DESCRIPTION
V_{SSPLL}	40	power supply			negative supply voltage (ground) for XTAL clock and PLL circuitry
XTAL2	41	O	running	ANAD	crystal oscillator output
XTAL1	42	I	–	ANAD	crystal oscillator input
V_{DDPLL}	43	power supply			supply voltage (3 V) for XTAL clock and PLL circuitry
V_{DD3V3}	44	power supply			digital supply voltage 3 (3 V)
P3.0/MOUT0/DO	45	I/O	H	BUP4SW	80C51 port pin/MSK output 0/IOM data output
P3.1/MOUT1/ DCK	46	I/O	H	BUP4SW	80C51 port pin/MSK output 1/IOM DCK signal
P3.2/EX0N	47	I/O	H	BUP4SW	80C51 port pin/EX0N input
P3.3/EX1N	48	I/O	H	BUP4SW	80C51 port pin/EX1N input
P3.4/T0	49	I/O	H	BUP4SW	80C51 port pin/timer 0 input
P3.5/T1	50	I/O	H	BUP4SW	80C51 port pin/timer 1 input
P3.6/MOUT2/ FSC	51	I/O	H	BUP4SW	80C51 port pin/MSK output 2/IOM FSC signal
P3.7/MIN/DI	52	I/O	H	BUP4SW	80C51 port pin/MSK input/IOM data input
V_{DD3V1}	53	power supply			digital supply voltage 1 (3 V)
TST	54	I	–	IBUFD	test input
RSTIN	55	I	–	SCHMITC	reset in
P4.0/LE	56	I/O	L	BUP4SW(OD)	general purpose I/O/LCD enable
P4.1/FSK	57	O	Z	B8ROD	general purpose output/flash serial clock
P4.2/FSO	58	I/O	Z	BUP4SW(OD)	general purpose I/O/flash serial output
P4.4/FSI	59	I/O	Z	BUP4SW(OD)	general purpose I/O/flash serial input
P4.5/GPC	60	I/O	L	BUP4SW	general purpose output/GP clock output (crystal clock or microcontroller clock)
V_{SS3V2}	61	power supply			digital negative supply voltage 2 (ground)
P4.3	62	O	Z	BD4SCI	5 V tolerant open-drain general purpose output port
$\overline{RD}$	63	O	Z	B4OD	80C51 read (active LOW)
$\overline{WR}$	64	O	Z	B4OD	80C51 write (active LOW)
P0.0	65	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.1	66	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.2	67	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.3	68	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.4	69	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.5	70	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.6	71	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.7	72	I/O	Z	BUP4A	80C51 Port 0 input/output
P2.0	73	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0
P2.1	74	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0
P2.2	75	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0
P2.3	76	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE(1)	DESCRIPTION
P2.4	77	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0
P2.5	78	O	L	B4	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0
P2.6	79	I/O	L	BUP4A	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0; or input for in-system programming purposes
P2.7	80	I/O	L	BUP4A	general purpose output, $\overline{EA}$ = 1; add_high, $\overline{EA}$ = 0; or input for in-system programming purposes

Note

1. The pin type codes are explained in Section 6.1.

6.1 Pin types

6.1.1 Power supply pins

There are 6 different power supply domains (see Fig.3):

- Digital core circuits: V_{DD3V1}/V_{SS3V1}, V_{DD3V2}/V_{SS3V2} and V_{DD3V3}/V_{SS3V3}
- Program supply voltage for OTP programming: V_{PP}
- PLL circuits and crystal oscillator: V_{DDPLL} and V_{SSPLL}
- Analog circuits: V_{DDA} and V_{SSA}.

All V_{SS} pins must be connected to the same ground plane on the PCB. All V_{DD} pins must be connected to the same power supply. All V_{DD} pins have to be separately decoupled, according to the application diagram shown in Fig.35. If not programming, V_{PP} should be left open-circuit or should be pulled up to V_{DD}.

6.1.2 Analog pins

- ANA: Analog I/O pad (protection diode to ground)
- ANAD: Full ESD protected analog I/O pad (double protection diode).

6.1.3 Digital pins

- BUP4SW: 4 mA, 3 V 80C51 I/O pins, OD = configured as open-drain
- IBUPD: Input pad buffer, pull down
- IBUF: Input pad buffer
- SCHMITC: Input pad buffer with Schmitt trigger
- BD4SCI: 4 mA, 5 V tolerant open-drain output only
- B4: 4 mA plain output cell
- B4OD: 4 mA open-drain output cell
- BUP4A 4 mA microport pad, analog input
- BD4SCI4 4 mA bidirectional open-drain I²C-bus pad
- B8ROD 8 mA open-drain output.

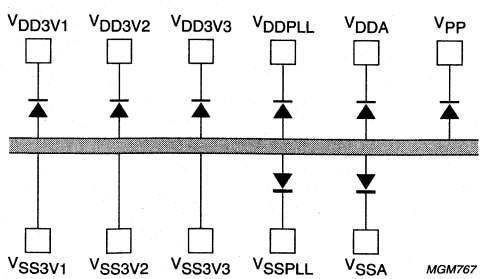


Fig.3 PCD6002 chip supply rails with protection diodes.

7 FUNCTIONAL DESCRIPTION

7.1 Architecture

The PCD6002 architecture is based on an embedded 8-bit 80C51 microcontroller, a Philips 'REAL' DSP core, two high quality analog-to-digital/digital-to-analog CODECs and a 32-kbyte OTP microcontroller memory (see Fig.1).

The most important DSP peripherals are the:

- CODECs
- DSP program ROM
- DSP RAM
- IOM interface.

The most important microcontroller peripherals are the:

- Memory Control Block (MCB)
- Watchdog
- General purpose ports
- I^2C-bus interface
- DTMF block
- MSK block (used for digital data transfer and analog cordless applications).

The MCB can interface to various types of flash memory including serial, parallel or multiplexed command/address data through ports P0, P2, P4 and Memory Address (MA). Most of the peripherals are controlled via microcontroller Special Function Registers (SFRs).

The microcontroller initializes and controls the:

- DSP via the DSP to Microcontroller Interface (DMI)
- Speech flash memory via the MCB and P0/P4 port pins
- Clock and power settings via the Timing and Control Block (TICB)
- Analog section via a 4-wire Digital Control Interface (DCI).

7.2 I/O summary

All digital I/Os for peripherals such as keyboard, display, line interface and others is handled by the microcontroller via ports P0, P1, P3, P4, P2 and MA.

Port 2 and Port MA provide 16 general purpose output-only lines (not bit-addressable, push-pull, 4 mA) to drive peripherals. These ports can be used for peripheral control if $\overline{EA}$ is HIGH. The 4 mA driving level should be adequate to drive a low power LED directly if required.

In addition to these16 output-only lines, 16 general purpose I/O lines are provided by Ports 1 and 3. Port 1 can handle 5 external interrupts (P1.0 to P1.4) that are also high/low interrupt level programmable. Port 1 also contains the I^2C-bus. Port 3 can handle an additional 2 external interrupts (P3.2 and P3.3) which are active LOW only. The timer 0/1 inputs are available on Port 3 as for the standard 80C51. Ports 1 and 3 are 80C51 weak pull-up I/O lines with a 4 mA sink capability, with the exception of the I^2C-bus lines P1.6 and P1.7 which are open-drain. If the P3 alternate port function for the MSK modem is chosen then the standard I/O is not available on ports P3.0, P3.1, P3.6 and P3.7.

Port 4 lines are open-drain with the exception of P4.5 which will be push-pull. These open-drains can be connected via pull-up resistors to the telephone system supply or to the mains AC supply. If a flash memory with a different supply voltage (V_{DD_FLASH} up to 5 V) is connected, P4.3 can be pulled up to this voltage. This is required so the Chip Enable Not (CEN) input of a flash device is equal to V_{DD_FLASH} to reduce the standby power consumption. All other Port 4 pins should not be pulled up to a voltage higher than V_{DD} of the PCD6002.

In case a CAD flash is used, P4.4 and P4.5 are free bit-addressable ports; P4.4 general purpose open-drain I/O, and P4.5 push-pull or open-drain output. This brings the total of I/O lines to 34.

In case an I^2C-bus LCD driver is used, P4.0, at which a LCD Enable (LE) function is provided for 68xx family microcontroller peripherals, is an additional free bit-addressable open-drain I/O port.

The analog interfacing for the PCD6002 consists of the analog audio I/O of the 2 CODECs and 2 additional general purpose analog-to-digital inputs and a general purpose digital-to-analog output for voltage measurement and control respectively. Furthermore, a stabilized microphone supply output V_{MIC} is provided which can be switched on/off for power control.

One audio CODEC is dedicated for the PSTN line communication. This line CODEC has a differential low-ohmic analog output which consists of LIFPOUT and LIFMOUT. In case only one of the differential outputs is used, LIFPOUT should be chosen, since at this output the emergency mode DTMF signal is also available. The line CODEC has 3 inputs which are configurable as 2 single-ended inputs LIFMIN1 and LIFMIN2 that can be selected by software control, while LIFPIN is AC-coupled to ground. It is also possible to use one of the LIFMIN inputs (leaving the other unconnected) in conjunction with the LIFPIN input as a differential input, in case a high CMRR is required.

The second CODEC is dedicated for a local microphone and loudspeaker connection. This handsfree CODEC has a differential low-ohmic analog output which consists of SPKRP and SPKRM. This output can be either differential or single-ended. The speaker output impedance and driving level is not suitable to directly connect a speaker. The handsfree CODEC has a differential microphone input which consists of MICP and MICM. This differential input features a fixed microphone preamplifier of 16 dB.

Both the line and handsfree CODEC outputs have on-chip filtering for out of band signals, so no external filters are required.

There are two 8-bit analog-to-digital inputs AD0IN and AD1IN for voltage measurements which can be used for parallel set detection algorithms or battery control. An 8-bit DAC output DAOUT can provide an analog peripheral control signal.

7.3 Overview of functional description

The detailed functional description is divided into separate Chapters covering the major functional blocks as follows:

Chapter 8: "Power supply, reset and start-up"

Chapter 9: "TICB, generation and selection of system clocks"

Chapter 10: "The microcontroller"

Chapter 11: "DSP I/O registers"

Chapter 12: "External memory interface"

Chapter 13: "The CODECs"

Chapter 16: "External I/O interfaces".

8 POWER SUPPLY, RESET AND START-UP

8.1 Power supply

The PCD6002 core circuitry is supplied by three 3 V supply pairs. The crystal oscillator and PLL are supplied by a separate pair of supply pins to provide a 'clean' supply voltage required for low jitter. The OTP can be programmed via the supplies V_{PP} and V_{SS3V2}.
The following supplies exist:

V_{DD3V1} and V_{SS3V1}: digital supply 1 (3 V)

V_{DD3V2} and V_{SS3V2}: digital supply 2 (3 V)

V_{DD3V3} and V_{SS3V3}: digital supply 3 (3 V)

V_{DDA} and V_{SSA}: analog supply (3 V)

V_{DDPLL} and V_{SSPLL}: crystal clock and PLL supply (3 V)

V_{PP} and V_{SS3V2}: OTP program supply (variable).

8.2 Reset and start-up

After applying the power supply voltage, the chip will perform a Power-on reset, responding to $V_{DDA} - V_{SSA}$. The POR signal is active until V_{DDA} rises above V_{trH} and will not become active again until V_{DDA} drops V_{hys} below V_{trH}.

The Power-on reset is one of 4 ways to perform a reset. The following reset conditions exist:

- From the Power-on reset circuit
- Wake-up from system-off (crystal is off, but power is on) by an external interrupt
- Reset to pin RSTIN
- Watchdog timer expiration.

After a Power-on reset and after a wake-up from system-off, a counter is activated, which guarantees that the first instruction fetch of the microcontroller is delayed by at least 4096 clock cycles.

To reduce power consumption during reset, the following reset strategy is used. If the DSP function is not required, it can be switched off by the micro. The DSP reset will then be delayed (until it is switched on again), in order to avoid a large (reset) power consumption.

9 TICB, GENERATION AND SELECTION OF SYSTEM CLOCKS

The Timing and Control Block (TICB) generates the clocks for all digital chip blocks, and controls the on/off switching of these blocks by using clock gating. The TICB is controlled via the microcontroller Special Function Registers (SFRs) SYMOD, CKCON and SPCON.
The TICB contains:

- An input section to adapt to different input clock rates
- A clock generation section
- A clock selection section
- The real-time clock for a 1 minute interrupt generation
- The microcontroller interrupt timers (FS_event and TIME_event) and the DSP interrupt timer (FS1) to synchronize the microcontroller and DSP processes respectively.

9.1 Microcontroller, DSP, CODEC and IOM clock generation

Figure 4 shows the TICB input section and the clock generation section.

The clock generation section contains a PLL to generate the clock rates which are higher then the input clock rate. With the input section a wider variety of input clock frequencies can be adapted to the input frequency values needed by the PLL (3.456 or 3.580 MHz). In order to save power the PLL can be switched off. This should however only be done when the chip is in the emergency mode. When switching on the PLL, it takes 50 µs (173 emergency clock periods) plus the latency of writing SYMOD (see Section 10.7) until the clock frequencies are derived from the PLL output.

Table 2 gives a description of the signals and their values for a crystal frequency of 3.456 and 3.580 MHz.

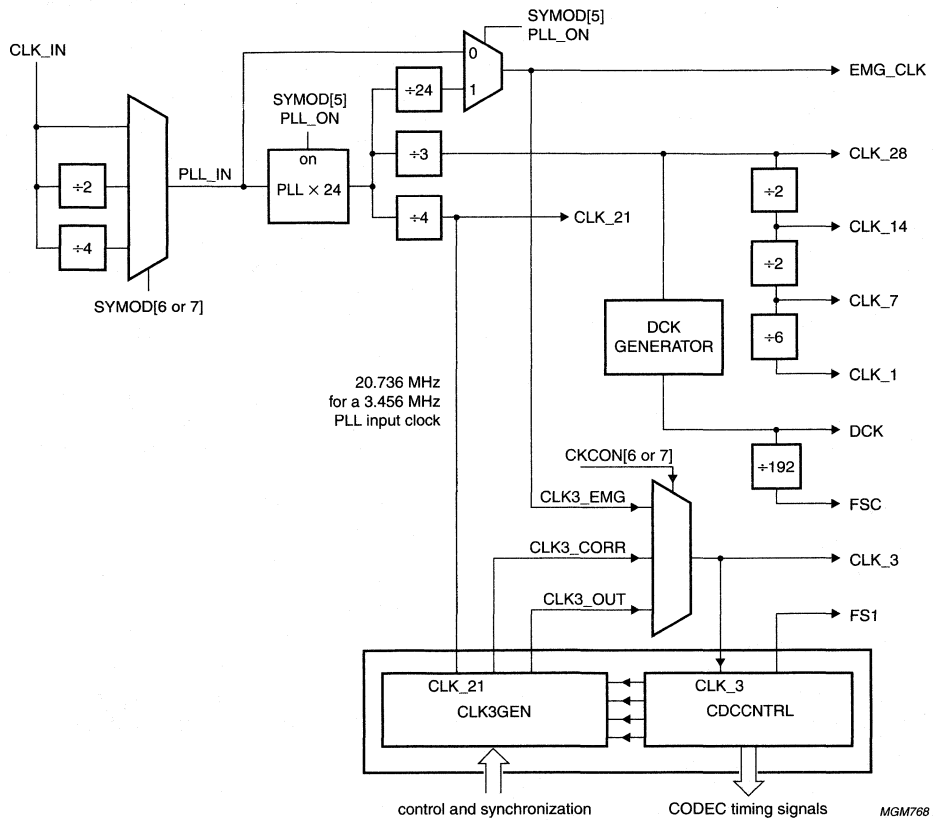


Fig.4 TICB input section and clock generation.

Table 2 Descriptions and frequency values for signals shown in Fig.4

SIGNAL	FUNCTION	VALUE	
		PLL_IN 3.456	PLL_IN 3.580
Microcontroller and DSP clock signals			
EMG_CLK	emergency clock	3.456 MHz	3.580 MHz
CLK_28	DSP selectable clock frequency	27.648 MHz	28.640 MHz
CLK_21	DSP and microcontroller selectable clock frequency	20.736 MHz	21.480 MHz
CLK_14	microcontroller selectable clock frequency	13.824 MHz	14.320 MHz
CLK_7	DSP and microcontroller selectable clock frequency	6.912 MHz	7.160 MHz
CLK_1	DSP and microcontroller selectable clock frequency	1.152 MHz	1.193 MHz
CODEC clock signals			
CLK_21	input clock for phase corrected CLK3_OUT	20.736 MHz	21.480 MHz
CLK3_EMG	EMG_CLK input to CLK_3 multiplexer	3.456 MHz	3.580 MHz
CLK3_CORR	frequency corrected CODEC clock (24/25 × 3.580 MHz)	–	3.437 MHz[1][2]
CLK3_OUT	phase corrected 3.456 MHz CODEC clock	3.456 MHz[1][2]	–
IOM clock/timing signals			
DCKmaster	the IOM master clock signal DCK generated by the TICB	1.536 MHz[1][3]	1.527 MHz[1][3]
FSCmaster	the IOM master frame sync FSC generated by the TICB	8 kHz[1][3]	7.955 kHz[1][3]

Notes

1. These values are only valid if the RTC mode bit CKCON.6 has been set according to the PLL_IN frequency used (see also Table 6).
2. If the IOM slave mode is activated, these clock signals are synchronized to the externally applied FSC.
3. If the IOM slave mode is activated, the externally applied DCK and FSC signals are used.

The clock generation section also contains logic to synchronize the CODEC timing signals and the DSP and microcontroller interrupt timers to an external Frame Synchronization (FSC). This synchronization is only activated when using the IOM in slave mode. If the IOM is activated in master mode, the TICB generates the DCK and FSC signals from CLK_28.

Some of the clock signals can be made available as general purpose clock for various peripherals needing a clock source such as an PCA1070 line interface. This GPC (General Purpose Clock) signal is an alternative output of P4.5 and can be turned on with ALTP bit 3. With ALTP bit 2, the source for GPC can be defined. The GPC source is EMG_CLK (normally 3.580 MHz) when bit 2 is logic 0 and the GPC source is µC_CLK when bit 2 is set to logic 1. The ALTP register is described in more detail in Section 16.2.

9.2 Selection of system clocks

Selection of system clocks involves:

- Selection of the crystal input clock in conjunction with PLL on/off selection (SYMOD register)
- Selection of clocks for the DSP, microcontroller and CODEC, together with microcontroller timing interrupt rates (CKCON register)
- Activation, deactivation of individual clocks or deactivation of the whole TICB in order to get an optimum power consumption (SPCON register).

Tables 3, 4 and 5 summarize the control registers and settings used for system clock selection. SYMOD is a control register in the analog section which the microcontroller accesses via the DCI.

SPCON and CKCON are SFR registers in the digital section which can be directly accessed by the microcontroller.

The activation of the DSP and the digital part of both CODECs is controlled via the SPCON special function register. The clock rates of the DSP and microcontroller, and the microcontroller timing interrupt rates are set via the CKCON special function register.

Figure 5 shows the multiplexers with their input and control signals for the DSP processor clock, the microcontroller clock, the CODEC clock (CLK_3) and the chip input clock frequency. Figure 5 also shows the signals affecting DIS_XTAL. The functional position of the CODEC clock multiplexer is shown in Fig.4.

Table 3 SYMOD register (C5H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
input clock 1	input clock 0	PLL on/off	V_{MIC} on/off	handsfree CODEC and analog		line CODEC and analog	
				D/A (loudspeaker) on/off	A/D (microphone) on/off	D/A (to_line) on/off[1]	A/D (from_line) on/off

Note

1. The DAC of the Line CODEC should not be enabled at the same time as the DTMF TONE output, since there would be a conflict between the two output drivers. This would lead to a high current consumption. The DTMF TONE output is enabled with the TONE bit (DTCON.0).

Table 4 SPCON register (99H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
system off	spare	spare	DSP on/off	handsfree CODEC and digital		line CODEC and digital	
				D/A (Loudspeaker) on/off	A/D (Microphone) on/off	D/A (To_line) on/off	A/D (From_line) on/off

Table 5 CKCON register (9AH) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EMG mode	RTC mode	DSP clock 1	DSP clock 0	µC clock 1	µC clock 0	FS_event 1	FS_event 0

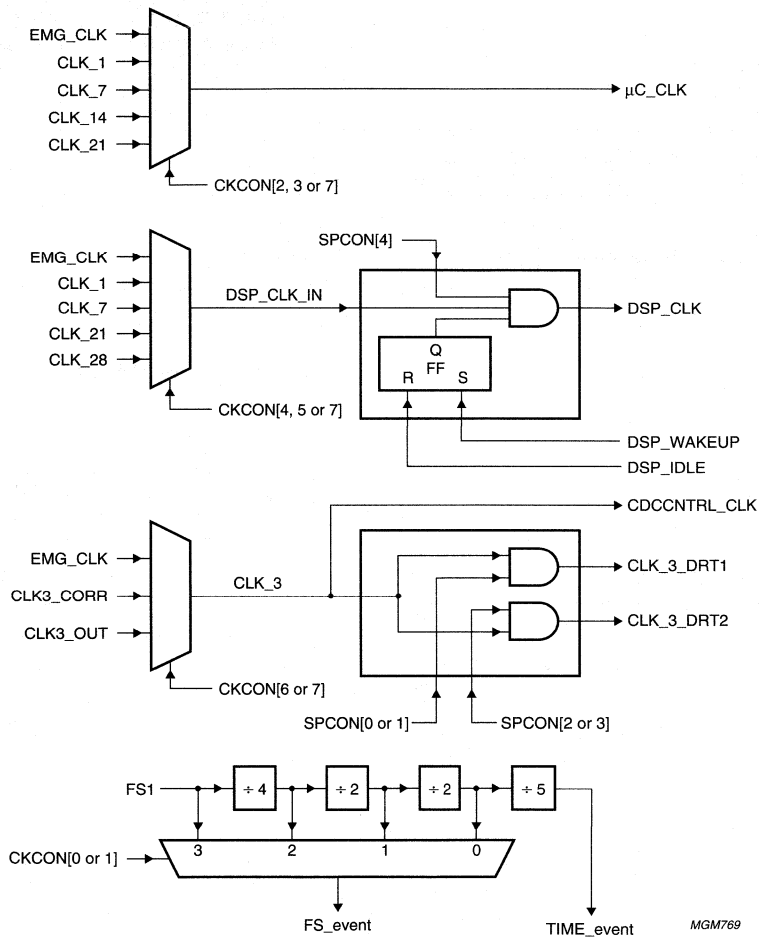


Fig.5 Clock and event rate selection.

Table 6 shows the input clock selection in the analog section of the chip. It should be noted that for 3.456 MHz and the 3.580 MHz crystal input clock, no clock division is done prior to inputting it to the PLL. After reset the input clock division rate is per default 1. This means that in applications using an input clock frequency other than 3.456 or 3.580 MHz, the proper division rate has to be set after system start-up, before the PLL is switched on. Otherwise proper functionality of the PLL and the analog blocks is not guaranteed.

Table 6 Input clock selection

CKCON BIT 6 RTC MODE	SYMOD BIT 7	SYMOD BIT 6	INPUT CLOCK DIVISION RATIO	CHIP INPUT CLOCK FREQUENCY (MHz)
0	0	0	1	3.456
1	0	0	1	3.580(1)
0	0	1	2	6.912
0	1	0	4	13.824

Note

1. The PCD6002 timing system is based on the 3.456 MHz (or multiples) input clock frequency. In order to be able to use the low cost 3.580 MHz crystal or ceramic resonator, a clock frequency correction is needed for some blocks (RTC, CODEC and IOM)

Table 7 shows the microcontroller clock frequencies. In emergency mode (bit 7 of CKCON reset), the EMG_CLK is input directly to the microcontroller. The values of CKCON bits 2 and 3 are then irrelevant.

Table 7 Microcontroller clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 3	CKCON BIT 2	SYMOD BIT 5 PLL ON	MICROCONTROLLER CLOCK FREQUENCY(1)
0	X	X	X	EMG_CLK
1	X	X	0	DO NOT USE(2)
1	0	0	1	CLK_1
1	0	1	1	CLK_7
1	1	0	1	CLK_14(3)
1	1	1	1	CLK_21(3)

Notes

1. 6 clocks/cycle.
2. If the PLL is switched off when not in emergency mode, the selected clock would not be available. The microcontroller would hang up. Before CKCON.7 is set to logic 1, SYMOD.5 must be set to logic 1 to activate the PLL.
3. At these frequencies, correct functionality cannot be guaranteed over the whole temperature and supply voltage range. Under well controlled conditions (room temperature, V_{DD} > 3.0 V), these frequencies can be used e.g. to download information in a flash at a higher frequency. However before selecting these frequencies the OTP sense amplifiers have to be switched on permanently. This should be done by setting the OTP TestControl register to 08H (MOVX to address: 0203). If the OTP TestControl register value is 00H (reset state), the switching on/off of the sense amplifiers is self-timed. This can be used for the lower clock frequencies (EMG_CLK, CLK_1 or CLK_7). If for power saving the sense amplifiers are switched to self-timing mode (e.g. in Idle/Power-down/system-off mode) this should be done after changing the microcontroller clock frequency to one of the lower frequencies EMG_CLK, CLK_1 or CLK_7.

Table 8 shows the DSP clock frequency settings. Setting the DSP frequency to the correct value according to the operating mode of the DSP is done by the Application Programming Interface (API). Please refer to the API specification for more details.

Table 8 DSP clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 5	CKCON BIT 4	CKCON BIT 5 PLL ON	DSP CLOCK FREQUENCY
0	X	X	X	EMG_CLK
1	X	X	0	no clock active
1	0	0	1	CLK_1
1	0	1	1	CLK_7
1	1	0	1	CLK_21
1	1	1	1	CLK_28

Table 9 shows CLK_3 selection (CLK3_SEL see Fig.4). The selection depends on the type of crystal which is connected (determined by RTC mode setting see Table 6). The setting of CKCON[6 and 7], determines the selection of the CLK_3 source (see Table 2 and Fig.4). If CKCON.7 = 0 (emergency mode), CLK_3 will be derived from the EMG_CLK as shown in the following tables.

Table 9 CODEC clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 6 (RTC MODE)	CLK_3 SOURCE
0	X	EMG_CLK
1	1	CLK3_CORR
1	0	CLK3_OUT(1)

Note

1. CLK3GEN is only active in this mode, when phase correction is required and when CLK_21 is available.

The TICB provides two periodic outputs to the microcontroller: FS_event and TIME_event. FS_event is programmable to 4 different rates. Both outputs are derived from and therefore synchronized to FS1. The outputs are connected to an interrupt input of the microcontroller and are called 'time_event interrupt' and 'FS_event interrupt' respectively.
The selection of the FS_event interrupt rate is done via the CKCON SFR, see Section 9.2. Figure 8 shows the generation of these interrupts. Table 10 shows the selection of the FS_event rate. The FS1 clock is provided by the CDCCNTRL block shown in Fig.4.

Table 10 FS_event rate selection

CKCON BIT 1	CKCON BIT 0	FS_event INTERRUPT RATE		
0	0	FS1/16	500 Hz	2 ms
0	1	FS1/8	1 kHz	1 ms
1	0	FS1/4	2 kHz	500 µs
1	1	FS1	8 kHz	125 µs

9.3 Real-time clock generation

The Real-Time Clock (RTC) divider provides a 1 minute timing signal which is available as an interrupt to the microcontroller. The RTC_CLK input clock is always active, whether the PLL is active or not. Thus the complete chip can be set into Power-down mode (but not system-off mode), where the microcontroller can be woken up by the RTC to maintain the values for date and time.
The RTC_CLK is directly derived from the EMG_CLK input clock signal. Figure 6 shows the RTC generation. To divide a 3.456 or a 3.580 MHz clock into a 1 minute RTC signal a 28 bit counter is required to count $60 \times 3.456 \times 10^6$ clock periods. To determine the number of Most Significant Bits (MSBs) of this counter, required for an accurate RTC, the maximum allowed time deviation per month and the crystal accuracy need to be taken into account. The LSB of the 28 counter has an accuracy of $1/(60 \times 3.456 \times 10^6) = 0.005$ ppm (parts per million). Since a normal crystal accuracy is approximately 10 ppm it is tolerable to have only the 17 MSBs of the counter available (10/0.005 = 2000, which implies that the 11 LSBs can be disregarded), as shown in Fig.6.

If one month is $30 \times 24 \times 60 \times 60 = 2.6 \times 10^6$ seconds, 10 ppm deviation equals 26 seconds per month or approximately 5 minutes per year, which is tolerable. Since there are 2 possible RTC_CLK values, 3.580 and 3.456 MHz, there are 2 comparators selectable for the RTC: COMP_3.580 and COMP_3.456.

The nominal value of these comparators are (11 LSBs are set to logic 0):

COMP_3.580: CCD2800H (RTCON = A5H) and
COMP_3.456: C5C1000H (RTCON = 82H)

The conditions for the RTC_MODE signal are described in Section 9.2. To allow connection of various crystals or ceramic resonators, as well as to provide adjustment of the RTC clock according to the crystal tolerance, 8 of the 17 MSBs of the comparators are programmable via the SFR RTCON. The binary values of the comparators are shown in Table 11.

Since the accuracy of Q11 is 10 ppm, with the adjustment of the RTC via RTCON an accuracy of ±5 ppm can be achieved. For an RTC pulse every 1 minute the outer limits of the crystal frequency inputs which can be connected are:

COMP_3.580

Maximum: CCFF800H → 3.582600 MHz

Minimum: CC80000H → 3.573897 MHz.

COMP_3.456

Maximum: C5FF800H → 3.460267 MHz

Minimum: CC80000H → 3.451563 MHz.

The default value of RTCON for an input frequency of 3.580 MHz is A5H and for an input frequency of 3.456 MHz is 82H.

Table 11 Comparator contents

COMPARATOR	Q27									Q18							Q11
										bit 7	<-- RTCON -->						bit 0
COMP_3.580	1	1	0	0	1	1	0	0	1	x	x	x	x	x	x	x	x
COMP_3.456	1	1	0	0	0	1	0	1	1	x	x	x	x	x	x	x	x

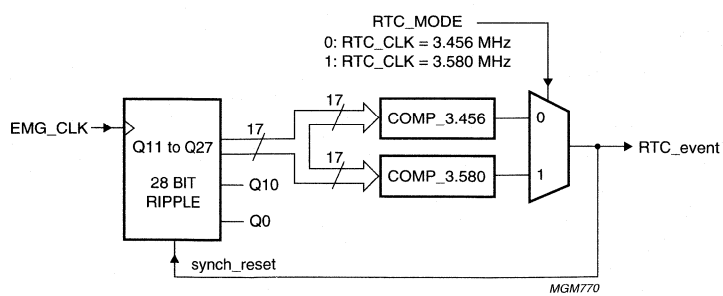


Fig.6 Real-Time Clock (RTC) generation.

10 THE MICROCONTROLLER

The embedded µCMS 80C51 microcontroller controls the Digital Telephone Answering Machine chip (DTAM) by means of Special Function Registers (SFRs). SFRs are defined for the blocks MCB, TICB, DCI, PCON, DSP, I²C-bus, P1/3/4, MA and MSK. All of these (except PCON-power control) are shown in Fig.1. The architecture of the microcontroller itself and the interface to these blocks will be described in this chapter.

10.1 Microcontroller architecture

The microcontroller architecture and its environment is shown in Fig.7.

The microcontroller has some application-specific peripherals such as I²C-bus, Watchdog (WD), P1, P3, P4, MCB and the SFRs of the DSP block, the TICB and the DCI block.

All of these functions and SFRs are located in the Application-Specific Function block (ASF).

The 80C51 core contains the 80C51 standard functions such as timer 0, timer 1 and power-down/IDLE states and a 15-vector dual-level interrupt controller INT15L2. Moreover the microcontroller contains the metalink enhanced hooks protocol which enables metalink emulation via ALE, $\overline{PSE}$, $\overline{EA}$, P0 and P2. The external program memory access is done via the standard ports P0 and P2. Connection of external flash memory is done via the P4, P0 and P2 I/O pads. The microcontroller Clock Driver (CD) has no clock divider, which means that the microcontroller operates on 6 µC_CLK clocks per machine cycle.

The 80C51 has a few basic modes of operation: RESET, NORMAL, METALINK, TEST (various), IDLE and PD. Entering the METALINK mode can be done via inputs ALE, $\overline{PSE}$, $\overline{EA}$ and P2.0 to P2.2 during a reset.

The Idle mode can be entered by setting the IDLE bit in PCON. Leaving the Idle mode can be done via the Master Reset (RSTIN, POR), any external interrupt, a DSP_event, TIME_event or RTC_event, timer 0, timer 1 or I²C-bus interrupt; if these interrupts are enabled.

The PD mode can be entered by setting the PD bit in PCON. The power-down logic of the microcontroller will turn all microcontroller clocks off. The TIME_event, DSP_event, RTC_event and EX2 to EX6 are mixed with EX0 (see Fig.10) and therefore make use of the standard wake-up circuitry of the 80C51. These interrupts should be active for more than 6 clocks (read, modify, write of IRQ1 takes 1 instruction) to guarantee the interrupt for the microcontroller.

Setting the PD bit of PCON after setting the system-off bit of SPCON, will trigger the analog section to turn off the oscillator and therefore the whole chip. Wake-up from system-off can be done via a RSTIN, POR or an external interrupt EX0 to EX6, if the EX0 or EX1 interrupt is enabled. A wake-up from system-off will always reset the PCD6002. The EX interrupt condition should last more than 4096 + 64 + 4 clocks to be sure that the interrupt is handled when entering the NORMAL mode. If the interrupt is shorter the microcontroller will only enter the NORMAL mode after the reset is gone.

10.2 Memory mapping

The memory map of the 80C51 is shown in Fig.8. In addition to all the SFRs, the microcontroller has 128 bytes of directly addressable (DATA) memory, 128 bytes of indirectly addressable (IDATA) memory and 512 bytes of AUX RAM, the on-chip 'MOVX' addressable (XDATA) memory. On-chip XDATA memory access can be disabled by setting the ARD bit in PCON to logic 1.

It is possible to access up to 512 kbytes of external speech data memory stored in a parallel flash memory via ports P0, P2 and P4. A CAD flash memory can also be mapped in this area. A serial (SPI or microwire compatible) flash memory can be connected to P4 which is controlled by the MCB. Up to 64 kbytes of program (CODE) memory can be connected to the P0, P2 and $\overline{PSE}$ pads. This can be the internal 32-kbyte OTP if $\overline{EA}$ is set to logic 1 or any external program memory (such as the MON51 target debug ROM) if $\overline{EA}$ is logic 0. The OTP control registers can only be accessed if P4.3 is logic 1.

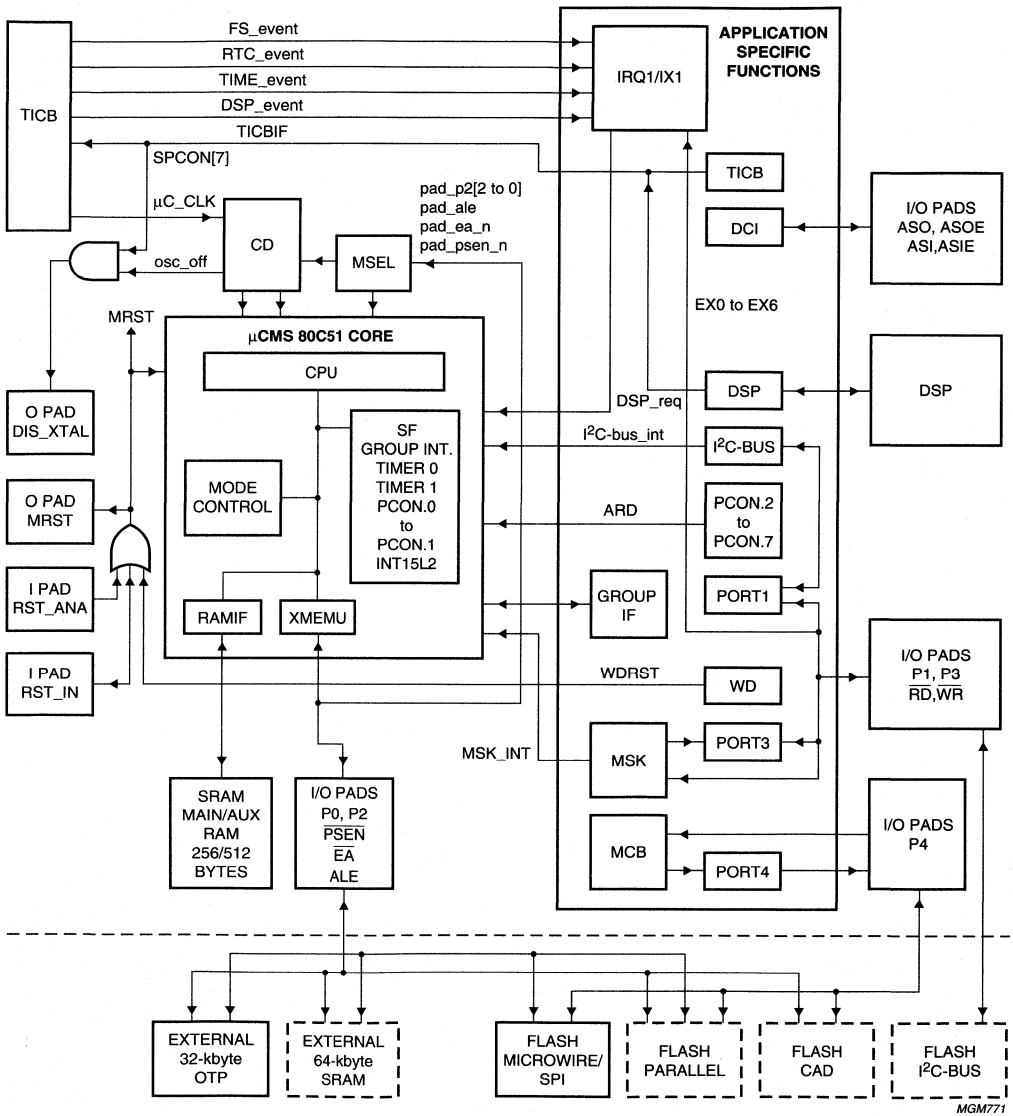


Fig.7 Microcontroller (µCMS 80C51) architecture and environment.

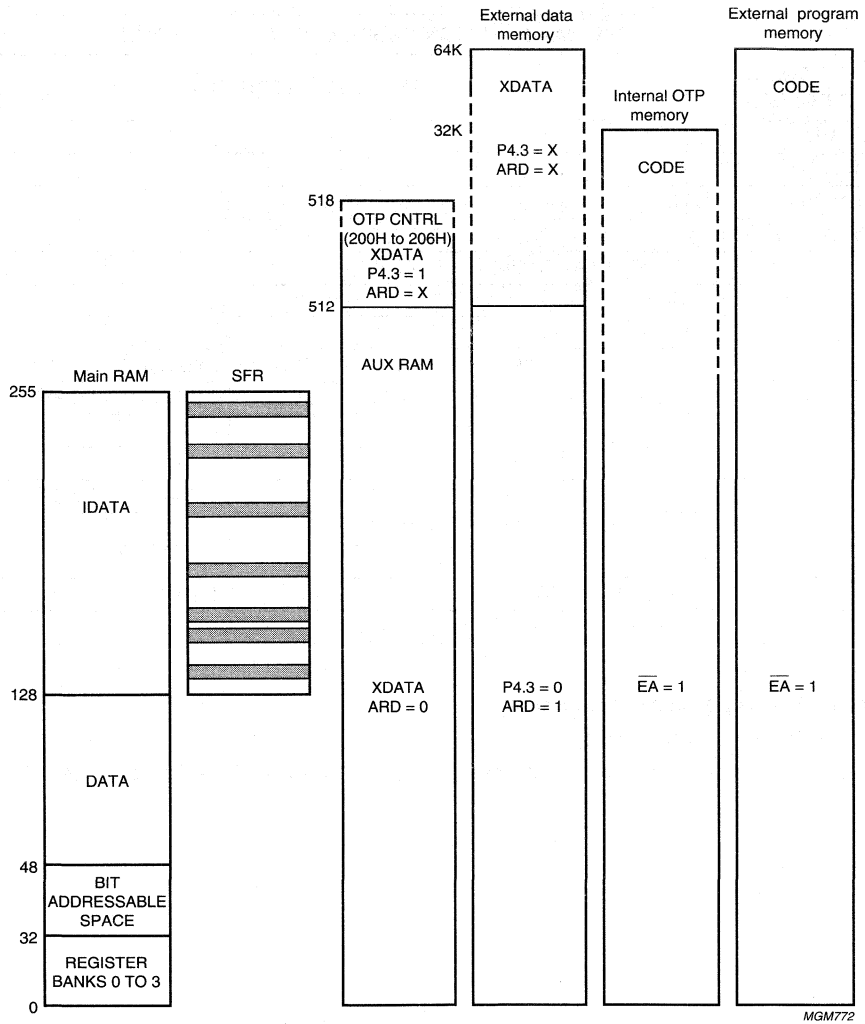


Fig.8 Microcontroller memory map.

10.3 SFR mapping

The SFR mapping for the microcontroller is shown in Table 12. All SFRs together with their reset states are described in Table 13.

Table 12 SFR mapping

SFR ADDRESS (HEX)	SPECIAL FUNCTION REGISTERS - 8 BYTES EACH							
	BIT AND BYTE ADDRESSABLE	ONLY BYTE-ADDRESSABLE						
F8 to FF	IP1(1)	–	–	–	–	–	–	WDT(1)
F0 to F7	B(1)	–	–	–	–	–	–	WDTKEY
E8 to EF	IEN1(1)	IX1	–	–	–	–	–	–
E0 to E7	ACC(1)	–	–	–	–	–	–	–
D8 to DF	S1CON(1)	S1STA(1)(2)	S1DAT(1)	S1ADR(1)	–	–	–	–
D0 to D7	PSW(1)	–	–	–	–	–	–	–
C8 to CF	MCON	MBUF	MSTAT	–	–	–	–	–
C0 to C7	IRQ1	INTC	GPADR	GPADC(3)	GPDAR(3)	SYMOD(3)	DHGF(3)	DTCON(3)
B8 to BF	IP0(1)	XWUD	VREFR(3)	CDVC1(3)	CDVC2(3)	CODTR(3)	DLGF(3)	–
B0 to B7	P3(1)	–	–	–	–	–	–	–
A8 to AF	IEN0(1)	MCSC	MCSD	ALTP	–	–	–	–
A0 to A7	–	–	DTM0(2)	DTM1(2)	DTM2(2)	MTD0	MTD1	MTD2
98 to 9F	P4	SPCON	CKCON	RTCON	–	–	–	–
90 to 97	P1(1)	–	–	–	–	–	–	–
88 to 8F	TCON(1)	TMOD(1)	TL0(1)	TL1(1)	TH0(1)	TH1(1)	–	–
80 to 87	–	SP(1)	DPL(1)	DPH(1)	–	–	–	PCON

Notes

1. Complies to 80C51 family architecture specification.
2. Read only (all other SFRs are read/write).
3. Control register of the analog section. Rewriting these SFRs during the latency period described in Section 10.7 is forbidden.

Table 13 Microcontroller register list

NAME	ADDRESS (HEX)	DESCRIPTION	RESET STATE[1]
ACC	E0	accumulator	0000 0000
ALTP	AB	LE and GPC control	x000 0000
B	F0	B register for multiply, divide or scratch	0000 0000
CKCON	9A	clock control register	0000 0000
CDVC1	BB	CODEC digital volume control for CODEC1	0000 0000
CDVC2	BC	CODEC digital volume control for CODEC2	0000 0000
CODTR	BD	CODEC test register	0000 0000
DLGF	BE	DTMF low group frequency	0000 0000
DHGF	C6	DTMF low group frequency	0000 0000
DTCON	C7	DTMF control register	0000 0000
DPL	82	data pointer low	0000 0000
DPH	83	data pointer high	0000 0000
DTM0	A2	DSP to microcontroller communication register 0	0000 0000
DTM1	A3	DSP to microcontroller communication register 1	0000 0000
DTM2	A4	DSP to microcontroller communication register 2	0000 0000
GPADC	C3	automatic analog-to-digital conversion, channel select bit and request/confirm bit	xxxx x000
GPADR	C2	digital value of analog input	0000 0000
GPDAR	C4	digital value of analog output	1000 0000
IEN0	A8	interrupt enable register 0	0000 0000
IEN1	E8	interrupt enable register 1	0000 0000
INTC	C1	interrupt control register	xxxx xx00
IP0	B8	interrupt priority register 0	x000 0000
IP1	F8	interrupt priority register 1	0000 0000
IRQ1	C0	interrupt request flag register	0000 0000
IX1	E9	interrupt polarity register	xxx0 0000
MCSD	AA	memory control serial data register	0000 0000
MCSC	A9	memory control serial command register	0000 0000
MTD0	A5	microcontroller to DSP communication register 0	0000 0000
MTD1	A6	microcontroller to DSP communication register 1	0000 0000
MTD2	A7	microcontroller to DSP communication register 2	0000 0000
MCON	C8	MSK control register	0000 0000
MBUF	C9	MSK data buffer register	xxxx xxxx
MSTAT	CA	MSK status register	0x00 0000
P1	90	general purpose digital I/O	1111 1111
P3	B0	general purpose digital I/O	1111 1111
P4	98	P4 can be used to control flash memory	xx01 1110
PCON	87	power and interrupt control register	x000 0000
PSW	D0	program status word	0000 0000

NAME	ADDRESS (HEX)	DESCRIPTION	RESET STATE[1]
RTCON	9B	real time clock control	0000 0000
S1CON	D8	I²C-bus serial control register	0000 0000
S1ADR	DB	I²C-bus own slave address register	0000 0000
S1DAT	DA	I²C-bus data shift register	0000 0000
S1STA	D9	I²C-bus status register	1111 1000
SYMOD	C5	analog system mode control	0000 0000
SPCON	99	system power and clock configuration	0000 0000
SP	81	stack pointer	0000 0111
TCON	88	timer/counter control register	0000 0000
TMOD	89	timer/counter mode control register	0000 0000
TL0	90	timer low register 0	0000 0000
TL1	91	timer low register 1	0000 0000
TH0	92	timer high register 0	0000 0000
TH1	93	timer high register 1	0000 0000
VREFR	BA	voltage reference register	1001 1010
WDT	FF	Watchdog timer	0000 0000
WDTKEY	F7	Watchdog key register	0000 0000
XWUD	B9	external wake-up disable	0000 0000

Note

1. All SFR bits with a reset state with an 'x' are spare but have a flip-flop in this position with reset state '0'.

10.4 Microcontroller interrupts

The microcontroller has 15 interrupt sources which can be programmed to have a low or high priority:

- EX2 to EX6 asynchronous external interrupts via P1.0 to P1.4
- EX0 and EX1 asynchronous external interrupts via P3.2 (INT0N) and P3.3 (INT1N)
- DSP_event
- FS_event
- TIME_event
- I²C-bus interrupt
- RTC_event
- Timer 0 and timer 1 interrupt
- MSK interrupt.

If enabled these interrupts sources result in a jump to the addresses shown in Table 14.

Table 14 Allocation of interrupt sources

VECTOR	SOURCE	NUMBER(1)	PRIORITY(2)	DESCRIPTION	IENx/IPx
0003	EX0	0	1	external interrupt 0	IEN0.0/IP0.0
000B	T0	1	4	timer 0 interrupt	IEN0.1/IP0.1
0013	EX1	2	7	external interrupt 1	IEN0.2/IP0.2
001B	T1	3	10	timer 1 interrupt	IEN0.3/IP0.3
0023	MSK_event	4	13	MSK RI or TI interrupt	IEN0.4/IP0.4
002B	TIME_event	5	2	TIME interrupt	IEN0.5/IP0.5
0033	FS_event	6	5	FS interrupt	IEN0.6/IP0.6
003B	EX2	7	8	external interrupt 2	IEN1.0/IP1.0
0043	EX3	8	11	external interrupt 3	IEN1.1/IP1.1
004B	EX4	9	14	external interrupt 4	IEN1.2/IP1.2
0053	EX5	10	3	external interrupt 5	IEN1.3/IP1.3
005B	EX6	11	6	external interrupt 6	IEN1.4/IP1.4
0063	I²C-bus	12	9	I²C-bus interrupt	IEN1.5/IP1.5
006B	DSP_event	13	12	DSP interrupt	IEN1.6/IP1.6
0073	RTC_event	14	15	RTC interrupt	IEN1.7/IP1.7

Notes

1. For some C-compilers '1' has to be added to this number.
2. The interrupt controller supports up to 15 interrupt sources, each with a 2-level (high or low) priority. A high priority interrupt is always serviced before a low priority interrupt, but within the high and low levels, interrupts are serviced in the order shown in this column.

The external interrupt configuration of P1 is shown in Fig.9. Pins P1.5, P1.6 and P1.7 cannot be used as external interrupts. The IX1 SFR determines the polarity of the external interrupt sources of P1. Clearing the Global Enable bit in IEN0 disables all interrupt sources. Using IEN0 (and IEN1) each individual external interrupt can be enabled or disabled.

The IRQ1 SFR stores all external interrupts. So, if an external interrupt with a low priority is detected during execution of another (high or low priority) interrupt, it will be handled just after the return of this interrupt. The interrupt service routine for an external interrupt must clear the right IRQ1 flag to indicate that it has serviced the interrupt request. It should be noted that during the interrupt routine this flag can be set again immediately after clearing the IRQ1 flag if the interrupt source is (still) HIGH.

The complete interrupt system is shown in Fig.10. All 15 interrupts are allocated and can be given a low or high priority according to the setting of IP0 and IP1.

Each interrupt source can be individually enabled by means of IEN0 and IEN1.

The IRQ1 and IX.7 registers are clocked (a clock which is active during IDLE) and can be set by P1.0 to P1.4, the TIME_event, the DSP_event, the FS_event and the RTC_event. These flags can only be cleared by software. Only TCON.1, TCON.3, TCON.5 and TCON.7 flags are cleared by the interrupt controller hardware. All other flags must be cleared by software.

The polling of a potential interrupt goes from a high priority to a low priority interrupt. Within a high (or low) priority interrupt level the EX0 (if set to high priority) will be polled first followed by the next high priority interrupt.

The interrupt SFRs IP0, IP1, IEN0, IEN1, IRQ1 and IX1 (described previously) are defined in Tables 15 to 20. A flag set to logic 1 in IP0 or IP1 (Tables 15 and 16) causes the corresponding interrupt to have high priority.

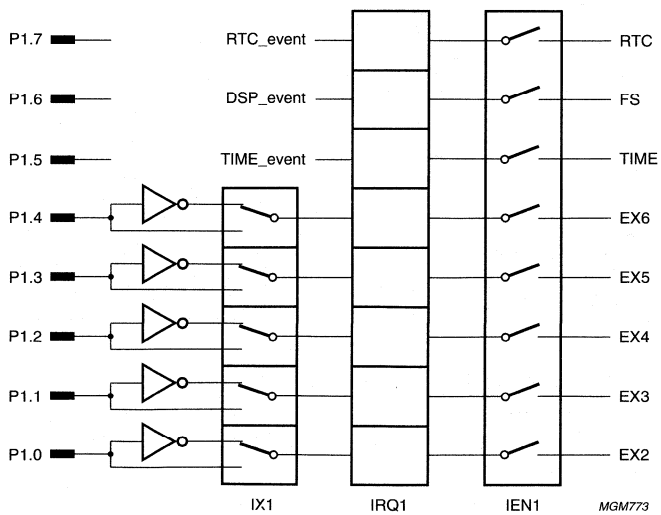


Fig.9 PCD6002 Port 1 external interrupt configuration.

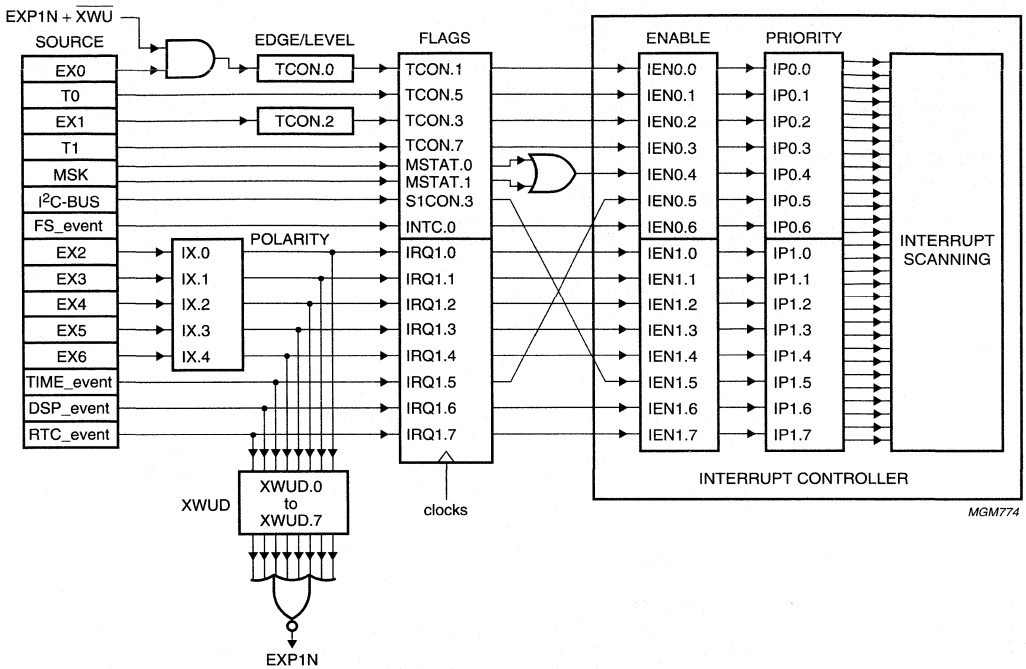


Fig.10 PCD6002/80C51 interrupt system.

Table 15 IP0 (B8H) bit assignment, reset state X0000000b

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	priority FS_event	priority TIME	priority MSK	priority T1	priority EX1	priority T0	priority EX0

Table 16 IP1 (F8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
priority RTC	priority DSP	priority I²C-bus	priority EX6	priority EX5	priority EX4	priority EX3	priority EX2

Table 17 IEN0 (A8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Enable	enable FS_event	enable TIME	enable MSK_event	enable T1	enable EX1	enable T0	enable EX0

Table 18 IEN1 (E8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
enable RTC	enable DSP	enable I^2C	enable EX6	enable EX5	enable EX4	enable EX3	enable EX2

Table 19 IRQ1 (C0H) bit assignment, reset state 00H; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RTC Flag	DSP Flag	TIME Flag	EX6 Flag	EX5 Flag	EX4 Flag	EX3 Flag	EX2 Flag

Note

1. The flags of IRQ1 will be set to logic 1 by hardware if the interrupt occurs. They must be cleared by software in the interrupt service routine.

Table 20 IX1 (E9H) bit assignment, reset state 00H; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	spare	spare	polarity EX6	polarity EX5	polarity EX4	polarity EX3	polarity EX2

Note

1. A polarity bit set to logic 1 in IX1 will cause the external interrupt to be active 'HIGH'.

Table 21 INTC (C1H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	spare	spare	spare	spare	spare	eXtended Wake-Up, XWU	FS Flag

Table 22 XWUD (B9H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RTC XWU disable	DSP XWU disable	TIME XWU disable	EX6 XWU disable	EX5 XWU disable	EX4 XWU disable	EX3 XWU disable	EX2 XWU disable

10.5 Interface to DSP

The DSP-to-Microcontroller Interface (DMI) can be used for the following purposes:

- Transferring compressed speech data from microcontroller to DSP
- Transferring compressed speech data from DSP to microcontroller
- Transferring DSP parameters (DSP mode, tone frequency, etc.) from microcontroller (API) to the DSP
- Transferring DSP events (caller ID, ring detect, VOX, call progress, etc.) to the microcontroller.

The microcontroller and the DSP can communicate by means of 6 SFRs (MTD0 to MDT2 and DTM0 to DTM2) and 4 DSP I/O registers (DTMC, DTMD, MTDC and MTDD), (see Fig.11). The DTMC and MTDC registers are used for communication and control and the DTMD and MTDD registers for transferring data.

The MT (Micro Transmit), DR (DSP Receive), DT (DSP Transmit), and MR (Micro Receive) ensure that either the old data is read or new data is read although the DSP and microcontroller operate on different clocks. This can be achieved by means of simple handshake circuitry in either direction. The DR state machine ensures that the DSP will never read new MTDC control data and old MTDD speech data. In order to guarantee proper transitions of the DR state machine the DSP always has to read the DTMC first and afterwards the DTMD I/O register.

The TICB generates the DSP_event interrupt when it receives a dsp_µc_req signal. The dsp_µc_req cannot be generated by the microcontroller because the dsp_event interrupt must be able to wake-up the microcontroller from PD.

MTD0 to MTD2 are written by the microcontroller. After each write to MTD0 the contents of MTD0 to MTD2 are transferred to the 16 bit register MTDD and the 8-bit register MTDC (the MSB is set to 00H), which can be read by the DSP via the DSP I/O bus. In this way the DSP always receives a valid control byte and a valid 16-bit data word. If MTD0 is written to while the DSP is turned off, the MTD0 value will be transferred to the MTDC I/O register as soon as the DSP is turned on.

The MTDC and MTDD registers are continuously and immediately read by the DSP after every FS1 interrupt. The microcontroller can write a new word to MTD0 to MTD2 but has to wait for at least 125 µs to be sure that the DSP has read the previous value.

DTM0 to DTM2 are read by the microcontroller as SFRs. The contents of the DTMD and DTMC registers are transferred to the DTM0 to DTM2 SFRs when the DSP writes to the DTMC register. At this time an interrupt signal called DSP_event is generated to the microcontroller, which triggers the microcontroller to read the DTM0 to DTM2 SFRs. In this way DSP events and speech data can be transferred easily to the microcontroller. The DSP will transfer every 125 µs a maximum of 3 bytes, for example one command byte and two data bytes, to the microcontroller. Thus one write to DTMC takes place every 125 µs.

Similarly, the microcontroller can transfer a maximum of 3 bytes every 125 µs to the DSP. Thus one write to MTD0 takes place every 125 µs. The default rate for the FS_event interrupt will be FS1/8 resulting in a data transfer rate of 10 words every 10 ms which equals 16 kbits/s. In case a higher rate is needed the FS_event interrupt rate can be switched to FS1/4.

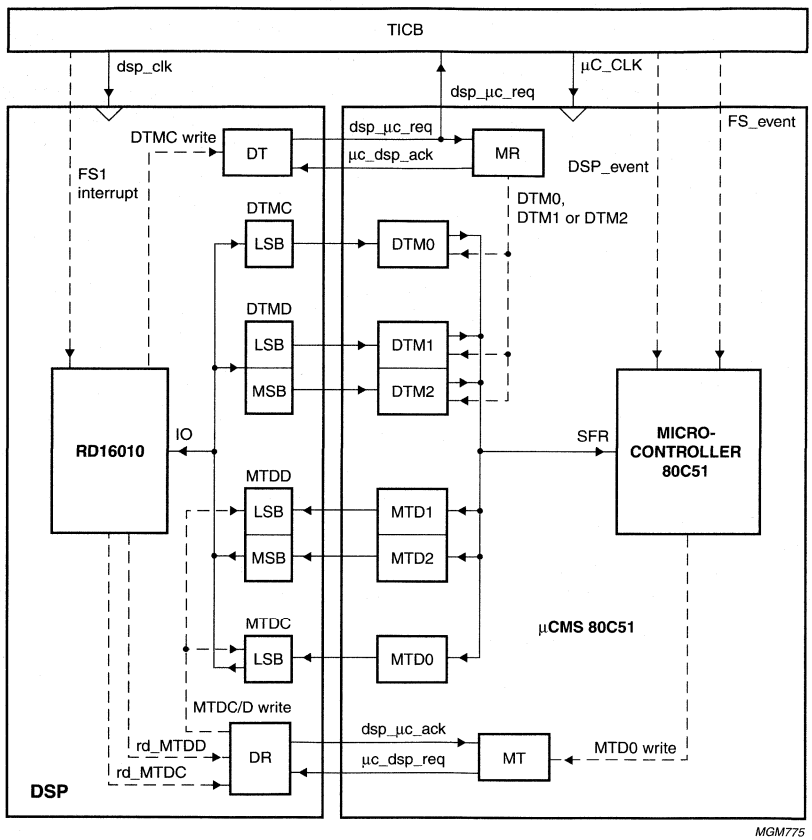


Fig.11 DSP-to-Microcontroller Interface (DMI).

10.6 Interface to Real-Time Clock (RTC)

When the RTC_event interrupt is enabled in IEN1 and the Global Enable bit in IEN0 is set and the PCD6002 is not in emergency mode (CKCON.7 = 1), the microcontroller will get an RTC_event interrupt every 1 minute. The RTC interrupt service routine must clear the RTC flag. The RTC_event interrupt will also wake-up the microcontroller when it is in the PD or in the IDLE state. Under power saving conditions this will allow the user to switch off the microcontroller and still maintain an accurate real-time clock.

10.7 Interface to the analog section (DCI)

The analog section is controlled by the microcontroller by means of the 10 SFRs listed below. The value of the GPADR register is defined by the analog section and can be read by the microcontroller as an SFR. The SFRs which are copied from the digital section to the analog section are:

- SYMOD
- GPADC
- GPDAR
- RVREF
- CDVC1
- CDVC2
- CODTR
- DLGF
- DHGF
- DTCON.

Due to the implementation of the analog section, it takes 15 emergency clock periods until a change of the SFR value is seen by the analog section. If the SFR is written a second time during this period, the value seen by the analog section will be corrupted.

When multiple analog control SFRs are written to shortly after each other the latency of the individual bytes adds up. This can lead to a 120 emergency clock periods long latency, during which rewriting of the SFRs is forbidden.

10.8 Interface to the Memory Control Block (MCB)

The MCB is a 3-wire serial interface designed to interface with a versatile range of serial flash memories (both microwire and SPI mode 0 or mode 3 compatible slave devices) in parallel with program OTP/external ROM and even external data SRAM.

The 3-wire serial interface consists of a serial data output (FSO), serial data input (FSI) and a serial clock signal (FSK). FSK, FSO and FSI are alternative functions of the general purpose I/O pins P4.1, P4.2 and P4.4. The serial interface is controlled via the MCSC and MCSD special function registers. The FSK and FSO outputs are both open-drain and must be pulled to 3 V with external resistors R_{FSK} and R_{FSO}. The recommended value for both resistors at high FSK speeds (>1 MHz) is 1 kΩ. The MCSC SFR is defined in Table 23.

Turning on the MCB by setting bit MCSC.3, will switch the FSK and FSO pins to logic 0. A write to MCSD will generate the appropriate FSK/FSO signal. A read from MCSD will only generate 8 FSK pulses and will shift-in the next byte. The shifting and the FSK/FSO signal can be suppressed by setting bit 2 of MCSC. This can be used for reading the last byte of the serial flash memory during a read sequence. The FSK shift-off operation however is not necessary if the MCB is already turned off when reading the MCSD SFR for the last time.

If a serial flash memory is chosen the FSK master clock rate can be selected with bits 0 and 1 as shown in Table 24. The MCB is always master, which means that the FSK clock is always generated by the PCD6002.

Data coming from or going to the serial flash memory can be accessed by means of the MCSD SFR. This is simply an 8-bit serial shift register. The first bits FSO and FSI are always the most significant bits of MCSD. The first read from the MCSD SFR will only serially load the MCSD SFR with valid data. Therefore the first read operation must always be followed with another read operation which reads the actual received data out of the MCSD SFR.

The serial shifting of bits into and out of MCSD is done at the same moment: 1 microcontroller clock before the falling edge of FSK (= t_{SF}). When the FSK speed is programmed at the highest speed (μC_CLK/4) this shifting will be done in the middle of the FSK HIGH-level time. The most time-critical situation is when FSK is only 2 clocks wide and has a frequency of 3.5 MHz (14 MHz/4). In this case make sure that $t_{r(FSK)}$, which can be controlled by the value of R_{FSK}, is greater than the hold time requirement of the slave device.

Figure 12 describes how a microwire compatible device can be accessed with an FSK speed of µC_CLK/4. An SPI mode 0 or mode 3 device requires an additional FSK clock falling edge to trigger the slave device to generate valid data on the FSI line. The SPI mode 3 can be achieved by starting with FSK HIGH when the device is turned on (turn MCB on after asserting the chip enable of the slave device) and by ending with FSK. The SPI mode 0 can be achieved by generating an additional FSK pulse (by turning the MCB off and on again, see Fig.12) between the last write to MCSD and the first read of MCSD.

A variety of serial flash memory driver software packages is included in the API software for the microcontroller that is provided with the chip.

Table 23 MCSC (A9H) bit assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	Spare	Spare	MCB On	Shift off	FSK Rate 1	FSK Rate 0

Table 24 FSK clock rate

MCSC BIT 1	MCSC BIT 0	FSK CLOCK RATE
0	0	µC_CLK/4
0	1	µC_CLK/8
1	0	µC_CLK/16
1	1	µC_CLK/32

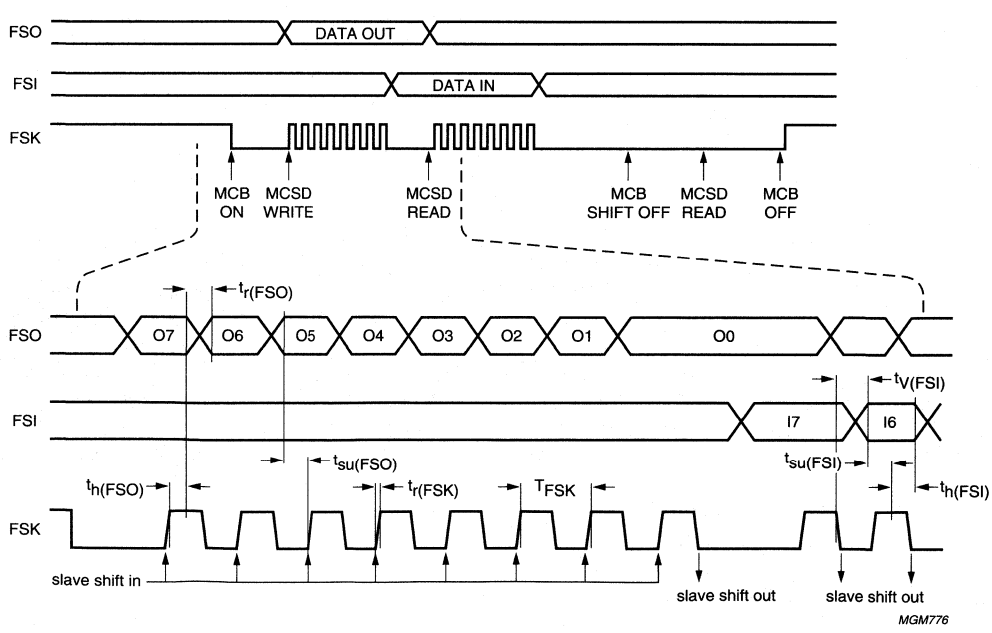


Fig.12 MCB timing for a microwire compatible device.

10.8.1 PARALLEL FLASH INTERFACE

If a parallel (4-Mbit) flash memory is chosen Table 25 is valid.

Since parallel flash memory has a much larger addressing range than the 64 kbytes addressing capability of the 80C51, additional addressing is done by means of the P4 SFR and the P4 I/O pad. The P4 SFR is connected to port P4 as shown in Table 26.

One pin is necessary to enable and disable the flash memory to reduce power consumption. Four pins of P4 are necessary to connect various types of flash memories:

- A parallel flash: P4.0 to P4.2, P4.3, $\overline{RD}$ and $\overline{WR}$ are connected to MA16 to MA18, CEN, OEN and WN
- A serial flash: FSO, FSI, FSC and P4.3 are connected to DI, DO, SK and CEN pins
- A CAD flash: P4.1 to P4.3, $\overline{RD}$ and $\overline{WR}$ are connected to CLE, ALE, CEN, REN and WEN pins.

$\overline{RD}$ and $\overline{WR}$ are available as separate pins. If an access is done to the AUX RAM (ARD bit of PCON equals logic 1) the $\overline{RD}$ and $\overline{WR}$ will be logic 1 on these pins.

Bits 1, 2 and 4 of Port 4 are set to FSI, FSK and FSO when a serial flash is selected in the MCSC SFR.

The P4 SFR is defined in Table 27. Bits P4.6 and P4.7 are not available as chip port pins. These bits can however be used as bit-addressable general purpose bits.

Table 25 Using P4 with 4-Mbit parallel flash memory

P4.2	P4.1	P4.0	ADDRESS
0	0	0	Bank 0, 00000H to 0FFFFH
0	0	1	Bank 1, 10000H to 1FFFFH
0	1	0	Bank 2, 20000H to 2FFFFH
0	1	1	Bank 3, 30000H to 3FFFFH
1	0	0	Bank 4, 40000H to 4FFFFH
1	0	1	Bank 5, 50000H to 5FFFFH
1	1	0	Bank 6, 60000H to 6FFFFH
1	1	1	Bank 7, 70000H to 7FFFFH

Table 26 P4 port pin behaviour

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	spare	P4.5/GPC	P4.4/FSI	P4.3	P4.2/FSO	P4.1/FSK	P4.0/LE

Table 27 P4 (98H) bit assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0

10.9 The test register CODTR

The special function register CODTR can put the DSP or the digital parts of the CODECs into various test modes. In these test modes normal operation is not guaranteed any more. The output behaviour of P3.0, P3.1, P3.2, P3.3 and P3.4 can be changed and the DSP test modes can lead to a higher current consumption and to malfunction of the DSP. Therefore changing the value of this register should be avoided.

10.10 Interface to Timing and Control Block (TICB)

The interface to the TICB consists of the special function registers SPCON, CKCON and RTCON and the signals µC_CLK_EN, µC_CLK, FS_event, Time_event and RTC_event. The signals are described in Section 10.1.

10.11 The PCON special function register

Table 28 PCON (87H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	ARD	spare	WLE/EW	GF1	GF0	PD	IDL

Bits 0 and 1 of PCON can be set to logic 1 to put the microcontroller into the IDLE or PD state.

In the IDLE state the functions Timer 0/1 and the I^2C-bus controller are still clocked. The CPU status along with all SFRs, Main RAM and AUX RAM registers are preserved. Leaving the IDLE state can be done by any enabled interrupt or reset. The microcontroller hardware will clear the IDLE flag and start executing the interrupt. When the interrupt is serviced (RETI instruction) the microcontroller will execute the next instruction following the instruction that put the microcontroller in the IDLE state.

In the PD state the clock of the entire microcontroller with its peripherals is off. The CPU status along with all SFRs, Main RAM and AUX RAM registers are preserved. Leaving the PD state can be done by any active enabled interrupt source or reset. The microcontroller hardware will clear the PD flag and start executing the interrupt. When the interrupt is serviced (RETI instruction) the microcontroller will execute the instruction following the instruction that put the microcontroller in the PD state.

Bits 2 and 3 of PCON are general purpose flags. Bit 4 is used to enable the (load of the) Watchdog timer. The Watchdog function is explained in Section 10.12.

The ARD bit is used to disable the access of a MOVX instruction to the 512 bytes of the AUX RAM. If ARD is set to logic 1 a MOVX operation can access the lower 512 bytes of the external memory. The upper part of the external memory can always be accessed independently of the setting of the ARD bit.

10.12 The Watchdog circuitry

The purpose of the Watchdog is to reset the microcontroller if it enters erroneous states caused by EMI or bugs in the software that cannot be detected or eliminated.

When enabled the Watchdog circuitry will generate a reset if the user program fails to reload the Watchdog timer within a specified duration of time known as the Watchdog interval.

The Watchdog interval is determined by the following equation: $T_{WD} = (256 - WDT) \times \frac{12287}{\mu C\_CLK}$

The programmer should implement the following protocol:

1. Write the key value 55H to the WDTKEY SFR to disable the Watchdog.
2. Set the WLE/EW bit to logic 1 to initially enable the Watchdog. WLE/EW now functions as a WLE bit. Only a reset can clear the EW bit.
3. Enable the Watchdog timer by writing a value not equal to 55H to the WDTKEY SFR. This is only necessary if the previous value of the WDTKEY register was 55H. The value after reset is 00H.
4. Enable the load of the WDT SFR by setting the WLE bit to logic 1.
5. Load the Watchdog interval by writing the required value into the WDT SFR. After the load the WLE bit is set to logic 0 again by the Watchdog hardware. The value of WDT is 00H after reset.
6. Write a value not equal to 55H to the WDTKEY SFR to enable the Watchdog.
7. Repeat steps 4 and 5 in the user software before the Watchdog timer expires.

It should be noted that in metalink emulation mode the Watchdog cannot be used and that the Watchdog reset will reset the entire chip.

10.13 I²C-bus

The serial port of the I²C-bus is a simple bidirectional 2-wire bus for efficient inter-IC data exchange.
The I²C-bus consists of a data line (SDA) and a clock line (SCL), see Fig.13. These lines also function as I/O port P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and supports all four I²C-bus operating modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

The I²C-bus block contains 4 SFRs. The mode of operation is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR is the slave address register. Slave address recognition is performed by hardware.

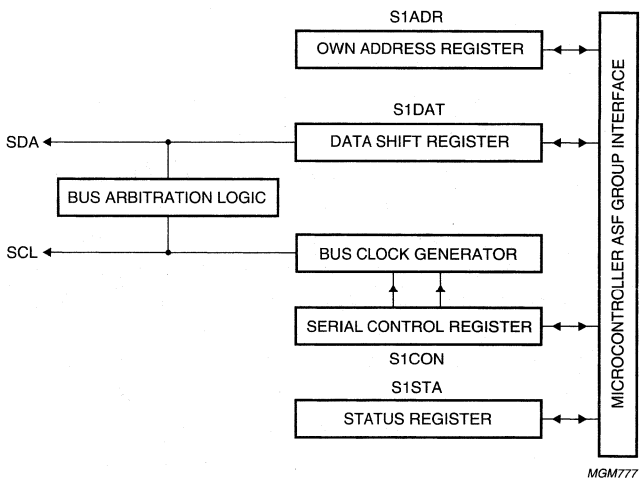


Fig.13 I²C-bus serial I/O.

10.13.1 SPECIAL FUNCTION REGISTER S1CON (D8H)

Two bits are affected by the SIO1 hardware, the SI bit is set to logic 1 when a serial interrupt is requested, and the STO bit is set to logic 0 (cleared) when a STOP condition is present on the I²C-bus. The STO bit is also cleared when ENS1 = 0. When the SIO1 is in the master mode the serial clock frequency is determined by the clock rate bits CR2, CR1 and CR0 (see Tables 29 and 30).

Table 29 Serial control register S1CON

BITS	SYMBOL	DESCRIPTION
7	CR2	Determines together with CR1 and CR0 the SCL bit rate, see Table 30.
6	ENS1	When this bit is set to logic 0 the SIO1 is disabled: outputs SDA and SCL are in high impedance state, and P1.6 and P1.7 function as open-drain ports. With this bit set to logic 1 the SIO1 is enabled. The P1.6 and P1.7 port latches must be set to logic 1.
5	STA	Start flag. When the STA bit is set to logic 1 in slave mode, the SIO1 hardware checks the status of the I^2C-bus and generates a START condition if the bus is free. If STA is set to logic 1 while the SIO1 is in master mode, SIO1 transmits a repeat START condition.
4	ST0	Stop flag. With this bit set to logic 1 while in master mode, a STOP condition is generated. When a STOP condition is detected on the bus, the SIO1 hardware clears the STO flag. In the slave mode, the STO flag may also be set to logic 1 to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO1 hardware behaves as if a STOP condition has been received and releases SDA and SCL. The SIO1 then switches to the 'not addressed' receiver mode. The STO flag is automatically cleared by hardware.
3	SI	SIO1 interrupt flag. When this flag is set to logic 1, an acknowledge is returned after any one of the following conditions: • A START condition is generated in master mode • Own slave address received during AA = 1 • General call address received while S1ADR[0] = 1 and AA = 1 • Data byte received or transmitted in master mode (even if arbitration is lost) • Data byte received or transmitted as selected slave • STOP or START condition received as selected slave receiver or transmitter.
2	AA	Assert acknowledge. When set to logic 1 an acknowledge will be returned during the acknowledge clock pulse on SCL when: • Own slave address is received • General call address is received while S1ADR[0] = 1 • Data byte is received while device is a selected slave. With AA = 0 no acknowledge will be returned. Consequently, no interrupt is requested when the 'own slave address' or general call address is received.
1 and 0	CR1 and CR0	Together with CR2 these bits determine the serial clock frequency when SIO1 is in master mode, see Table 30.

Table 30 I^2C-bus bit frequencies in master mode

CR2	CR1	CR0	$f_{\mu C\_CLK}$ DIVIDED BY	I^2C-BUS BIT FREQUENCY (kHz) AT $f_{\mu C\_CLK}$				
				0.9 MHz	3.580 MHz	7.16 MHz	14.32 MHz	21 MHz
0	0	0	10	90	358	–	–	–
0	0	1	20	45	179	358	–	–
0	1	0	30	30	119	239	–	–
0	1	1	40	22	90	179	358	–
1	0	0	80	11	45	89.5	179	269
1	0	1	120	7.5	30	59.7	119	179
1	1	0	160	5.6	22	44.8	89.5	134
1	1	1	–	–	–	–	–	–

It should be noted that any I^2C-bus device tolerates a maximum and sometimes a minimum SCL frequency. The right setting of bits CR2, CR1 and CR0 using a specific microcontroller clock frequency is therefore important.

10.13.2 Special function register S1STA (D9H)

The status register S1STA is an 8-bit read-only register (see Table 31). Its contents may be used as a vector to a service routine. This optimizes the response time of the software and consequently the I^2C-bus.

Table 31 Status register S1STA (reset state 0xF8)

BITS	SYMBOL	DESCRIPTION
7, 6, 5, 4 and 3	SC4, SC3, SC2, SC1 and SC0	contains the status code defined by the I^2C-bus protocol
2, 1 and 0	–	not used, all bits are 0

10.13.3 Special function register S1DAT(DAH)

The data shift register S1DAT contains the serial data to be transmitted or data that has just been received (see Table 32). Bit 7 is transmitted or received first.

Table 32 Status register S1DAT (reset state 0x00)

BITS	SYMBOL	DESCRIPTION
7 to 0	bit 7 to bit0	I^2C-bus serial data

10.13.4 Special function register S1ADR (DBH)

This 8-bit 'own address register' can be loaded with the 7-bit address to which the controller will respond when programmed as a slave receiver/transmitter (see Table 33). The LSB bit GC is used to determine whether the general CALL address is recognized.

Table 33 Status register S1ADR (reset state 0x00)

BITS	SYMBOL	DESCRIPTION
7 to 1	address	own I^2C-bus address
0	GC	0: general CALL address is not recognized
		1: general CALL address is recognized

10.14 MSK modem

The MSK modem is used for in band signalling between handset and base in analog cordless telephone systems CT0, CT1 and CT1+. The MSK modem receiver and transmitter can be enabled separately. Receive and transmit interrupts can wake-up the microcontroller during its power saving Idle mode. The baud rates are programmable between 1200 and 4800 baud. Figure 14 shows the functional diagram of the MSK modem.

The MIN input is the alternative input of P3.7 and MOUT2 to MOUT0 is the alternative output of P3.0, P3.1 and P3.6. The RX and TX MUTE can be done in software by any pin of MA, P1, P3 and P2. The MTI and MRI interrupts are OR-ed together to a single interrupt called MSK_INT. So the MSK_IN interrupt handler should investigate the status of the MRI and MTI bit in the MCON SFR.

The MOUT2 to MOUT0 outputs and the MIN input are alternative functions of P3.0, P3.1, P3.6 and P3.7. The MOUT2 to MOUT0 outputs are '111' when the MSK transmitter is disabled (default after reset). So P3.0, P3.1, P3.6 and P3.7 can still be used as general purpose I/O ports. Setting bit 7 of MSTAT will invert the MIN polarity.

The modem has the following features:

- Full-duplex operation via 8-bit parallel interface
- The message is fully Manchester
- Automatic detection of 16-bit Manchester preamble pattern
- The last received 4 bits of the preamble pattern are programmable
- Receiver full, transmitter empty indication bits
- Manchester coding and decoding for clock recovery and early error detection
- Programmable input polarity
- Baud rate selection from 1200, 2400, 3600 or 4800 baud with internal modem timer
- Receiver and transmitter off-states with no power consumption.

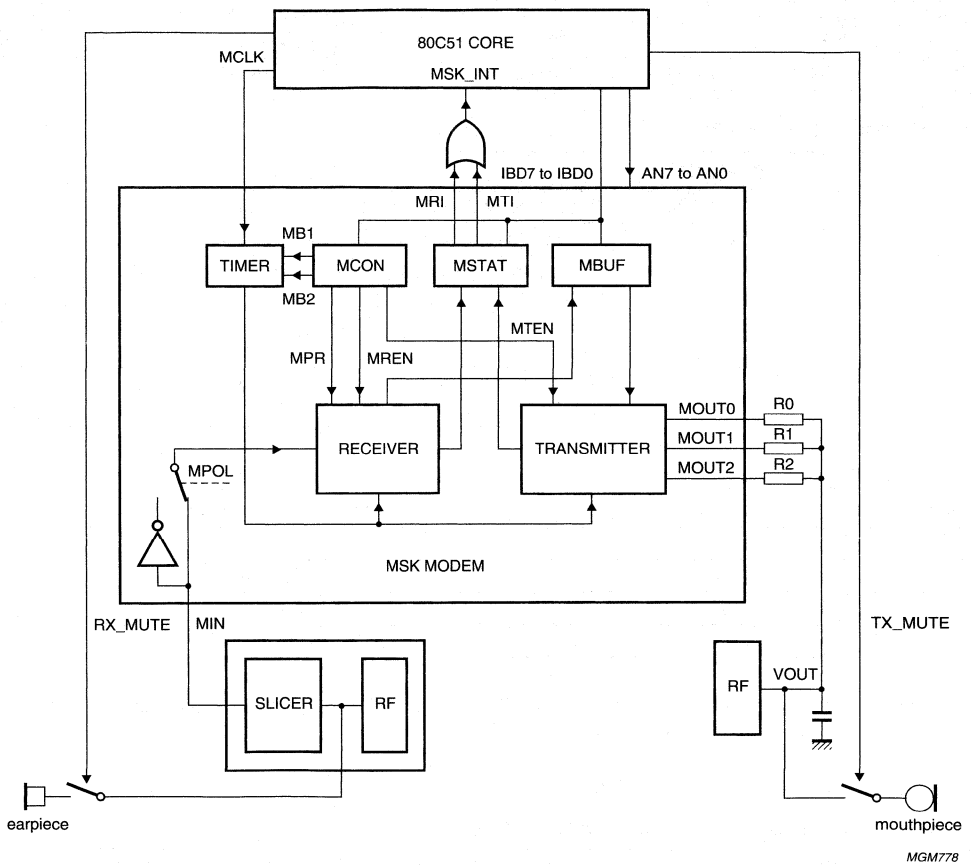


Fig.14 MSK modem functional diagram.

10.14.1 80C51 MICROCONTROLLER INTERFACE.

The modem block interfaces to the microcontroller via the interrupt signal MSK_INT and via the control and data SFRs MCON, MSTAT and MBUF. The MSK modem receiver and transmitter registers are both accessed via the special function register MBUF. Writing to MBUF loads the transmit register and reading from MBUF accesses a physically separate receive register.

10.14.1.1 MSK modem control register (MCON)

Table 34 MSK modem control register (SFR address D3H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MPR3	MPR2	MPR1	MPR0	MB1	MB0	MTEN	MREN

Table 35 Description of MCON bits

BIT	SYMBOL	DESCRIPTION
7 to 4	MPR3 to MPR0	These bits define the modems preamble pattern.
3 to 2	MB1 to MB0	These bits define the modem transmit/receive frequency (see Table 36).
1	MTEN	Modem transmitter enable. If set, the transmitter is active and MOUT3 to MOUT1 will get the value '100' if no data is transmitted. If reset, MOUT3 to MOUT1 will get the value '111' to zero the currents in the resistive DAC.
0	MREN	Modem receiver enable. If set, the modem receiver is active and scans for Manchester data.

Table 36 Baud rates.

MB1	MB0	MODEM BAUD RATE
0	0	1200 baud
0	1	2400 baud
1	0	3600 baud
1	1	4800 baud

If both the transmitter and the receiver are disabled (MTEN = 0 and MREN = 0), the clock of the MSK modem is switched off. It is advised to use this state for power saving.

10.14.1.2 MSK modem status register (MSTAT)

Table 37 MSK modem status register (SFR address CAH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MPOL	–	MRF	MRE	MRP	MRL	MTI	MRI

Table 38 Description of MSTAT bits

BIT	SYMBOL	DESCRIPTION
7	MPOL	MIN polarity switch. If MPOL = 1 the value of the MIN pin is inverted before being applied to the MSK block.
5	MRF	Modem receiver full flag. This bit is set when MBUF holds a newly received byte. MRF is reset if the receiver is disabled (MREN = 0) or by reading MBUF. This bit is read-only. Writing to it will have no effect.
4	MRE	Modem receiver error flag. Indicates the reception of a non-Manchester bit. This bit is set by hardware and is reset by reading MBUF, by disabling the receiver (MREN = 0) or by resetting MRI. This bit is read-only. Writing to it will have no effect.
3	MRP	Modem receiver preamble flag. This bit is set by hardware when the modem recognized the programmed preamble pattern (AAAH, MPR3 to MPR0) after locking the receiver clock (MRL = 1). MRP is reset by hardware if the receiver is disabled (MREN = 0) or if non-Manchester data is received (MRE = 1). This bit is read-only. Writing to it will have no effect.
2	MRL	Modem receiver clock locked flag. This bit is set when the clock of the receiver is locked, i.e. when the receiver has detected Manchester data but has not found the preamble pattern yet. MRL is reset when the receiver detects a non-Manchester bit or when the receiver is disabled. This bit is read-only. Writing to it will have no effect.
1	MTI	Modem transmit interrupt flag. Indicates MBUF is empty to accept a new byte for transmission. This bit is reset by writing to MBUF or by writing a logic 0 to it. Writing a logic 1 to MTI will set the bit. This allows to generate a hardware interrupt by software.
0	MRI	Modem receive interrupt flag. Indicates: Modem Receiver Full (MRF = 1) Modem Receiver Error (MRE = 1) Modem Receiver Preamble (MRP = 1) Modem Receiver Clock Locked (MRL = 1). This bit is reset by reading MBUF or by writing a logic 0 to MRI. A reset of MRI will also reset MRE. Writing a logic 1 to MRI will have no effect.

10.14.1.3 MSK modem data buffer (MBUF)

Table 39 MSK modem Data Buffer (SFR address C9H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 40 Description of MBUF bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	Writing to MBUF will load the data in the transmit buffer, and will automatically start a transmission at MOUT if the transmitter is enabled (MTEN = 1). A new byte can be loaded after MTI is set. If a new byte is loaded before the setting of MTI then the previous byte will be lost. After data has been received on pin MIN, indicated by bit MRI, the received byte can be read from register MBUF.

10.14.2 DATA TRANSMISSION

Data transmission is enabled if bit MTEN in register MCON is set to logic 1. If MTEN is set to logic 0 data transmission is disabled and MOUT2 to MOUT0 is set to '111' to zero the currents in the resistive DAC. Setting MTEN to logic 1 sets MOUT2 to MOUT0 to the idle value '100'. This results in a value close to $\frac{1}{2}V_{DD}$ on the output signal of the external DAC. Transmission is started by loading the first byte into register MBUF. All bytes are transmitted starting with the MSB.

A message is transferred in a block of three or more bytes, the first two bytes being the programmed Manchester preamble pattern. In order to insert the preamble pattern, the first two bytes AAH and AXH (with X being the MPR3 to MPR0 values programmed in the receiver MSK modem) are written to MBUF by software.

After this, the first byte of the message is written to MBUF. As soon as MBUF is ready to accept new input, signal MTI is set. A new byte written to MBUF automatically clears MTI. The time between two MTI interrupts is $t = 8 \times 1/\text{baud rate}$. (e.g. for 1200 baud, t = 6.7 ms). If no new byte is written to MBUF at the end of a byte transmission, the modem transmitter stops transmission and MOUT2 to MOUT0 is set to the idle state '100'. In this case MTI must be cleared explicitly. If MTEN is reset during transmission, the transmitter will finish the transmission of the current byte and then will set MOUT2 to MOUT0 to the off state '111'. No interrupt on MTI will be generated at the end of the transmission.

During reception, a digital PLL resynchronizes on the active transition of every bit. This allows a continuous transmission of long messages. Figure 15 shows a possible timing diagram of data transmission.

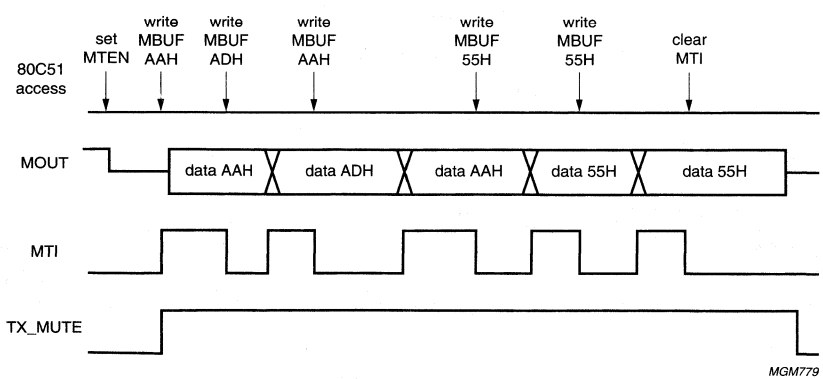


Fig.15 Data transmission timing diagram.

10.14.3 DATA RECEPTION

A message is received as a block of one or more data bytes. When enabled, the receiver starts sampling MIN and tries to detect a Manchester pattern. As soon as 3 consecutive Manchester bits are detected the receiver clock is locked (MRL = 1) and the receiver starts scanning the incoming data for the programmed Manchester preamble pattern. When the modem recognizes the preamble pattern, bit MRP is set to logic 1. If a non-Manchester bit is detected before finding the preamble pattern then MRL is reset and MRE is set to logic 1. The synchronization process has to restart. If the preamble pattern has been detected the receiver starts to Manchester decode the incoming data bits and shifts them into an internal register. After eight bits the contents of the internal register are copied to MBUF and the MRF bit is set to logic 1. The received byte can be read from MBUF while receiving continues in the internal register. If a non-Manchester bit is received during data reception then MRE is set to logic 1 and MRL and MRP are reset. The receiver has to resynchronize before receiving new data.

Whenever one of the bits MRF, MRE, MRP and MRL is set the MRI bit is also set and an MRI interrupt is generated. This means that when an MRI interrupt occurs the 4 status bits have to be polled by software. The bit MRL allows the software to decide very quickly whether an occupied channel contains Manchester coded data or not. The MRP bit is used to find the start of data transmission in a message that is repeated over and over again. MRE is used to detect a Manchester error, which is a violation of the Manchester coding rule that the received level should change in the middle of a bit cell. The MRF bit indicates that the data in MBUF is ready to be read by the software. During data reception the time between two settings of MRF (each one generating an MRI interrupt) is $t = 8 \times 1/\text{baud rate}$. Figure 16 shows an example of the timing diagram of data reception.

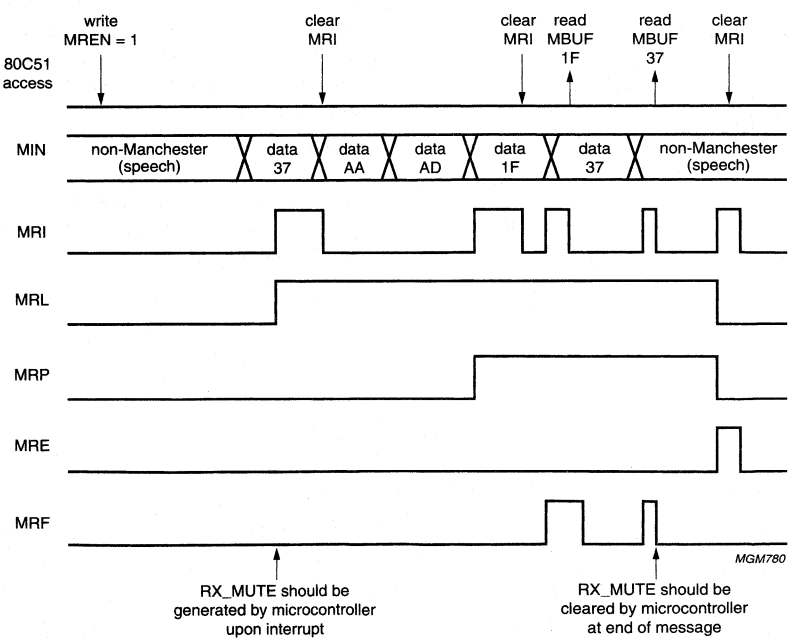


Fig.16 Data reception timing diagram.

10.14.4 Manchester coding of data

The bits of the data byte written in MBUF are Manchester encoded as shown in Fig.17. A logic 1 is coded as a LOW-to-HIGH transition in the middle of a bit cell, and a logic 0 is coded as a HIGH-to-LOW transition.
The Manchester encoded signal contains redundancy for early error detection in received bits. A non matching 1-0 or 0-1 pair indicates an error condition.
The Manchester encoded signal has a polarity change in each bit cell.

10.14.5 Waveform generation with MOUT2 to MOUT0

The 3 digital output pins MOUT2 to MOUT0 should be used as an input to a three bit external DAC. The signals can be connected via external resistors R2, R1 and R0 to a summation point and then be filtered with an external capacitor C1. This 3-bit DAC is shown in Fig.17.

Table 41 gives a relationship between MOUT2 to MOUT0, the resistor values and voltage VOUT.

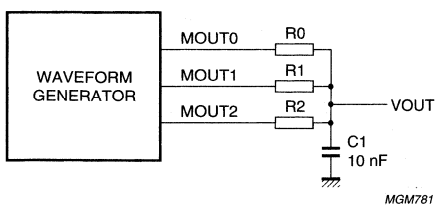


Fig.17 3-bit DAC with MOUT2 to MOUT0.

Table 41 VOUT as a function of MOUT and the resistor values

MOUT2 TO MOUT0	VOUT	RESISTOR VALUES
000	0	R0 = R R1 = 0.48 × R R2 = 0.25 × R
001	$0.14V_{DD}$	
010	$0.29V_{DD}$	
011	$0.43V_{DD}$	
100	$0.57V_{DD}$	
101	$0.71V_{DD}$	
110	$0.86V_{DD}$	
111	V_{DD}	

Figure 18 shows the possible waveforms that are produced by the waveform generator. The horizontal axis shows the sample counter on which the waveform changes its value. Each bit is built-up out of 2 × 40 samples (n × 3.456 MHz crystal; CKCON.6 = 0) or 2 × 42 samples (3.580 MHz; CKCON.6 = 1). The vertical axis shows the values of MOUT2 to MOUT0, forming the inputs of the resistive DAC. The first half of the waveform is determined by the previous and the current bit, whereas the second half of the waveform is determined by the current and the next bit to be transmitted. The count frequency of the sample counter depends on the programmed baud rate.

If the transmitter is disabled with MTEN set to logic 0, MOUT2 to MOUT0 is '111' to save power in the resistive DAC. If the transmitter is enabled and no data is transmitted, MOUT2 to MOUT0 has an Idle value of '100', which corresponds to $0.57V_{DD}$.

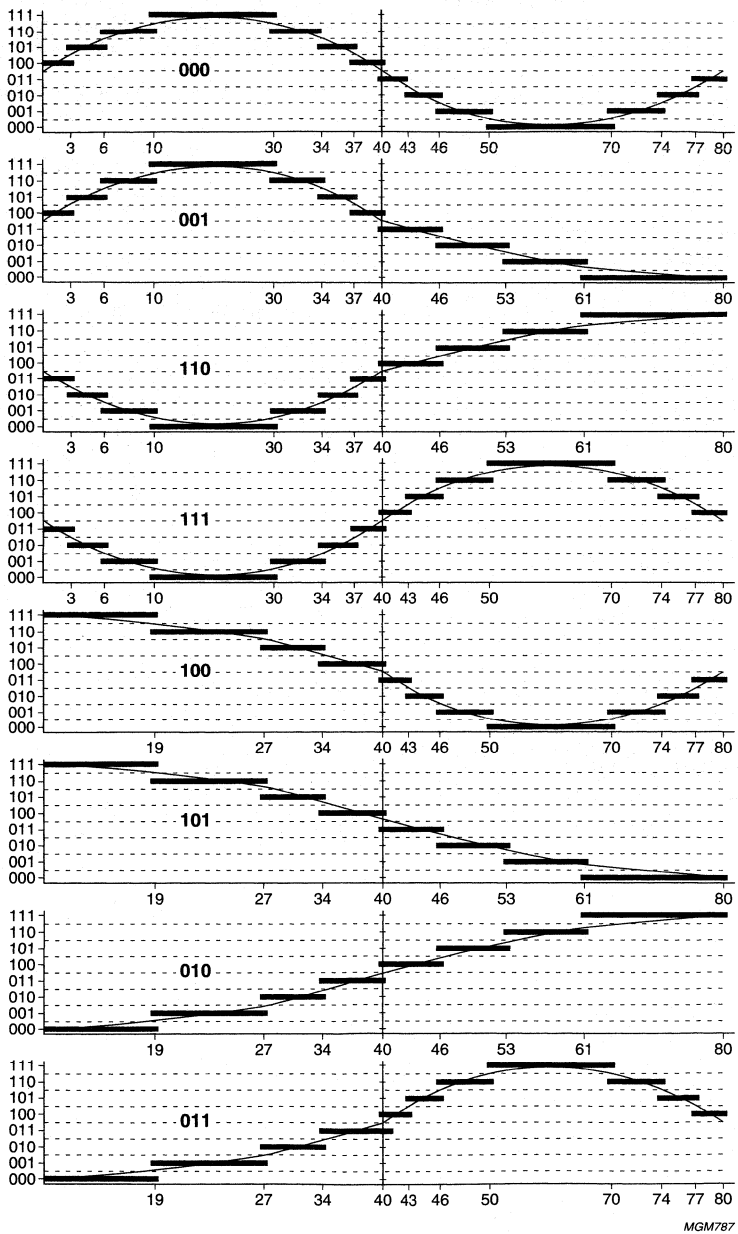


Fig.18 Waveforms with MOUT2 to MOUT0 for previous, current and next bits to be transmitted.

10.14.6 SYNCHRONIZATION

When enabled, the receiver samples pin MIN with a frequency f = 8 × baud rate. The sampled values are shifted into an 8-bit shift register. This register is regularly checked for containing samples that fulfil the Manchester coding rule i.e. whether there is a LOW-to-HIGH or a HIGH-to-LOW transition in the middle of the bit cell. The receiver searches for 3 consecutive sets of 8 samples that fulfil the Manchester coding rule. If these sets have been found the clock is locked (MRL = 1) and the receiver starts looking for the Manchester preamble pattern. From this point on the receiver uses a PLL to adjust the synchronization after each received Manchester bit.

10.15 DTMF generator

A versatile frequency generator section is provided (see Fig.19). The frequency generator includes precision circuitry for Dual Tone MultiFrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

One bit of the DTMF control register (DTCON) is used to select which line input is used for the CODEC.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

10.15.1 FREQUENCY GENERATOR DERIVATIVE REGISTERS

Table 42 gives the derivative addresses, mnemonics and access types of the three frequency generator derivative registers. When bit ETONE in register DTCON is set to logic 1 the TONE output is enabled. Bit LINESEL is used to select the alternative inputs for the line CODEC (see Chapter 13).

To reach the lowest possible power consumption, it is strongly recommended to write 00H in both frequency registers HGF and LGF. Reserved bits should not be changed.

Table 42 Addresses of the frequency generator derivative registers

ADDRESS	TYPE	MNEMONICS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C7H	W	DTCON (DTMF Control register)	reserved	reserved	–	LINESEL 0: LIFMIN1 1: LIFMIN2	–	–	reserved	ETONE
C6H	W	HGF (High Group Frequency register)	H7	H6	H5	H4	H3	H2	H1	H0
BEH	W	LGF (Low Group Frequency register)	L7	L6	L5	L4	L3	L2	L1	L0

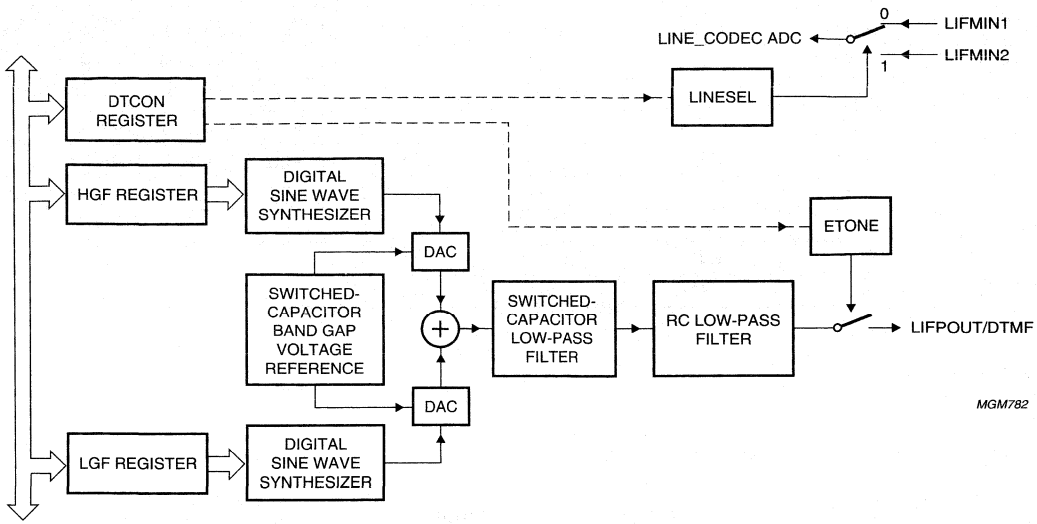


Fig.19 Frequency generator section and CODEC input selection.

10.15.2 Frequency registers

The two frequency registers define two frequencies. From these, the digital sine synthesizers together with the DACs construct two sine waves. Their amplitudes are precisely scaled according to the band gap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the low group frequency sine is attenuated by 2 dB compared to the amplitude of the high group frequency sine wave.

The two sine waves are summed and then filtered by on-chip switched-capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT CS203 recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components. '00H' in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain '00H', the whole frequency generator is shut off, resulting in lower power consumption.

A decimal value of 'x' in a frequency register yields a digital sine signal with frequency:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]} \quad \text{where } 60 \leq x \leq 255$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

10.15.3 DTMF frequencies

The input frequency to the frequency generator is f_{DTMF}. Assuming an oscillator frequency of a multiple of f_{DTMF} = 3.579545 MHz, the input clock division ratio (see Table 6) should be chosen such that f_{DTMF} = 3.579545 MHz. The DTMF standard frequencies can then be implemented as shown in Table 43.
The relationship between telephone keyboard symbols and the frequency register contents is given in Table 44.

Table 43 DTMF standard frequencies and their implementation

STANDARD FREQUENCY (Hz)	REGISTER VALUE		GENERATED FREQUENCY (Hz)		DEVIATION			
					(%)		(Hz)	
	f_{xtal1}[1]	f_{xtal2}[2]	f_{xtal1}	f_{xtal2}	f_{xtal1}	f_{xtal2}	f_{xtal1}	f_{xtal2}
697	DDH	D6H	697.90	695.65	+0.13	−0.19	+0.90	−1.35
770	C8H	C1H	770.46	770.57	0.06	0.07	0.46	0.57
852	B5H	AEH	850.45	853.75	−0.18	+0.21	−1.55	+1.75
941	A3H	9EH	943.23	939.13	+0.24	−0.20	+2.23	−1.87
1209	7FH	7AH	1206.45	1211.78	−0.21	+0.23	−2.55	+2.78
1336	72H	6EH	1341.66	1341.61	0.42	0.42	5.66	5.61
1477	67H	64H	1482.21	1473.15	+0.35	−0.26	+5.21	−3.85
1633	5DH	5AH	1638.24	1633.27	0.32	0.02	5.24	0.27

Notes

1. f_{xtal1} = 3.580 MHz.
2. f_{xtal2} = 3.456 MHz.

Table 44 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQUENCY PAIRS (Hz)	3.580 MHz CRYSTAL	
		LGF VALUE	HGF VALUE
0	(941 and 1336)	A3H	72H
1	(697 and 1209)	DDH	7FH
2	(697 and 1336)	DDH	72H
3	(697 and 1477)	DDH	67H
4	(770 and 1209)	C8H	7FH
5	(770 and 1336)	C8H	72H
6	(770 and 1477)	C8H	67H
7	(852 and 1209)	B5H	7FH
8	(852 and 1336)	B5H	72H
9	(852 and 1477)	B5H	67H
A	(697 and 1633)	DDH	5DH
B	(770 and 1633)	C8H	5DH
C	(852 and 1633)	B5H	5DH
D	(941 and 1633)	A3H	5DH
•	(941 and 1209)	A3H	7FH
#	(941 and 1477)	A3H	67H

10.15.4 MODEM FREQUENCIES

Again assuming an oscillator frequency f_{DTMF} = 3.579545 MHz, the standard modem frequency pairs summarized in Table 45 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains '00H', disabling low group frequency generation.

Table 45 Standard modem frequency pairs and their implementation

HGF VALUE	FREQUENCY (Hz) USING 3.580 MHz CRYSTAL		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9DH	980[1]	978.82	−0.12	−1.18
82H	1180[1]	1179.03	−0.08	−0.97
8FH	1070[2]	1073.33	0.31	3.33
79H	1270[2]	1265.30	−0.37	−4.70
80H	1200[3]	1197.17	−0.24	−2.83
45H	2200[3]	2192.01	−0.36	−7.99
76H	1300[4]	1296.94	−0.24	−3.06
48H	2100[4]	2103.14	0.15	3.14
5CH	1650[1]	1655.66	0.34	5.66
52H	1850[1]	1852.77	0.15	2.77
4BH	2025[2]	2021.20	−0.19	−3.80
44H	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

10.15.5 MUSICAL SCALE FREQUENCIES

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{DTMF} = 3.579545 MHz (see Table 46). It is suggested to define the frequency by the HGF register while the LGF contains '00H', disabling low group frequency generation.

Table 46 Musical scale frequencies and their implementation when using a 3.580 MHz crystal

NOTE	HGF VALUE	FREQUENCY (Hz) USING 3.580 MHz CRYSTAL	
		STANDARD[1]	GENERATED
D#5	F8H	622.3	622.5
E5	EAH	659.3	659.5
F5	DDH	698.5	697.9
F#5	D0H	740.0	741.1
G5	C5H	784.0	782.1
G#5	B9H	830.6	832.3
A5	AFH	880.0	879.3
A#5	A5H	923.3	931.9
B5	9CH	987.8	985.0
C6	93H	1046.5	1044.5
C#6	8AH	1108.7	1111.7
D6	82H	1174.7	1179.0
D#6	7BH	1244.5	1245.1
E6	74H	1318.5	1318.9
F6	6DH	1396.9	1402.1
F#6	67H	1480.0	1482.2
G6	61H	1568.0	1572.0
G#6	5CH	1661.2	1655.7
A6	56H	1760.0	1768.5
A#6	51H	1864.7	1875.1
B6	4DH	1975.5	1970.0
C7	48H	2093.0	2103.3
C#7	44H	2217.5	2223.3
D7	40H	2349.3	2358.1
D#7	3DH	2489.0	2470.4

Note

1. Standard scale based on A4 at 440 Hz.

10.16 LCD Enable (LE) control

The LE signal is an alternative output of P4.0 and can be turned on with ALTP bit 1. The LE signal can be used to connect to the E input of 68xx microcontroller compatible peripherals such as an LCD controller. If these peripherals have a slow access time the LE signal can be made HIGH earlier by setting bit 0 of ALTP. Bit 0 of ALTP will be cleared by hardware after the execution of a MOVX instruction. The ALTP register is described in more detail in Section 16.2.

Figure 20 shows the LE signal shapes for early read and/or write when the P4.0 alternate port function for LE is selected. In Fig.20, the $\overline{WR}$ signal is only shown for timing reference. Neither $\overline{WR}$ nor $\overline{RD}$ are physically connected to the display. The display RS and R/W pin can be connected to port 2 or port MA pins (logic 0 after reset) and controlled by software. The early LE timing hardware makes it possible to access LCD drivers (or other peripheral devices with the same interface) which require a large access time (>3 × μC_CLK).

The display LE pin (P4.0) rising edge is determined by software, by setting bit 0 and bit 1 of the ALTP SFR.

In order to latch the Port 0 data at the correct moment, the falling edge is determined by internal hardware. This generates, for the LCD write operation, an LE falling edge at 0.5 of a microcontroller clock before the Port 0 data is removed, such that the LCD data hold time requirement is always fulfilled.

Figure 21 shows the LE signal shape for normal read and/or write when the P4.0 alternate port function for LE is selected. Again, the $\overline{WR}$ signal is only shown for timing reference. Both the rising and falling edges of the display LE pin (P4.0) are determined by hardware if only bit 1 of the ALTP SFR is set. This generates, for the LCD write operation, an LE falling edge at 0.5 of a microcontroller clock before the falling edge of $\overline{WR}$, such that the LCD data hold time requirement is always fulfilled.

The normal LE timing is actually the inverted value of either the $\overline{RD}$ or $\overline{WR}$ signal. This timing can be used for peripheral devices that have an access time of less than 3 × μC_CLK.

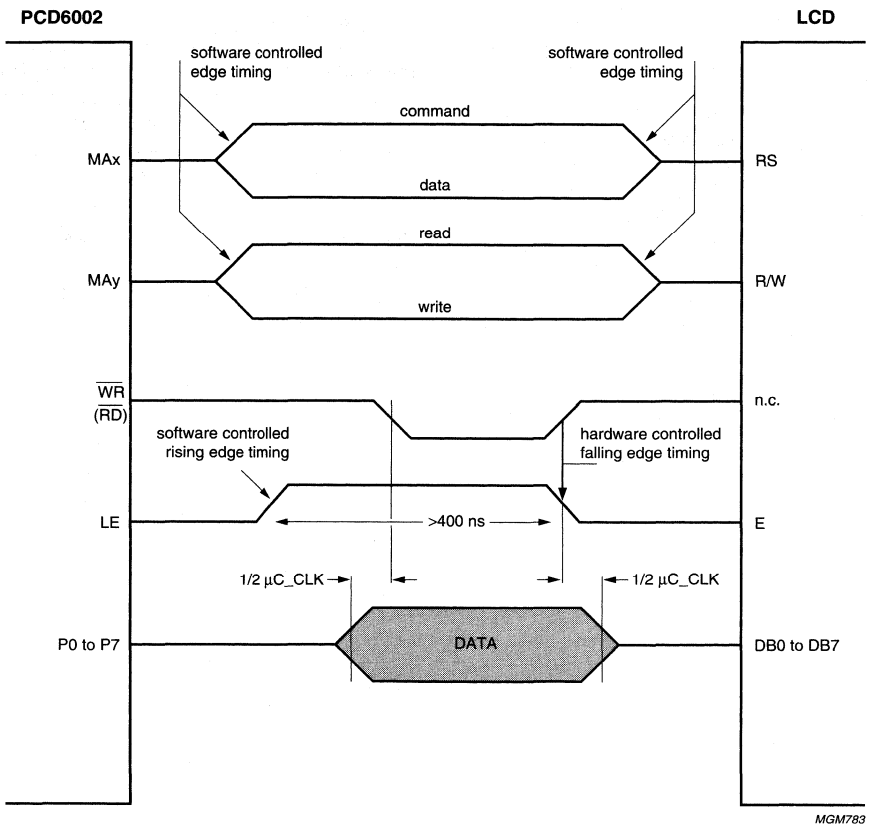


Fig.20 Early LE timing.

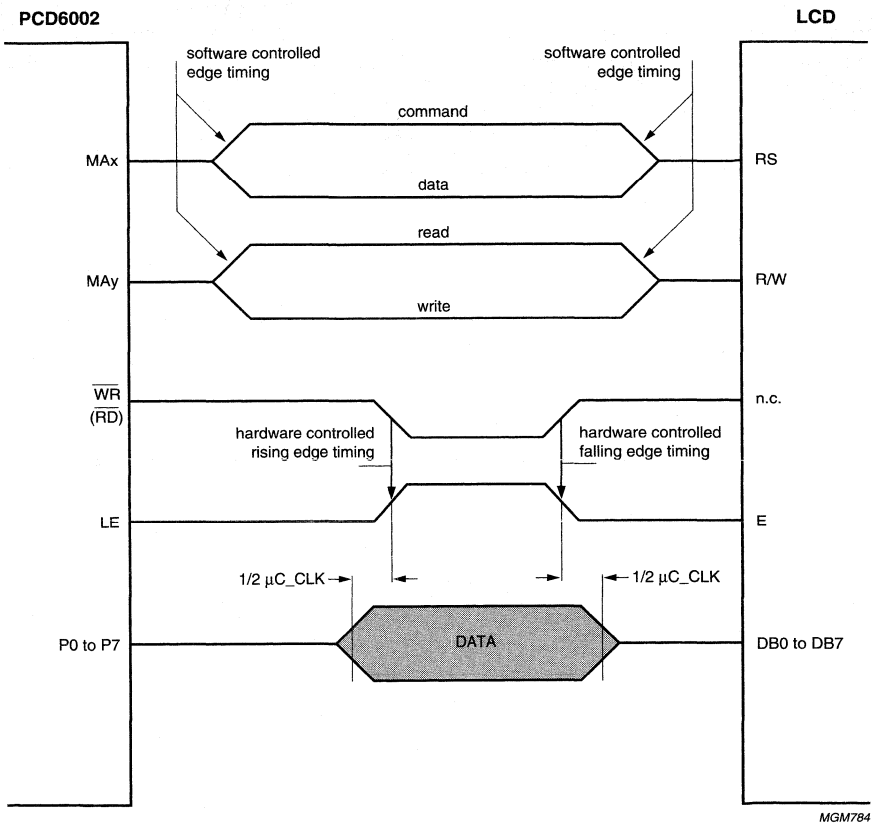


Fig.21 Normal LE timing.

11 DSP I/O REGISTERS

For the DTAM application, the DSP is connected with several peripherals as shown in Fig.22. Basically, the DSP is connected to the analog interfaces CODEC1 and CODEC2.

The DSP communicates with the peripherals via the DSP I/O registers. The data transfer is performed by the 16-bit XD data bus. The I/O registers of the different I/O units are 16 bits wide.

The microcontroller controls the DSP and is the link between an external speech memory and the DSP. The TICB provides the FS1 clock, which interrupts the DSP every 125 μs.

11.1 Interface to CODEC

The CODEC data buffers are used to exchange speech data between the DSP and the CODECs (see Fig.22).

The Digital Decimation Filter (DDF) writes equidistant in time 16-bit linear PCM samples to the DSP I/O registers CDC_DI0 to CDC_DI3 (address 01H to 04H for CODEC1 and address 09H to 0CH for CODEC2) at a rate of 32 kHz.

The Digital Noise Shaper (DNS) reads equidistant in time 16 bit linear PCM samples from the DSP I/O registers CDC_DO0 to CDC_DO3 (address 05H to 08H for CODEC1 and address 0DH to 10H for CODEC2) at a rate of 32 kHz. The input registers CDC_DI0 to CDC_DI3 and the output registers CDC_DO0 to CDC_DO3 are also called Data Input/Output (DIO) registers.

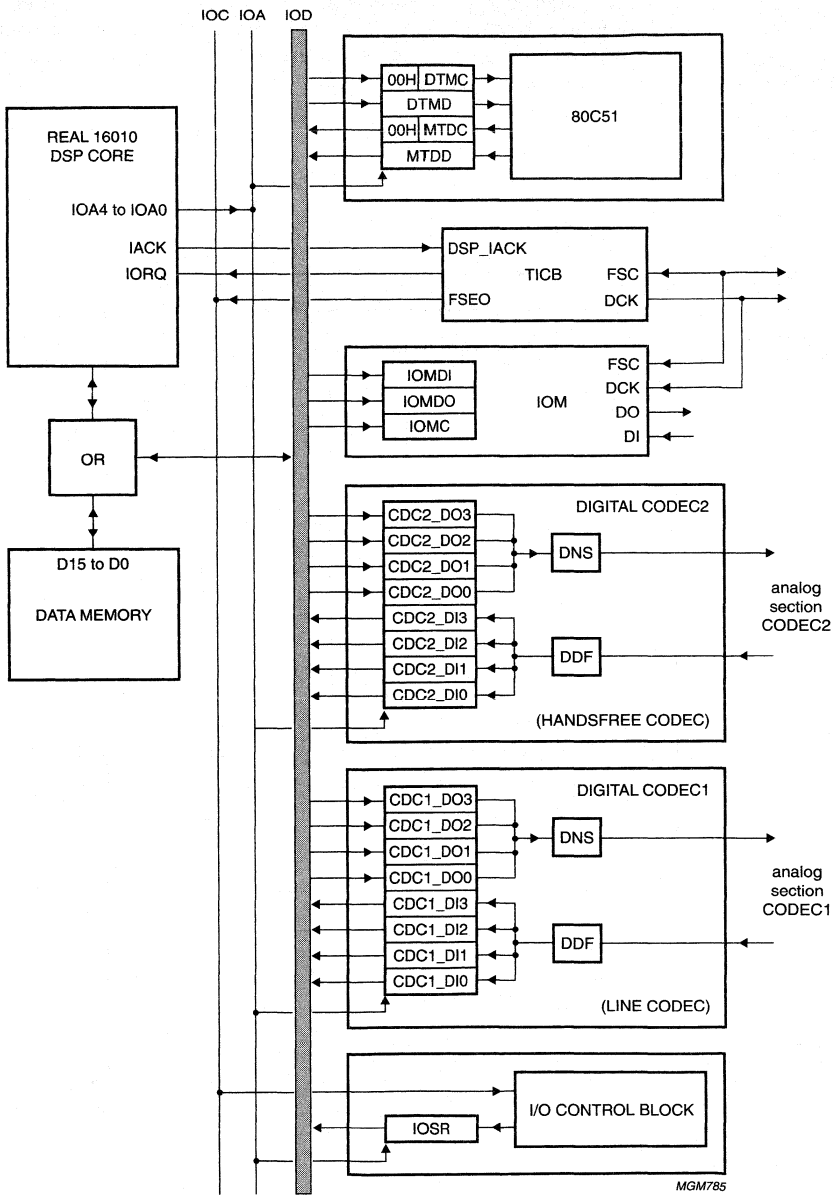


Fig.22 DSP I/O architecture.

12 EXTERNAL MEMORY INTERFACE

The external memory interface consists of the interface from the OTP to external flash memory and software debugging circuitry such as a metalink emulator or target debugger. The interface from the OTP to the remainder of the digital section is nearly the same as the OTP to external memory interface which facilitates the connection of external memory. The external memory interface also allows in-system programming of the OTP via the microcontroller. The external memory interface is shown in Fig.23.

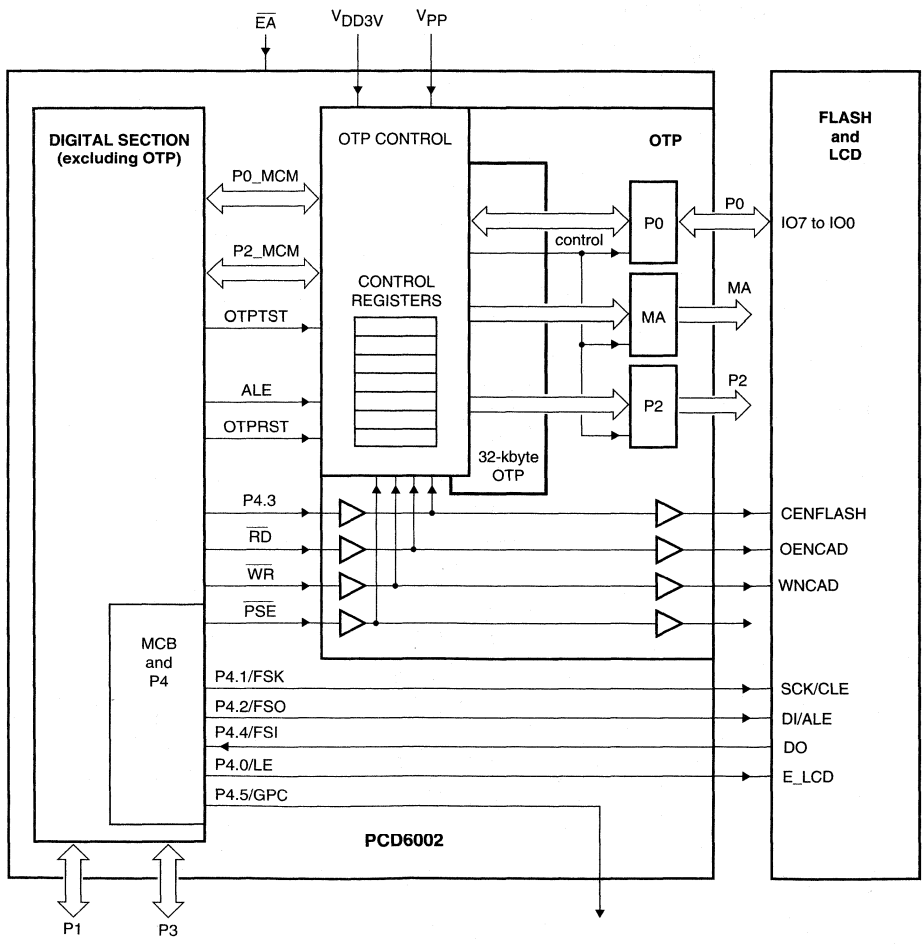


Fig.23 External memory interface.

The OTP will be activated by making $\overline{EA}$ logic 1. If $\overline{EA}$ is logic 0 external program memory can be connected and the OTP will be disabled. The OTP CNTRL block contains the MA and P2 generation and in-system programming logic and registers.

The P2 and MA latches have special enable signals. Appropriate bits MAGP (MA General Purpose) and P2GP (P2 General Purpose) in the control register make P2 and MA available as general purpose output ports or as the 80C51 address bus. The last option is necessary for target debugging ($\overline{EA}$ = 0), external ROM ($\overline{EA}$ = 0) or parallel flash memory (MAGP = 1 and P2GP = 1). In these cases external latches must be provided if the application needs the P2/MA output ports.

The MAGP and P2GP signals are bit 3 and 4 of the configuration register latch. MA will be a general purpose output port when MAGP is set to logic 0 by software (default after reset). If MAGP is set to logic 1 the MA port operates as the lower 8 bits of the program/data address bus. P2 will be a general purpose output port when P2GP is set to logic 0 by software (default after reset). If P2GP is set to logic 1 the P2 port operates as the higher 8 bits of the program/data address bus. The P2GP and MAGP bits of the ConfReg register in the OTP CNTRL block can only be read and written if P4.3 is logic 1.

Besides the configuration register, MA and P2 latches there are 4 other latches in the OTP CNTRL block used for system OTP programming. The OTP latches are mapped at address 200H to 206H of the external data memory and can only be accessed if P4.3 SFR bit is logic 1, (see Table 48).

- Register ADDL (8-bit): latches the low address byte for parallel/in-system programming.
- Register ADDH (8-bit): latches the high address byte for parallel/in-system programming.
- Register DATA (8-bit): latches the data which should be programmed in 'in-system programming mode'.
- Register TestControl (8-bit): In this register test modes can be selected and the sense amplifiers of the OTP block can be switched between self-timed (00H) and permanently on (08H). In Idle/Power-down/system-off mode, the sense amplifiers have to be in self-timed mode. If the value of this register is changed to a value other than 00H or 08H, proper operation of the OTP block and proper code fetching can not be guaranteed.
- Register ConfReg (6-bit): This is the configuration register. In this register single bits are set to control the functionality of the OTP chip.

The content of this register is given in Table 49. The output function of MA and P2 is determined by bits P2GP and MAGP.

When bit P2GP = 0 (reset value) the output P2 is latched and can be used as a general purpose output, for example to drive LEDs. Data can be written to register P2 with a MOVX command. When bit P2GP = 1 the input bus P2_MCM[7 to 0] is directly transferred to the output P2[7 to 0]. This mode is, for example, applied when using parallel flash memory. Output P2[7 to 0] then delivers the high address byte for the parallel flash memory. The output pins P2[7 to 6] are different from pins P2[5 to 0]. Pins P2[7 to 6] can be changed to inputs when in 'in-system programming mode'.

Bit VPon of the configuration register indicates high voltage for programming. VPon = 1 whenever there is a high voltage on input V_{PP} (V_{PP} = 12.5 to 13 V) indicating an in-system programming condition. VPon is the only bit of the configuration which is read only.

When bit CO = 1 (CO = Change Output) the configuration register changes the outputs P2[7 to 6] to inputs which are used for in-system programming (reset value CO = 0). The in-system programming algorithm is explained in detail in a separate application note.

When MAGP = 0 (reset value MAGP = 0) the output MA[7 to 0] can be used as a general purpose output. Otherwise output MA[7 to 0] serves as a latch (with ALE as enable signal) for the low address byte provided by the bus P0_MCM[7 to 0].

When SIG = 1 (SIG = signature byte) the 1-kbyte test memory array can be accessed during in-system programming mode. The test memory can be addressed either with SIG = 1 or with an address above the ordinary memory range of 32 kbytes (addresses > 7FFFH). The signature bytes (which are read only) are located in the test memory space.

Bit SEC is not used and must always be set to logic 0.

- Register MA (8-bit): If $\overline{EA}$ = 1 (internal OTP used) and MAGP = 0 (default after reset) the MA pins will output the contents of the MA register (0201H) which contains 00H after reset. The state of the MA pins can be changed by writing a new value to the MA register. This must be done with a MOVX instruction while the P4.3 bit is at logic 1.
- Register P2 (8-bit): If $\overline{EA}$ = 1 (internal OTP used) and P2GP = 0 (default after reset) the P2 pins will output the contents of the P2 register (0202H) which contains 00H after reset. The state of the P2 pins can be changed by writing a new value to the P2 register. This must be done with a MOVX instruction while the P4.3 bit is at logic 1.

Table 47 Data/program access and pin functions (normal mode)

$\overline{EA}$	ARD	P4.3	MAGP or P2GP	MOVX ADDRESS (HEX)	MOVX PHYSICAL LOCATION	$\overline{RD}/\overline{WR}$	MA or P2 FUNCTION[1]	PROG PHYSICAL LOCATION	$\overline{PSE}$
1	0	X	0	<0200	AUX-RAM	in-active	GP-IO	Internal	active[2]
			1		AUX-RAM	in-active	–		
	1	X	0		External[3]	active	GP-IO		
			1		External	active	D-address		
	X	1	0	0200–0206	OTP-REG	active	GP-IO		
			1		OTP-REG	active	D-address		
		0	0		External[3]	active	GP-IO		
			1		External	active	D-address		
		X	0	>0206	External[3]	active	GP-IO		
			1		External	active	D-address		
0	0	X	X	<0200	AUX-RAM	in-active	P-address	External	active
	1				External	active	PD-address		
	X	1		0200–0206	OTP-REG	active			
		0			External	active			
		X		>0206	External	active			

Notes

1. D-address: address of MOVX data; P-address: address of program code; PD-address: both addresses.
2. Does not conform to 80C51 standard.
3. MA and P2 do not hold the address which was used in the MOVX instruction if one of the bits in MAGP=0 or P2GP=0. This could lead to unexpected behaviour of the MOVX instruction.

Table 48 OTP control registers

OTP CONTROL REGISTER	ADDRESS P2/P0 (P4.3 = 1)	RESET VALUE	ACCESS
ConfReg	0200H	00H	R and W
MA	0201H	00H	R and W
P2	0202H	00H	R and W
TestControl	0203H	00H	R and W
ADDL	0204H	00H	R and W
ADDH	0205H	00H	R and W
DATA	0206H	00H	R and W

Table 49 Configuration register (ConfReg), reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	VPon (read only)	P2GP	MAGP	SEC	SIG	CO

12.1 Supported flash memories

Table 50 shows the ports that are available in an application using various flash memories.

For all types of flash memories shown in Table 50 (except for the parallel flash memory) at least 34 general purpose I/O pins can be used for the application (for example: display, line interface, keypad, LEDs). P0 can also be used for the application to connect memory mapped peripherals such as an LCD controller or keypad.

P0 pins have no output latch, so data written to this port will not remain there.

Table 50 Ports available for the application

FLASH MEMORY	PORTS USED BY FLASH			PORTS AVAILABLE FOR APPLICATION		
	I/O	I	O	I/O	I/O	O
CAD	P0	–	P4.1, P4.2 and P4.3	P1, P3, P4.0, P4.4 and P4.5	P0[1]	MA and P2
SPI/microwire	–	P4.4	P4.1, P4.2 and P4.3	P1, P3, P4.0 and P4.5	P0	MA and P2
I^2C-bus	P1.6 and P1.7	–	–	P1, P3 and P4	P0[1]	MA, P2 and P4.3
Parallel	P0	–	MA, P2, P4.0, P4.1, P4.2 and P4.3	P1, P3, P4.4 and P4.5	P0[1]	–

Note

1. P0 can be used as a data bus for other peripherals if not conflicting with the flash memory.

There are many different types of flash memories manufactured, and the PCD6002 can operate with many of them. Table 51 explains the most important characteristics of a few of the commercially available flash memories which can be connected to the PCD6002 directly.

Table 51 Ports available for the application

FLASH MEMORY TYPE NUMBER	MADE BY	INTERFACE TYPE	SIZE (Mbit)	MIN. WRITE SIZE (bytes)	MIN. READ SIZE (bytes)	MIN. ERASE SIZE (bytes)	t_{ACC} (ns)	SUPPLY (V)	TYPICAL STAND-BY CURRENT (μA)
AM29LV004	AMD	parallel 8	4	1	1	64 K	100	3	1
AM29LV400	AMD	parallel 8/16	4	1	1	64 K	100	3	1
MBM29LV004	Fujitsu	parallel 8	4	1	1	64 K	100	3	5
KM29V040[1]	Samsung	mux CAD	4	32	1	4 K	100	3	10
AT45DB041[1]	ATMEL	SPI	4	1[2]	1	264	–	3	10
NM29A040[1]	National Semiconductors	microwire	4	32	32	4 K	–	5	5
TMS29F040	Texas Instruments	parallel 8	4	1	1	64 K	60	5	25
TC58A040F[1]	Toshiba	microwire	4	32	32	4 K	–	5	50
M29V040	SGS Thomson	parallel 8	4	1	1	64 K	120	3	25

Notes

1. Supported by Philips PCD6002 API software.
2. With the aid of the internal flash data memory buffers.

The access time requirement of any external memory such as the OTP, parallel flash (PF), CAD flash or external ROM is explained in Table 52.

Table 52 Memory access time requirements

CASE	MEMORY TYPE	CEN CONNECTION	OEN OPERATION	t_{ACC} REQUIREMENT
1	ROM/OTP	VSS	$\overline{PSE}$	$t_{ACC} < (5/2 \times T_{\mu C\_CLK}) - delay$
2	CAD/PF	VSS	$\overline{RD}$	$t_{ACC} < (5 \times T_{\mu C\_CLK}) - delay$
3	ROM/OTP	ALE	$\overline{PSE}$	$t_{ACC} < (2 \times T_{\mu C\_CLK}) - delay$
4	CAD/PF	ALE	$\overline{RD}$	$t_{ACC} < (9/2 \times T_{\mu C\_CLK}) - delay$
5	ROM/OTP	$\overline{PSE}$	VSS	$t_{ACC} < (3/2 \times T_{\mu C\_CLK}) - delay$
6	CAD/PF	$\overline{RD}$ AND $\overline{WR}$	$\overline{RD}$	$t_{ACC} < (3 \times T_{\mu C\_CLK}) - delay$

The delay parameters are defined by the delay (capacitive load) of the address bus, data bus, $\overline{RD}$ and $\overline{PSE}$ pins, the power supply voltage and the internal delay in the OTP and digital section. As shown in Table 52 there is a trade-off between power consumption and memory speed requirement.

12.1.1 DTAM EXTERNAL MEMORY USING A PARALLEL FLASH

A parallel flash memory can be connected to the PCD6002 chip as shown in Fig.24. The MAGP and P2GP bits in the OTP configuration register must be set. Clearing P4.3 will enable the flash memory.

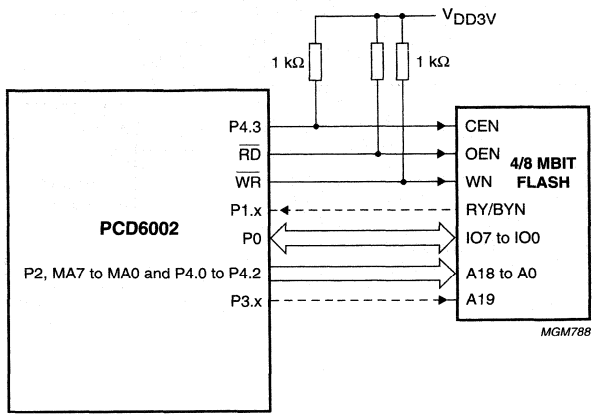


Fig.24 Parallel flash memory connection.

12.1.2 DTAM EXTERNAL MEMORY INTERFACE USING A 4-WIRE SERIAL FLASH

A 4-wire serial flash memory (such as SPI or microwire flash memory) can be connected to the PCD6002 chip as shown in Fig.25. P4.3 must be pulled up to 5 V with a resistor when using a 5 V serial flash memory. P4.1 and P4.2 must be pulled to 3 V with a resistor. When using a 5 V flash memory the DO output of the flash must be level-shifted to 3 V by means of two resistors of 1 kΩ and 1.5 kΩ.

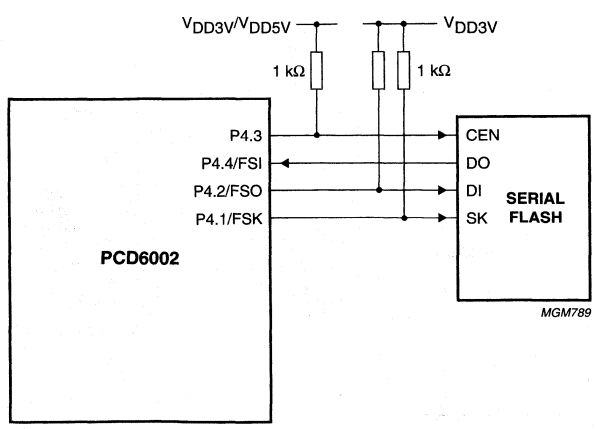


Fig.25 Serial flash memory connection.

12.1.3 DTAM EXTERNAL MEMORY INTERFACE USING AN I²C-BUS SERIAL FLASH

An I²C-bus flash memory can be connected to the PCD6002 as shown in Fig.26.

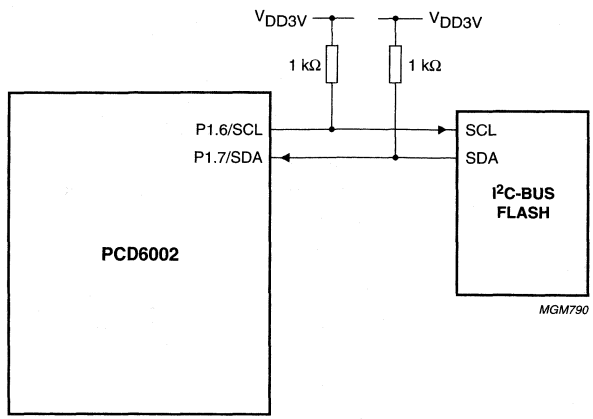


Fig.26 I²C-bus serial flash memory connection.

12.1.4 DTAM EXTERNAL MEMORY USING A CAD FLASH

A CAD flash memory can be connected to the PCD6002 as shown in Fig.27. P4.3 must be pulled up to 3 V with a resistor. P4.x, P4.y, $\overline{RD}$ and $\overline{WR}$ must also be pulled to 3 V with a resistor. Which of the P4 pins are used to control CLE and ALE is defined by the Application Programming Interface (API). Please refer to the API specification for more details.

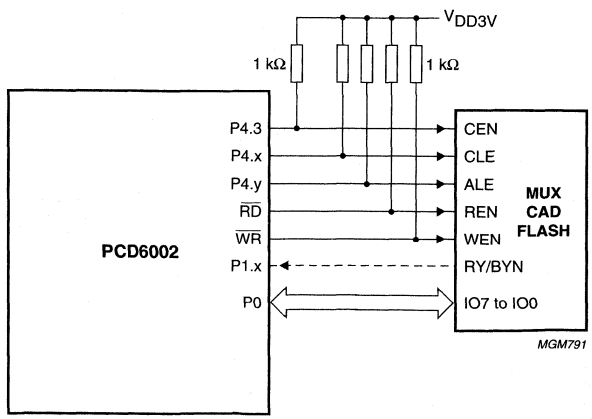


Fig.27 Muxed CAD flash memory connection.

12.2 DTAM external interface during target debugging

If the PCD6002 is used with the tScope-51 target debug tool the DTAM chip needs executable SRAM where the monitor program MON51 can store the program code. This SRAM is accessible by means of the $\overline{RD}$, $\overline{WR}$ and $\overline{PSE}$ signals. Connection to parallel flash memory with XSRAM and ROM is the worst case situation. This case is shown in Fig.28. Since it is not a commercial system additional logic can be connected to the DTAM chip to create executable SRAM.

The target debug logic only consists of combinational logic:

- CENROM ≤ P2.7, P2.6 or P2.5
- CENFLASH ≤ P4.3
- CENXSRAM ≤ ($\overline{PSE}$ or not CENROM) and ($\overline{RD}$ or not CENFLASH)
- OENXSRAM ≤ $\overline{PSE}$ and $\overline{RD}$
- $\overline{WR}$XSRAM ≤ $\overline{WR}$.

The port restore logic is necessary to make the MA/P2/P0 ports available for the application.

The MON51 program is assumed to be in the lowest 8 kbytes of the ROM. If the flash memory should be accessed, clear P4.3 to logic 0. Now the MON51 program has no access to the XSRAM with $\overline{RD}$ so no breakpoints are allowed in the code area when P4.3 is logic 0. Set P4.3 to logic 1 again after the flash memory access to enable MON51 again to access the XSRAM.

Target debugging requires I^2C-bus and one general purpose input port. This means that at least 33 I/O ports are available for the application (not using parallel flash) during target debugging.

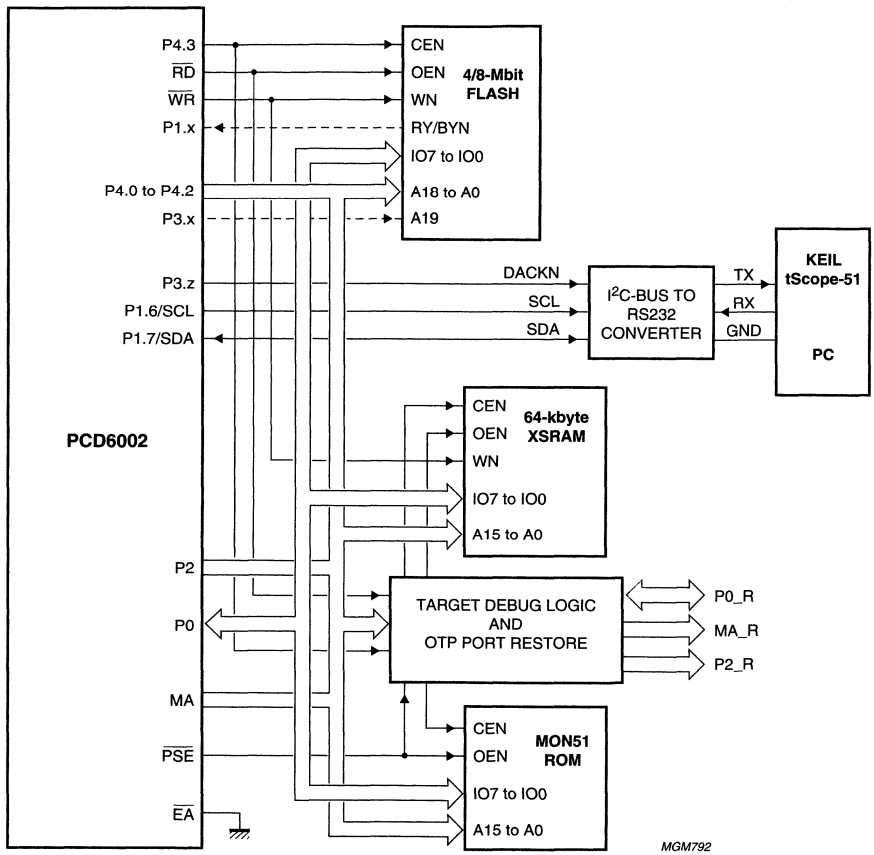


Fig.28 Flash, XSRAM and MON51 ROM memory connection.

13 THE CODECS

13.1 Definitions

In the description of the codec the amplitude units are written in dB. The following definitions apply:

- **dBm** used for absolute analog signal power levels. 0 dBm equals 1 mW in 600 Ω. A single sine wave signal with a power level of 0 dBm corresponds to an RMS voltage value of 774.6 mV.
- **dBm0** used for relative digital signal power levels. 0 dBm0 is defined in *"CCITT Recommendation G.711 (Section 4, Table 5)"*. It follows that the maximum signal power level is 3.14 dBm0 (A-law). Thus 3.14 dBm0 is the RMS value of a sine wave signal whose peaks just reach the full-scale of the digital code. For the (internal) bitstream signal (output of ARS and DNS) the positive full-scale value is a continuous stream of 'ones', whereas the negative full-scale value is a continuous stream of 'zeroes'. For the (internal) digital 14 or 16-bit words, represented in 2s complement (MSB first) the positive full-scale value is a 'zero' followed by 13 or 15 'ones', whereas the negative full-scale value is a 'one' followed by 13 or 15 'zeroes'.
- **dBmp** used for absolute analog signal power levels with psophometric weighting according to *"CCITT Recommendation G.223"*. This unit is used to express analog noise power levels.
- **dBm0p** used for relative digital signal power levels with psophometric weighting.
- The **uniform PCM reference point** is the (virtual) signal node in the DSP at the input of the ADPCM encoder for the analog-to-digital speech path. The uniform PCM reference point is the (virtual) signal node in the DSP at the output of the ADPCM decoder for the digital-to-analog speech path. These definitions apply for both the handset and base station version.
- **dB** is used for the signal level gain between any two nodes within the speech path. As different signal representations are used within the speech path, the gain value depends on the used signal definitions.

13.2 CODEC architecture

The PCD6002 is provided with two CODECs that perform the analog-to-digital and digital-to-analog conversion of speech signals. As shown in Fig.29, the CODECs are the interfaces between the external analog peripherals and the DSP. CODEC1 is used for the line interface and CODEC2 is used for the loudspeaker and the microphone. For convenience the DTMF block and associated registers are also shown in Fig.29.

The DTCON register bit DTCON.4 selects the input to CODEC1 (LIFMIN1 or LIFMIN2). The DTCON register bit DTCON.0 selects either the DTMF or CODEC output (see Table 42 in Section 10.15).

The main CODEC functions are:

- AMP: Pre-amplifier
- ARS: Analog Receive Sigma-delta ADC
- DDF: Digital Decimation Filter
- DNS: Digital Noise Shaper
- ATD: Analog Transmit DAC.

For CODEC1 the balanced line interface input is fed to the ARS block that performs analog-to-digital conversion and has an analog amplifier. This amplifier has a fixed gain of 6 dB and an additional 0 to 15 dB programmable amplification range. This programmable range is used by the microcontroller on command of the DSP to perform limiting or automatic gain control. The total gain then results in 6 to 21 dB. The analog data is converted by ARS to a bitstream. The basic sampling frequency f_s is 8 kHz. The DDF decimates the bitstream down to 16-bit linear PCM data. The DDF has a gain of 3.14 dB to achieve a uniform reference point at the DSP input for linear PCM data. Finally, the DSP will decimate this data to 16-bit linear PCM data at a rate of 8 kHz.

The reverse operation is performed in the transmit path. The DSP produces 16-bit linear PCM data to the digital noise shaper. The ATD converts the bitstream into an analog signal. The converter has a programmable amplification range of 15 dB.

CODEC2 is built-up in a similar manner as CODEC1. The only difference is the microphone amplifier before the ADC. This will amplify the balanced analog (microphone) signal in the receive path with a fixed 16 dB. For direct connection of an external microphone, a software on/off switchable supply voltage is available.

For control of the 2 CODECs several registers are available:

- DTCON: for selecting the input to CODEC1
- CDVC1: the volume control register for CODEC1
- CODTR: the test mode control register for both CODECs
- CDVC2: the volume control register for CODEC2.

Table 53 gives the bit assignment for registers CDVC1 and CDVC2; Table 54 shows the digital-to-analog and analog-to-digital gain values in the corresponding CODEC1 and CODEC2 paths.

Table 53 CDVC1 (BBH) and CDVC2 (BCH) bit assignment; reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
D/A3	D/A2	D/A1	D/A0	A/D3	A/D2	A/D1	A/D0

Table 54 Digital-to-analog and analog-to-digital gain values

BITS 7 TO 4	DIGITAL-TO-ANALOG GAIN	BITS 3 TO 0	ANALOG-TO-DIGITAL GAIN(1)	
			CODEC1(2)	CODEC2(3)
0000	−13 dB	0000	6 dB	22 dB
0001	−12 dB	0001	7 dB	23 dB
0010	−11 dB	0010	8 dB	24 dB
0011	−10 dB	0011	9 dB	25 dB
0100	−9 dB	0100	10 dB	26 dB
0101	−8 dB	0101	11 dB	27 dB
0110	−7 dB	0110	12 dB	28 dB
0111	−6 dB	0111	13 dB	29 dB
1000	−5 dB	1000	14 dB	30 dB
1001	−4 dB	1001	15 dB	31 dB
1010	−3 dB	1010	16 dB	32 dB
1011	−2 dB	1011	17 dB	33 dB
1100	−1 dB	1100	18 dB	34 dB
1101	0 dB	1101	19 dB	35 dB
1110	1 dB	1110	20 dB	36 dB
1111	2 dB	1111	21 dB	37 dB

Notes

1. 3 dB digital gain of DDF hardware block is not included here.
2. System application should be such that the maximum line input signal level does not exceed −6 dBm to avoid distortion. At a minimum line input level of −21 dBm full-scale control the internal ADC can be achieved by a maximum gain setting of 21 dB.
3. System application should be such that the maximum differential microphone input signal level does not exceed −22 dBm to avoid distortion. At a minimum microphone input level of −37 dBm full-scale control the internal ADC can still be achieved by a maximum gain setting of +37 dB. The high dynamic range of the ADC allows for additional digital gain up to 18 dB by the DSP.

The analog, analog-to-digital and digital-to-analog parts of both CODECs can be independently activated by the SYMOD register; see Table 3. Bit 4 of SYMOD is used to activate the microphone supply voltage, if the bit is logic 0 the supply is off.

The balanced microphone input has an input resistance of approximately 200 kΩ, and the balanced line interface input has an input resistance of approximately 20 kΩ. The output resistance of the balanced CODEC outputs is approximately 10 Ω with a typical output level of 1350 mV (RMS).

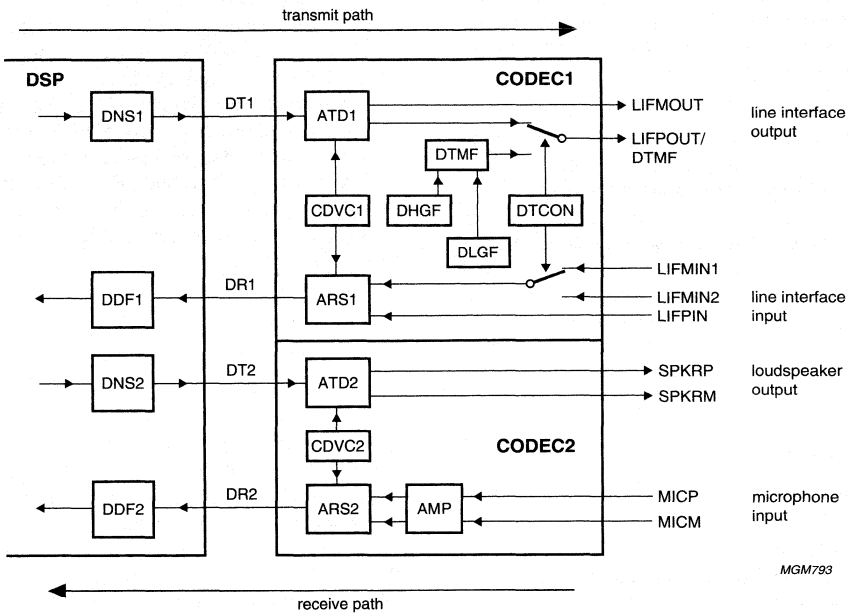


Fig.29 Block diagram of CODECs.

14 ANALOG VOLTAGE REFERENCE

14.1 Band gap reference

The Analog Voltage Reference (AVR) circuitry includes a band gap circuit with a nominal output voltage of approximately 1.20 V. This voltage is used by the Power-on reset block and by the analog voltage source to generate the reference voltage V_{ref}. Block AVR is always on, even in system-off mode, and will consume only a few μA of current.

The output AVR is directly connected to the Power-on reset block and it determines the Power-on reset threshold levels accuracy in first order. The connection from AVR to Analog Voltage Source (AVS) is via an internal series resistor of approximately 200 kΩ. The voltage after this resistor is connected to pin V_{BGP}, which allows an external capacitor (100 nF) to be connected to filter out any noise from AVR, so preventing it from entering into the AVS. With this configuration the noise at pin V_{BGP} will be approximately −115 dBmp. The pin also allows a direct measurement of the band gap voltage, but no current must be drawn.

14.2 Analog voltage source

The Analog Voltage Source (AVS) generates the following voltages:

- A precise reference voltage V_{ref}. The value in register VREFR determines the V_{ref}. In the application this voltage should be tuned to 2000 mV, since it will determine the absolute accuracy of the auxiliary analog-to-digital and digital-to-analog conversion, as well as the gains in the CODEC analog-to-digital and digital-to-analog paths. V_{ref} is the direct output of an operational amplifier which can source an output current, and not sink. An external capacitor of 10 to 30 μF should be connected between V_{ref} and V_{SSA} for stability and noise performance.

  The reference voltage can also directly supply an external electret microphone via pin V_{MIC}. The switch between V_{ref} and V_{MIC} is controlled via bit 4 of the SYMOD special function register.
- An analog output voltage DAOUT. This voltage can be set between approximately 8 mV (1 LSB = V_{ref}/256) and V_{ref} (= 2000 mV) by changing the register GPDAR. This large range is possible while no operational amplifier is used. This causes a relatively high output resistance with a settling time of approx. 10 ms. The dynamic switching of DAOUT causes the output resistance to be dependent of the actual load on DAOUT. This effect can be cancelled if an external capacitor larger than 500 pF is connected between DAOUT and V_{SSA}. This will however result in a slower settling time of the output voltage, to approx. 30 ms.
- The internal analog common mode voltage V_{acm}, used in the CODEC. The voltage is fixed to $V_{ref} \times 161/256$ and cannot be changed by any register.
- The internal voltage V_{adc}, used only when an analog-to-digital conversion is executed.

As mentioned above, the reference voltage V_{ref} has to be adjusted in the application to 2000 mV. For this purpose the VREFR special function register has been defined. It is reset to 9AH. The reset state should ensure that the reference voltage is approximately 2000 mV. Exact adjustment has to be done under software control using the VREFR register, where increasing the VREFR value will decrease the reference voltage.

Table 55 VREFR (BAH) bit assignment; reset state 9AH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	V_{ref} bit 6	V_{ref} bit 5	V_{ref} bit 4	V_{ref} bit 3	V_{ref} bit 2	V_{ref} bit 1	V_{ref} bit 0

15 INPUT/OUTPUT MODULE

15.1 Features

The Input/Output Module (IOM) block in the PCD6002 is a 4-wire serial interface which performs the following functions:

- Digital interface with up to two 64 kbits/s channels at a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8), complying with the *"IOM-2 specifications"* (IOM-2 is a registered trademark of Siemens AG)
- Digital interface with 32 slots/frame and non-doubled data clock, compatible with the digital interface of some speech CODEC ICs
- Autonomous storing/fetching of data into/from the DSP I/O registers
- Byte or word (16 bits) transfer.

15.2 Pin description

The following pins are used by the IOM interface:

- DI: serial data input with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8)
- DO: serial data output with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8)
- FSC: 8 kHz frame synchronization input/output
- DCK: data clock input/output with twice the data transmission frequency on DI and DO, except in the non-doubled data clock mode (see Section 15.3).

These pins are alternative functions of P3. When activated, DO is an open-drain pin, as many devices must be able to write on the same data line in a time-multiplexed mode. Therefore DO must be externally pulled up. FSC and DCK are inputs or push-pull outputs, depending on the IOM being in slave or master mode. Activation of the IOM alternative functions of P3 and switching between slave or master mode is controlled by the SFR ALTP, bit 6 and 5 respectively (see Section 16.2).

15.3 Functional description

The digital interface of the PCD6002 can work at several bit rates, summarized in Table 56. A particular bit rate is selected by writing the 3-bit code given in the first column of the table into the IOM Control register bits IOMC.15, IOMC.14 and IOMC.13. Choosing the code '000' or '001' deactivates the IOM interface and stops all the transactions on the IOM bus. This is the default state after reset.

The PCD6002 IOM can be master or slave. After reset the IOM is in slave mode. Switching between slave or master mode is controlled by the SFR ALTP, bits 5 and 6 respectively (see Section 16.2 for more details). In slave mode both FSC and DCK are inputs. In master mode both FSC and DCK are outputs. In master mode FSC and DCK are generated by the TICB (see Section 9.1). Master mode should only be used in combination with the bit rate 768 kbits/s.

FSC is an 8 kHz framing signal for synchronizing data transmission on DI and DO. The rising edge of FSC gives the time reference for the first bit transmitted in the first slot of a speech frame. The number of slots per speech frame depends on the selected data rate. Each slot contains 8 data bits.

DCK is a data clock. Its frequency is twice the selected data rate in IOM mode. In speech mode, the DCK frequency is equal to the data rate (2048 kHz for 2048 kbits/s).

DI is the serial data input. Data arriving on DI in packets of 8 bits (A-law PCM encoded data) or 16 bits (linear PCM data) is stored temporarily in an IOM data buffer, from where it is processed by the on-chip DSP. On the other hand, data written into the IOM data buffers by the DSP is shifted out on pin DO.

There are two IOM data buffers, allowing the use of two 8-bit channel. One channel is 64 kbits/s in case of A-law PCM encoded data and 128 kbits/s if linear PCM data is transferred, in which case two consecutive slots are used.

The speech mode is implemented to support the codec interface of some speech compression ICs. This mode is very similar to the IOM 32 slots mode, the main difference being the non-doubled data clock. See Section 15.6 for timing information.

Table 56 IOM modes

CODE IOMC[15 TO 13]	MODE
000 or 001	inactive (default after reset)
010	IOM slave mode, 256 kbits/s in 4 slots/speech-frame
011	IOM slave mode, 512 kbits/s in 8 slots/speech-frame
100	IOM master/slave mode, 768 kbits/s in 12 slots/speech-frame
101	IOM slave mode, 1024 kbits/s in 16 slots/speech-frame
110	speech slave mode, 2048 kbits/s in 32 slots/speech-frame; note 1
111	IOM slave mode, 2048 kbits/s in 32 slots/speech-frame

Note

1. The speech mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCK.

15.4 IOM data buffers

Tables 57 and 58 show the two 16-bit DSP registers used as data buffers: IOMDI for storing inbound data and IOMDO for the outbound data. The high byte stores the data of buffer 1, the low byte the data of buffer 0.

Table 57 IOMDI bit assignment; reset state 00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOM inbound data buffer 1								IOM inbound data buffer 0							

Table 58 IOMDO bit assignment; reset state 00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOM outbound data buffer 1								IOM outbound data buffer 0							

15.5 IOM Control register

The bit rates, the selection of active slots on the IOM interface and the logic connection between an IOM slot and an IOM data buffer is defined in register IOMC. The IOM modes which can be selected are listed in Table 56.

Writing of the IOMC register is done via the API software (Application Programming Interface). Please refer to the API specification for more details.

Table 59 IOMC bit assignment; reset state 00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOM mode select			IOM buffer 0: slot position					spare	buffer 0 active	buffer 1 active	IOM buffer 1: slot position				

15.6 Timing

The timing on the 4-wire interface is given in Fig.30 for the IOM mode, and in Fig.31 for the speech mode.

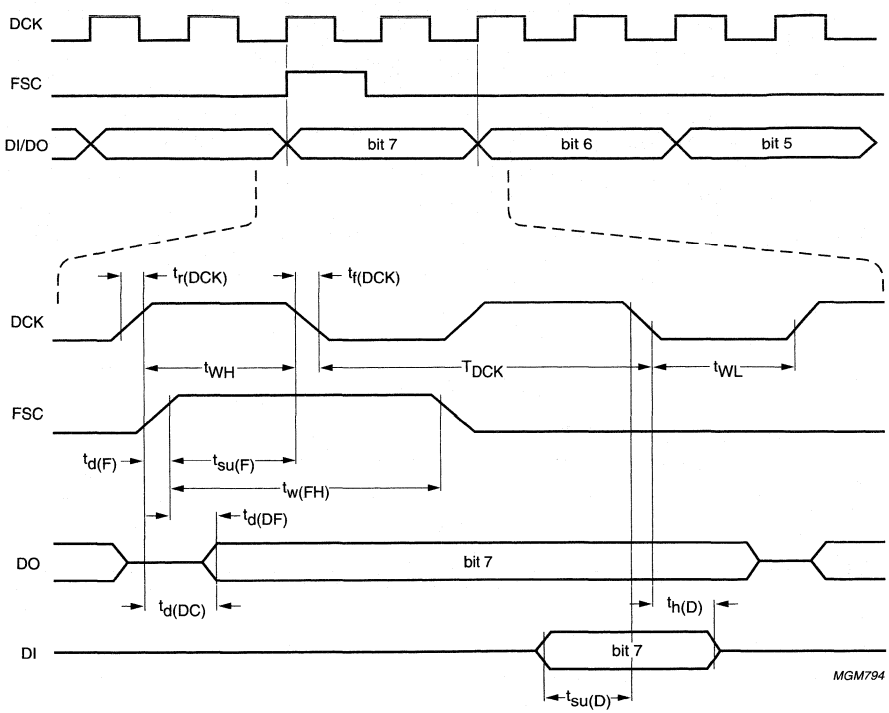


Fig.30 4-wire interface timing in IOM mode.

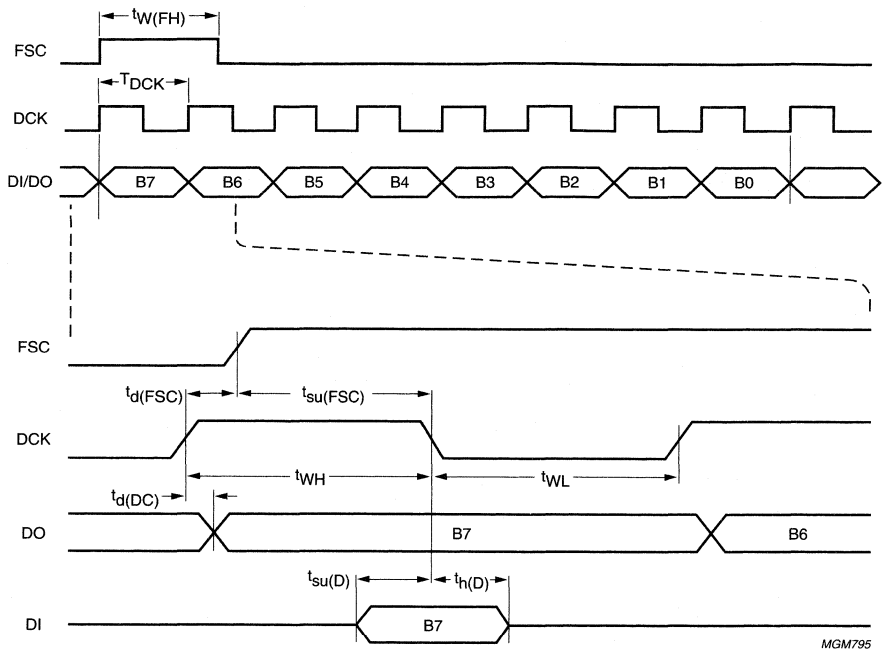


Fig.31 4-wire interface timing in speech mode.

16 EXTERNAL I/O INTERFACES

16.1 External analog interfaces

16.1.1 General purpose ADCs and DACs

For general use such as battery management, parallel set detection or speaker amplifier volume control, a 2-line multiplexed 8-bit ADC and an 8-bit DAC are on board of the chip. The ADC and DAC consist of several analog sub blocks called AVS and AAD, which are controlled by the digital block DCA (see Fig.32). Block AVS generates voltages in a time multiplexed way, and as such is a DAC with the band gap voltage V_{BGP} as input voltage.

Block AAD contains a comparator that is part of the successive approximation ADC formed by a combination of AVS, AAD and DCA. The analog-to-digital conversion can be performed on two external input signals AD0IN and AD1IN.

The whole circuit is active as long as the chip is in system-on mode. Both the ADC and the DAC can be controlled by the microcontroller, using the special function register mapped DCA block, allowing the user a flexible interface to analog peripherals.

If the microcontroller writes to the GPADC or GPDAR registers there is a latency until these SFRs have been changed (see Section 10.7).

16.1.2 General purpose ADC

The ADC on the chip is a 2-line multiplexed 8-bit converter. The control of this converter is done via two bits in the microcontroller GPADC SFR. One bit selects the channel and the other bit is the converter request bit. The request bit is reset by hardware when the converter has finished it's conversion cycle. The ADC (AAD in Fig.32), is of the successive approximation type.

An internal register contains the value of the slider position and is changed after each comparison of V_{ADC} with one of the two possible analog-to-digital input signals (AD0IN and AD1IN).

After 8 comparisons the conversion is finished and the contents of the internal register is copied into register GPADR. The conversion time will be less than 30 µs. This register can in turn be read by the internal microcontroller.

A valid conversion can only be done if V_{ref} and the comparator have stabilized. This means that after reset, approximately 10 to 20 ms should be waited and 100 analog-to-digital conversions should be done before the value of the conversion is used.

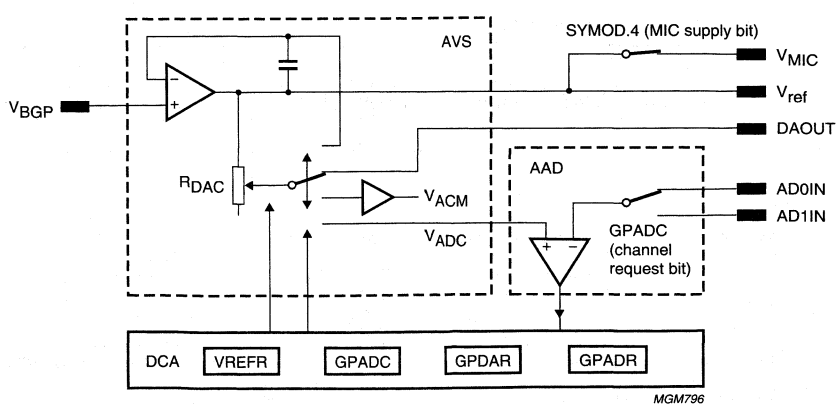


Fig.32 The architecture of the auxiliary DAC and ADC.

Table 60 GPADC (C3H) bit assignment; reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
spare	spare	spare	spare	spare	automatic analog-to-digital conversion[1]	channel select[2]	request confirm[3]

Notes

1. Automatic analog-to-digital conversion is performed every 30 ms if this bit is logic 1, regardless the state of the request confirm bit.
2. Channel select = 0: analog-to-digital conversion input is on pin AD0IN. Channel select = 1: analog-to-digital conversion input is on pin AD1IN.
3. The request bit should not be set in the same instruction which changes the channel.

The 8-bit result value from the conversion is presented in the GPADR register. The conversion range is 0 to 2000 mV (V_{ref}) with 8 mV resolution.

Table 61 GPADR (C2H) bit assignment; reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
result A/D7	result A/D6	result A/D5	result A/D4	result A/D3	result A/D2	result A/D1	result A/D0

16.1.3 General purpose DAC

The DAC on the chip is a single channel 8-bit converter. The control of this converter is done via the GPDAR register. It should be noted that for both writing GPDAR and reading GPADR a latency has to be added until these SFRs are being changed, see Section 10.7.

The value written in this register triggers the conversion which will be present at the output pin after the digital-to-analog conversion cycle (<10 µs). The range from the DAC output is 0 to 2000 mV (V_{ref}).

The conversion principle for both analog-to-digital and digital-to-analog conversion is shown in Fig.33.

Table 62 GPDAR (C4H) bit assignment; reset state 80H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
output D/A7	output D/A6	output D/A5	output D/A4	output D/A3	output D/A2	output D/A1	output D/A0

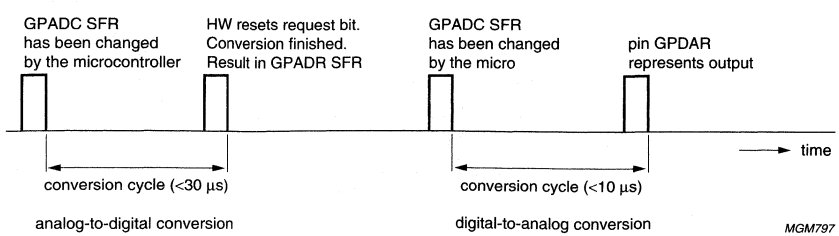


Fig.33 Analog-to-digital and digital-to-analog conversion principle.

16.2 External digital interfaces

For control of peripherals such as a display, ringer, key pad and line interface a large number of general purpose digital I/O pins are available in addition to the flash memory, LCD control pins and MSK or IOM modem pins. The exact number of free I/O pins depends on the choice of peripherals that make up the system configuration.
In the event that all alternate port functions of P1 and P3 are used, 10 input lines remain available on P1 and P3 of which 7 are programmable for interrupts. I/O ports P1 and P3 are 'weak pull-up' types which can therefore be used either as inputs or outputs. The reset value of P1 and P3 is FFH (input mode). In output mode for driving with a logic 1 (weak pull-up) the external load of P1 and P3 should be equivalent to >100 kΩ, for driving with a logic 0 the sink current should not exceed 4 mA. In addition to P1 and P3 there are 16 output ports available at P2 and MA. Output ports P2 and MA are push-pull ports and their reset value is 00H (output 00H). The driving level of P2 and MA is 4 mA for either logic 0 or 1. Port P4 provides the flash memory and display control signals. The P1, P3, and P4 I/O lines are available as SFR bit-addressable I/O registers in the configuration shown in Fig.34, while P2 and MA are (not bit-addressable) XDATA mapped ports when $\overline{EA}$ = 1.

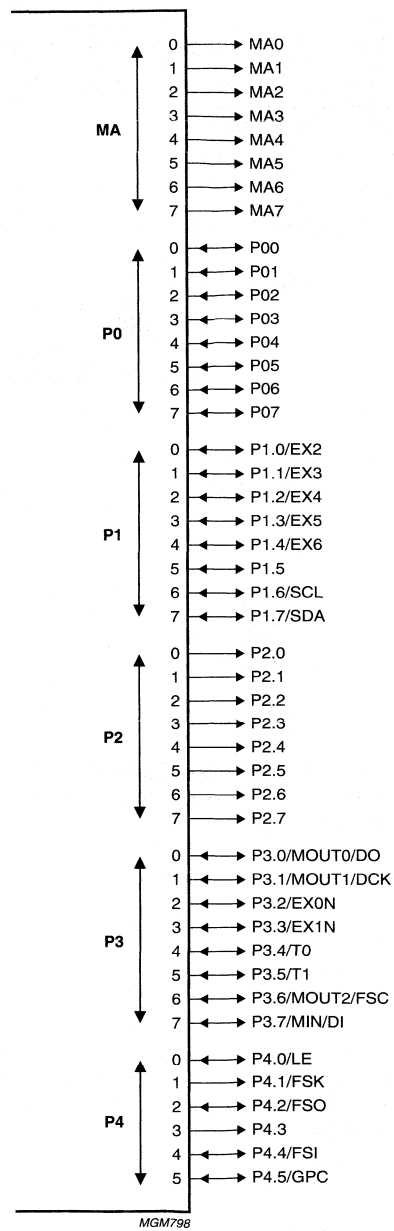


Fig.34 DTAM general purpose digital I/O configuration.

The MA and P2 ports are described in Chapter 12. The configuration of ports P1, P3 and P4 are described in the following tables.

Table 63 P1 (90H) bit assignment; bit-addressable and reset state FFH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P1.7/SDA[1]	P1.6/SCL[1]	P1.5	P1.4/EX6	P1.3/EX5	P1.2/EX4	P1.1/EX3	P1.0/EX2

Note

1. The alternative outputs (SDA and SCL) are connected with the general purpose outputs via an AND gate. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 64 P1 pin configuration

PORT PINS	CONFIGURATION
P1.7 and P1.6	open-drain
P1.5 to P1.0	quasi-bidirectional

For control of I²C-bus peripherals such as for instance EEPROMs and LCD displays, P1.6 and P1.7 can also be used as SDA and SCL to support I²C-bus. Section 10.13 describes how to activate this alternative function of P1.6 and P1.7. The rest of Port 1 is defined as general purpose I/O pins such as the standard 80C51 microcontroller.

Table 65 P3 (B0H) bit assignment, bit-addressable and reset state FFH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P3.7/ MIN/ DI	P3.6/ MOUT2/ FSC[1]	P3.5/ T1	P3.4/ T0	P3.3/ EX1N	P3.2/ EX0N	P3.1/ MOUT1/ DCK[1]	P3.0/ MOUT0/ DO[1]

Note

1. The alternative outputs (MOUT2, MOUT1, MOUT0, FSC, DCK and DO) are connected with the general purpose outputs via an AND gate. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 66 P3 pin configuration

PORT PINS	CONFIGURATION
P3.7, P3.6, P3.1 and P3.0	see Table 67
P3.5 to P3.2	quasi-bidirectional

Port 3 is defined as a set of 8 general purpose I/O pins such as the standard 80C51 microcontroller except for P3.6 and P3.7 which do not have the $\overline{RD}$ and $\overline{WR}$ function (the $\overline{RD}$ and $\overline{WR}$ are separate pins). Table 67 gives the different functions and the corresponding port configurations available on P3.7, P3.6, P3.1 and P3.0. The last column gives the function and configuration after reset.

Table 67 Ports 3.7, 3.6, 3.1 and 3.0 modes and configuration

MSK		IOM			GENERAL PURPOSE I/O PORT (RESET STATE)	
PIN FUNCTION	CONFIGURED	PIN FUNCTION	CONFIGURED AS MASTER	CONFIGURED AS SLAVE		
MOUT0	push-pull	DO	open-drain 4 mA	open-drain 4 mA	P3.0	quasi-bidirectional weak pull-up
MOUT1	push-pull	DCK	push-pull	input	P3.1	
MOUT2	push-pull	FSC	push-pull	input	P3.6	
MIN	input	DI	input	input	P3.7	

Table 68 shows how the pin configuration required for the MSK, IOM master/slave and general purpose function can be selected with the alternative port function register bits ALTP.6 and ALTP.5.

Table 68 Ports 3.7, 3.6, 3.1 and 3.0 selection of pin configurations for alternative function

ALTP.6	ALTP.5	MODE
0	0	general purpose I/O port
0	1	MSK
1	0	IOM slave
1	1	IOM master

Table 69 P4 (98H) bit assignment, bit-addressable and reset state 1EH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	P4.5/GPC[1]	P4.4/FSI	P4.3	P4.2/FSO[1]	P4.1/FSK[1]	P4.0/LE[1]

Note

1. The alternative outputs (GPC, FSO, FSK and LE) are connected with the general purpose outputs via an AND gate. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 70 P4 pin configuration

PORT PINS	CONFIGURATION
P4.5	open-drain (if ALTP.4 = 0) or push-pull (if ALTP.4 = 1)
P4.4, P4.2 and P4.0	open-drain
P4.3	open-drain, write only, 5 V tolerant
P4.1	open-drain, write only, double drive (8 mA)

The ALTP special function register is defined in Table 71.

Table 71 ALTP (ABH) bit assignment; reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	IOM on P3	IOM master/ MSK	P4.5 PP/OD	GPC on/ off(1)	GPC source(1)	LE on/off(2)	Early LE(2)

Notes

1. The general purpose clock function is described in more detail at the end of Section 9.1.
2. The LE function is described in more detail in Section 10.16.

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+3.6	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

18 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD3V}	digital supply voltage to pins V_{DD3V1}, V_{DD3V2} and V_{DD3V3}		2.7	3.0	3.3	V
V_{DDA}	analog supply voltage to pin V_{DDA}		2.7	3.0	3.3	V
V_{DDPLL}	analog supply voltage to pin V_{DDPLL}		2.7	3.0	3.3	V
V_{PP}	programming voltage		12.5	–	13.0	V
$I_{DD(max)}$	total input current	when recording a message from PSTN, CAS, line echo cancellation, listen-in on CODEC2; PLL on; CODEC1 and CODEC2 active; DSP at 28 MHz; microcontroller at 21 MHz; no load	–	40.0	50.0	mA
I_{DD3V1}	digital supply current at pin V_{DD3V1}		–	30	–	mA
I_{DD3V2}	digital supply current at pin V_{DD3V2}		–	2	–	mA
I_{DD3V3}	digital supply current at pin V_{DD3V3}		–	2	–	mA
I_{DDA}	analog supply current at pin V_{DDA}		–	4	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDPLL}	analog supply current at pin V_{DDPLL}		–	2	–	mA
$I_{DD(POTS)}$	Plain Old Telephone Service (POTS) mode supply current to all supply pins	PLL off; DSP off; CODECs off; microcontroller in Power-down; XTAL runs at 3.580 MHz; DTMF on; no load	–	1.6	2.0	mA
$I_{DD(sys-off)}$	total input current in system-off mode		–	0.45	0.70	mA
POR (Power-On Reset)						
$V_{th(H)}$	POR threshold voltage value HIGH	note 1	1.80	2.00	2.20	V
$V_{th(L)}$	POR threshold voltage value LOW	note 1	1.65	1.85	–	V
V_{hys}	POR hysteresis voltage	note 1	0.08	0.15	–	V
Crystal oscillator						
$C_{o(xtal1,2)}$	crystal output capacitance at pins XTAL1 and XTAL2 to V_{SS}	3.580 MHz	–	39	–	pF
		13.824 MHz	–	18	–	pF
Digital I/O						
V_{IL}	LOW-level input voltage					
	SDA and SCL		0	–	$0.3V_{DD}$	V
	other pins		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage					
	SDA and SCL		$0.7V_{DD}$	–	V_{DD}	V
	other pins		$0.8V_{DD}$	–	V_{DD}	V
$\|I_{OL}\|$	LOW-level output current	note 2				
	$\overline{RD}$, $\overline{WR}$, $\overline{PSE}$, P0, P1, P2, P3, P4.0, P4.2, P4.3, P4.4, P4.5 and MA		4	–	–	mA
	P4.1		8	–	–	mA
I_{OH}	HIGH-level output current	note 2				
	$\overline{PSE}$, P0, P2 and MA		4	–	–	mA
	P1.0, P1.1, P1.2, P1.3, P1.4, P1.5, P3 and P4.5		50[3][4]	–	250	µA
Analog levels; pins V_{BGP}, V_{ref} and V_{MIC}						
V_{BGP}	AVR band gap voltage	note 5	1.10	1.20	1.30	V
$V_{ref(TUNED)}$	reference voltage, tuned via VREFR	notes 6 and 7	1975	2000	2025	mV
$V_{ref(RESET)}$	reference voltage, after reset		1900	2030	2200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC; pin DAOUT						
R_o	output resistance	note 8	–	30	–	kΩ
V_o	output voltage		8	–	V_{ref}	mV
ADC; pins AD0IN and AD1IN						
V_i	input voltage		0	–	V_{ref}	mV
V_{IO}	input offset voltage		–50	–	+50	mV
R_i	input resistance	note 8	–	200	–	kΩ
DTMF						
$V_{DTMF(LG)}$	Low group DTMF level on pin LIFPOUT	RMS values	128	142	180	mV
$V_{DTMF(HG)}$	High group DTMF level on pin LIFPOUT	RMS values	161	181	225	mV
CODECS; note 9						
V_{MIC}	microphone input level	notes 10 and 11	–	–	–22	dBm
$R_{MIC(DM)}$	microphone input resistance; differential mode	note 12	–	200	–	kΩ
$R_{MIC(CM)}$	microphone input resistance; common mode	notes 12 and 13	–	500	–	kΩ
$V_{LIFIN(dif)}$	differential input level between LIFPIN and LIFMIN1 or LIFMIN2	notes 10 and 14	–	–	–6	dBm
$V_{LIFIN(s-e)}$	single-ended input level at LIFMIN1 or LIFMIN2 with LIFPIN to AC ground	notes 10 and 15	–	–	–12	dBm
$R_{LIFIN(DM)}$	LIFPIN to LIFMIN1 or LIFMIN2 input resistance; differential mode	notes 13 and 16	–	30	–	kΩ
$R_{LIFIN(CM)}$	LIFPIN, LIFMIN1 and LIFMIN2 input resistance; common mode	notes 13 and 16	–	15	–	kΩ
$\Delta G_{MIC(A/D)}$	delta analog-to-digital path gain of CODEC2 from MIC to PCM	notes 10 and 17	–1	0	+1	dB
$\Delta G_{LIF(A/D)}$	delta analog-to-digital path gain of CODEC1 from LIF to PCM	notes 10 and 18	–1	0	+1	dB
$\Delta G_{(D/A)}$	delta digital-to-analog path gain from PCM to SPKR or LIFOUT	notes 10 and 19	–1	0	+1	dB
$F_{(A/D)(idle)}$	analog-to-digital idle channel noise	notes 10 and 21	–	–87	–75	dBm0p
$(THD + N)/S_{(A/D)(-25)}$	analog-to-digital total harmonic distortion-plus-noise to signal ratio for CODEC2	notes 10 and 22	–	63	–	dBp
$(THD + N)/S_{(A/D)(-65)}$		notes 10 and 23	30	45	–	dBp
$(THD + N)/S_{(A/D)(-9)}$	analog-to-digital total harmonic distortion-plus-noise to signal ratio for CODEC1	notes 10 and 24	–	72	–	dBp
$(THD + N)/S_{(A/D)(-49)}$		notes 10 and 25	30	44	–	dBp
$t_{d(g)(A/D)}$	analog-to-digital path group delay		–	500	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{LIFOUT(dif)}$	line interface differential output level	note 26	–	1350	–	mV
R_{LIFOUT}	line interface output resistance	note 13	–	15	–	Ω
$V_{SPKR(dif)}$	speaker output, differential level	note 27	–	1350	–	mV
R_{SPKR}	speaker output resistance	note 13	–	15	–	Ω
$F_{(D/A)(idle)}$	digital-to-analog idle channel noise	notes 10 and 28	–	–88	–75	dBmp
(THD + N)/$S_{(D/A)(0)}$	digital-to-analog total harmonic distortion-plus-noise to signal ratio	notes 10 and 29	–	78	–	dBp
(THD + N)/$S_{(D/A)(-40)}$		notes 10 and 30	30	48	–	dBp
$t_{d(g)(D/A)}$	digital-to-analog path group delay		–	500	–	µs

Notes

1. The POR responds to $V_{DDA} - V_{SSA}$.
2. $V_{OUT} - V_{SS}$ = 400 mV (for $|I_{OL}|$), $V_{DD} - V_{OUT}$ = 400 mV (for I_{OH}).
3. On a LOW-to-HIGH transition, the output current value will be 4 mA for one microcontroller clock period, before changing to the specified lower value.
4. If the MSK mode is activated, the output current value for P3.0, P3.1 and P3.6 will be continuously 4 mA. If the IOM master mode is activated, the output current value for P3.1 and P3.6 will be continuously 4 mA.
5. V_{BGP} output current is zero. Decoupling capacitance between V_{BGP} and V_{SSA} is 100 nF. Value at 25 °C. The band gap has a temperature coefficient between –0.2 and +0.2 mV/°C.
6. V_{ref} output current is zero. Decoupling capacitance between V_{ref} and V_{SSA} is between 1 µF and 100 µF, with a 100 nF capacitance in parallel. The voltage is programmed by settings in register VREFR. The output can only source current (i.e. not sink).
7. Pin V_{MIC} is internally connected to V_{ref} via a switch. The V_{MIC} switch is closed by setting SYMOD.4 = 1. The V_{MIC} DC output current is maximum 400 µA, and V_{ref} must be programmed to its typical value. For the connections of V_{MIC} to a microphone see Fig.35. V_{MIC} adjustment can only be done by adjusting V_{ref}.
8. All input resistances represent the theoretical minimum, all output resistances represent the theoretical maximum which can be guaranteed by design.
9. V_{ref} is tuned to 2.0 V; typical values for the analog-to-digital and digital-to-analog filter characteristics conform to the G.712 specification; unless otherwise specified.
10. For the definition of the amplitude units (dB, dBm, dBm0, dBmp and dBm0p) see Section 13.1.
11. Sine wave RMS level applied differentially between pins MICP and MICM. The analog-to-digital path gain in control register CDVC2 = 00H is set to 22 dB (minimal gain for CODEC2). For larger input levels the output signal will saturate.
12. The differential resistance is seen between pins MICP and MICM. The common mode resistance is seen between pins MICP and V_{SSA} or pins MICM and V_{SSA}.
13. All input resistances represent the theoretical minimum, all output resistances represent the theoretical maximum which can be guaranteed by design.
14. Sine wave RMS level applied differentially between pins LIFP and LIFM. The analog-to-digital path gain in control register CDVC1 = 00H is set to 9 dB (minimum gain for CODEC1, including digital gain). For larger input levels the output signal will saturate.
15. Sine wave RMS level applied between V_{SSA} and LIFMIN1 or LIFMIN2. LIFPIN is connected to V_{SSA} via a capacitor (see Fig.35). The analog-to-digital path gain in control register CDVC1 is set to 9 dB. For larger input levels the output signal will saturate.

16. The differential resistance is seen between pins LIFP and LIFMIN1 or LIFM. The common mode resistance is seen between LIFP and V_{SSA} or LIFM and V_{SSA}.
17. The deviation of the absolute gain as specified in CDVC2, measured at 1020 Hz.
18. The deviation of the absolute gain as specified in CDVC1, measured at 1020 Hz.
19. The deviation of the absolute gain as specified in CDVC1/CDVC2, measured at 1020 Hz.
20. The difference between two adjacent gain settings as specified in CDVC1/CDVC2. Valid for both analog-to-digital and digital-to-analog path.
21. The analog-to-digital path gain for CODEC1 is set to 9 dB and for CODEC2 is set to 25 dB (CDCV1/2 = 00H). LIFPIN and LIFMIN1 or LIFMIN2 are shorted together for CODEC1. MICP and MICM are shorted together for CODEC2. The measured value is psophometrically weighted.
22. The analog-to-digital path gain in control register CDVC2 = 00H is set to 25 dB for CODEC2, when a sine wave of 1020 Hz with a level of –24 dBm is applied between MICP and MICM. The value includes harmonic distortion and is psophometrically weighted.
23. The analog-to-digital path gain in control register CDVC2 = 00H is set to 25 dB for CODEC2, when a sine wave of 1020 Hz with a level of –65 dBm is applied between MICP and MICM. The value includes harmonic distortion and is psophometrically weighted.
24. The analog-to-digital path gain in control register CDVC1 = 00H is set to 9 dB for CODEC1, when a sine wave of 1020 Hz with a level of –9 dBm is applied between LIFPIN and LIFMIN1 or LIFMIN2. The value includes harmonic distortion and is psophometrically weighted.
25. The analog-to-digital path gain in control register CDVC1 = 00H is set to 9 dB for CODEC1, when a sine wave of 1020 Hz with a level of –49 dBm is applied between LIFPIN and LIFMIN1 or LIFMIN2. The value includes harmonic distortion and is psophometrically weighted.
26. Sine wave RMS level applied differentially between pins LIFPIN and LIFMIN1 or LIFMIN2. The analog-to-digital path gain is set to 9 dB and the digital-to-analog path gain is set to 2 dB (CDVC1 = F0H). The input signal is 970 Hz with a level of 3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω.
27. Sine wave RMS level applied differentially between pins SPKRP and SPKRM. The analog-to-digital path gain is set to 25 dB (CDVC1/2 = 00) and the digital-to-analog path gain is set to 2 dB (CDVC2 = F0H). The input signal is 970 Hz with a level of 3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω.
28. The digital-to-analog path gain for CODEC1 and CODEC2 is set to 0 dB (CDVC1/2 = D0H). The DSP is in Idle mode. The value is differentially measured and psophometrically weighted.
29. The digital-to-analog path gain in control register CDVC1/2 = D0H is set to 0 dB for CODEC1 and CODEC2, when a bitstream representing a sine wave of 970 Hz with a level of 0 dBm0 is applied at the PCM interface (DSP output). The value includes harmonic distortion and is psophometrically weighted. The load between SPKRM and SPKRP or LIFMOUT and LIFPOUT is 100 pF in parallel to 150 Ω and 800 μH.
30. The digital-to-analog path gain in control register CDVC1/2 = D0H is set to 0 dB for CODEC1 and CODEC2, when a bitstream representing a sine wave of 970 Hz with a level of –40 dBm0 is applied at the PCM interface (DSP output). The value includes harmonic distortion and is psophometrically weighted. The load between SPKRM and SPKRP or LIFMOUT and LIFPOUT is 100 pF in parallel to 150 Ω and 800 μH.

18.1 Timing characteristics

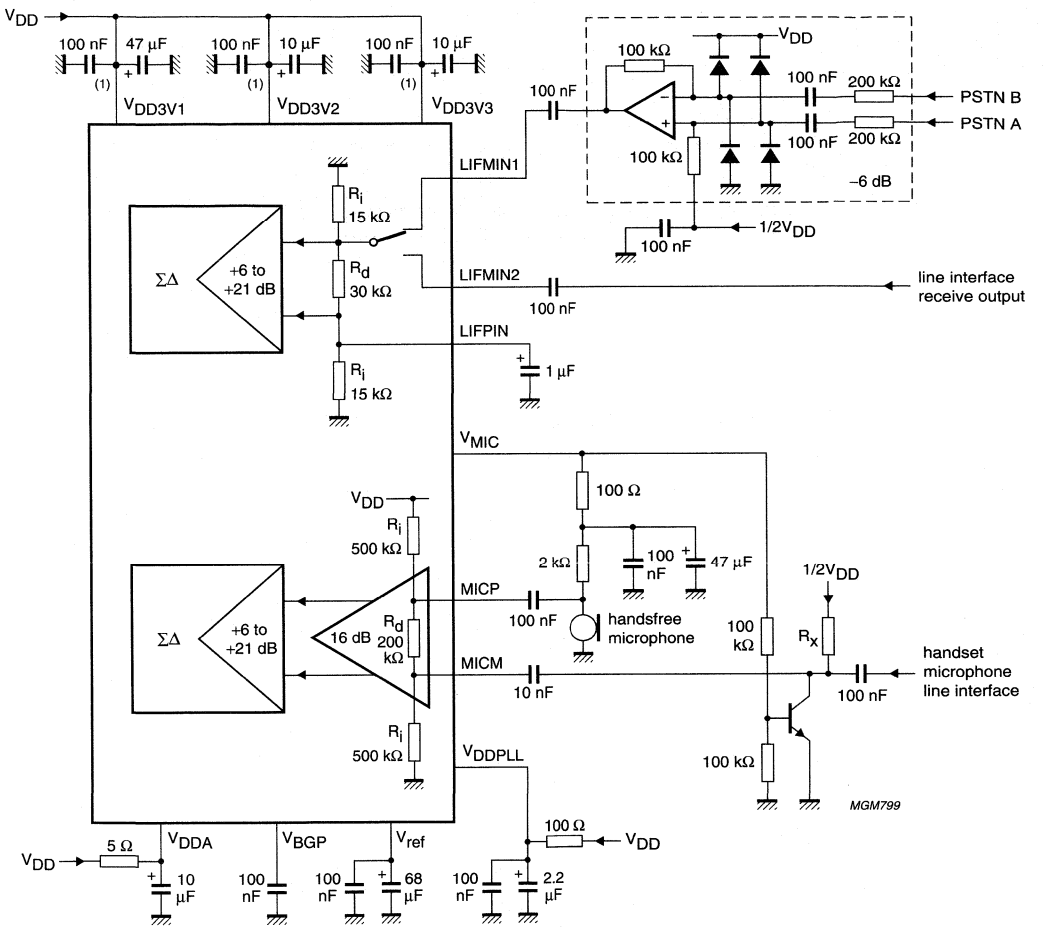
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCB timing; see Fig.12						
T_{FSK}	FSK period		–	$N \times t_{\mu C\_CLK}$[1]	–	s
$t_{su(FSO)}$	FSO setup time with respect to the rising edge of FSK		–	$(N/2 + 1) \times t_{\mu C\_CLK} - t_{r(FSO)}$	–	s
$t_{h(FSO)}$	FSO hold time with respect to the rising edge of FSK		–	$(N/2 - 1) \times t_{\mu C\_CLK} - t_{r(FSK)}$	–	s
$t_{r(FSK)}$	FSK rise time		–	note 2	–	s
$t_{r(FSO)}$	FSO rise time		–	note 2	–	s
$t_{su(FSI)}$	FSI setup time with respect to the internal shift clock		–	$(N/2 - 1) \times t_{\mu C\_CLK} - t_{V(FSI)}$	–	s
$t_{h(FSI)}$	FSI hold time with respect to the internal shift clock		–	$> t_{\mu C\_CLK}$	–	s
$t_{V(FSI)}$	FSI valid time with respect to the falling edge of FSK		–	depending on the used flash memory	–	s
IOM mode timing; see Fig.30						
$t_{r(DCK)}$	data clock (DCK) rise time		–	–	60	ns
$t_{f(DCK)}$	data clock (DCK) fall time		–	–	60	ns
T_{DCK}	data clock (DCK) cycle time		220[3]	–	–	ns
t_{WH}	data clock (DCK) pulse width HIGH		80	–	–	ns
t_{WL}	data clock (DCK) pulse width LOW		80	–	–	ns
$t_{r(FSC)}$	frame sync (FSC) rise time		–	–	60	ns
$t_{f(FSC)}$	frame sync (FSC) fall time		–	–	60	ns
$t_{d(F)}$	frame sync (FSC) delay time		$-t_{WL}$	–	+60	ns
$t_{su(F)}$	frame sync (FSC) set-up time		60	–	–	ns
$t_{W(FH)}$	frame sync (FSC) pulse width HIGH		130	–	–	ns
$t_{d(DC)}$	output data (DO) to data clock delay time	C_L = 150 pF	–	–	100	ns
$t_{d(DF)}$	output data (DO) to frame sync delay time	C_L = 150 pF	–	–	150	ns
$t_{su(D)}$	input data (DI) set-up time		t_{WH}	–	–	ns
$t_{h(D)}$	input data (DI) hold time		50	–	–	ns
Speech mode timing; see Fig.31						
$t_{d(FSC)}$	frame sync (FSC) delay time		$-t_{WL}$	–	+100	ns
$t_{su(FSC)}$	frame sync (FSC) set-up time		60	–	–	ns
$t_{W(FH)}$	frame sync (FSC) high time pulse width		130	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{DCK}	data clock (DCK) cycle time		440[4]	–	–	ns
t_{WH}	data clock (DCK) pulse width HIGH		150	–	–	ns
t_{WL}	data clock (DCK) pulse width LOW		150	–	–	ns
$t_{d(DC)}$	output data (DO) to data clock delay time	C_L = 150 pF	–	–	100	ns
$t_{su(D)}$	input data (DI) set-up time		60	–	–	ns
$t_{h(D)}$	input data (DI) hold time		60	–	–	ns

Notes

1. N depends on the chosen FSK clock rate and can be 4, 8, 16 or 32.
2. The rise time of FSK and FSO depends on the externally connected pull-up resistor and the capacitive load.
3. Corresponds to the highest DCK frequency allowed (4.096 MHz) with a 10% margin.
4. Corresponds to the DCK frequency (2.048 MHz) with a 10% margin.

19 APPLICATION INFORMATION



(1) The decoupling capacitors for V_{DD3V1}, V_{DD3V2} and V_{DD3V3} must be mounted as close as possible to the respective pins.

Fig.35 Supply connections and analog input connections for line interface, caller ID and handsfree.

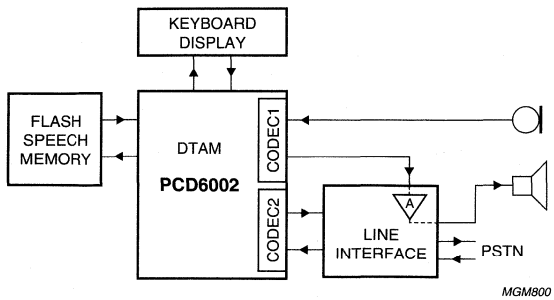


Fig.36 Stand alone digital answering machine with handsfree application example.

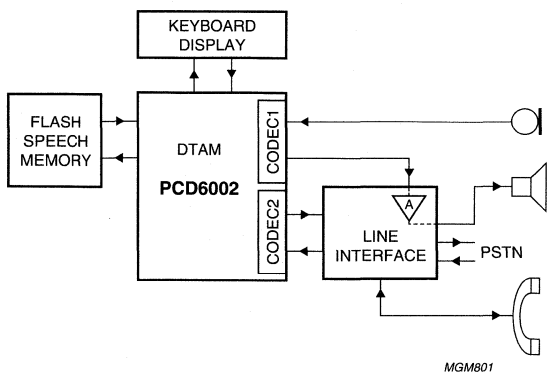


Fig.37 Digital telephone answering machine with handsfree application example.

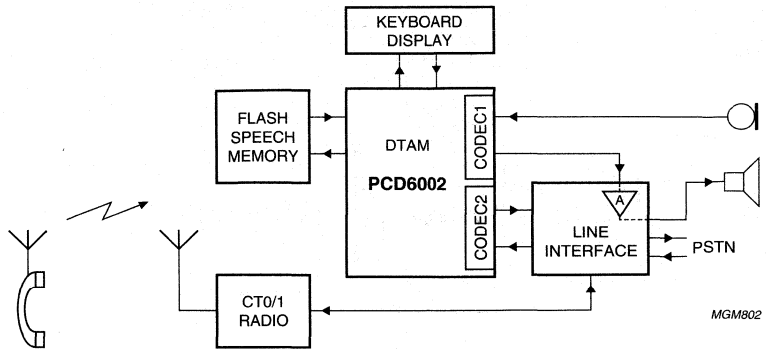


Fig.38 Analog cordless base station with digital handsfree answering machine application example.

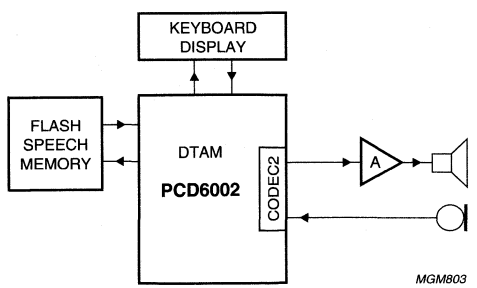


Fig.39 Portable voice memo recorder application example.

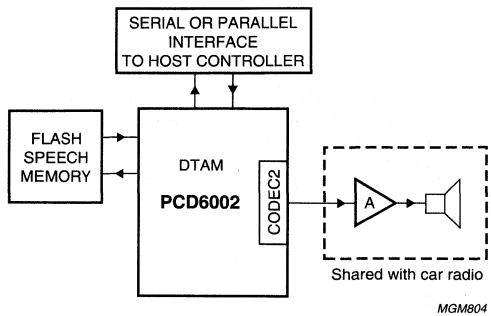


Fig.40 Automotive application example (audible car status information is presented to the driver).

CONTENTS

48 × 84 pixels matrix LCD controller/driver PCD8544

1 FEATURES

- Single chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48 × 84 bits
- On-chip:
  - Generation of LCD supply voltage (external supply also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External $\overline{RES}$ (reset) input pin
- Serial interface maximum 4.0 Mbits/s
- CMOS compatible inputs
- Mux rate: 48
- Logic supply voltage range V_{DD} to V_{SS}: 2.7 to 3.3 V
- Display supply voltage range V_{LCD} to V_{SS}
  - 6.0 to 8.5 V with LCD voltage internally generated (voltage generator enabled)
  - 6.0 to 9.0 V with LCD voltage externally supplied (voltage generator switched-off).
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Temperature range: –25 to +70 °C.

2 GENERAL DESCRIPTION

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.

The PCD8544 interfaces to microcontrollers through a serial bus interface.

The PCD8544 is manufactured in n-well CMOS technology.

3 APPLICATIONS

- Telecommunications equipment.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD8544U	–	chip with bumps in tray; 168 bonding pads + 4 dummy pads	–

5 BLOCK DIAGRAM

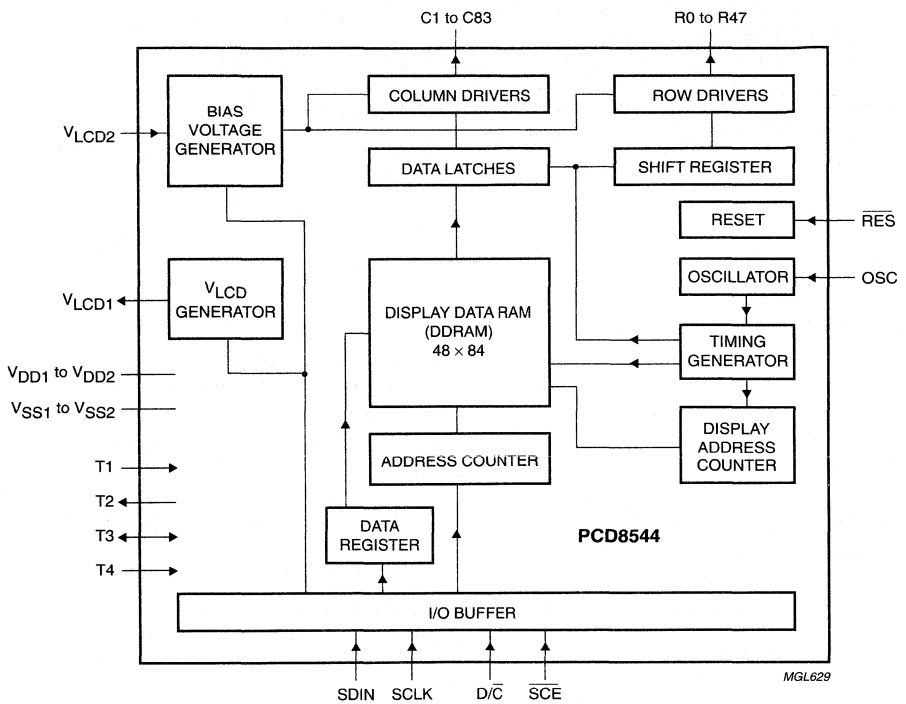


Fig.1 Block diagram.

6 PINNING

SYMBOL	DESCRIPTION
R0 to R47	LCD row driver outputs
C0 to C83	LCD column driver outputs
V_{SS1}, V_{SS2}	ground
V_{DD1}, V_{DD2}	supply voltage
V_{LCD1}, V_{LCD2}	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 input/output
T4	test 4 input
SDIN	serial data input
SCLK	serial clock input
D/$\overline{C}$	data/$\overline{\text{command}}$
$\overline{SCE}$	chip enable
OSC	oscillator
$\overline{RES}$	external reset input
dummy1, 2, 3, 4	not connected

Note

1. For further details, see Fig.18 and Table 7.

6.1 Pin functions

6.1.1 R0 TO R47 ROW DRIVER OUTPUTS

These pads output the row signals.

6.1.2 C0 TO C83 COLUMN DRIVER OUTPUTS

These pads output the column signals.

6.1.3 V_{SS1}, V_{SS2}: NEGATIVE POWER SUPPLY RAILS

Supply rails V_{SS1} and V_{SS2} must be connected together.

6.1.4 V_{DD1}, V_{DD2}: POSITIVE POWER SUPPLY RAILS

Supply rails V_{DD1} and V_{DD2} must be connected together.

6.1.5 V_{LCD1}, V_{LCD2}: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. Supply rails V_{LCD1} and V_{LCD2} must be connected together.

6.1.6 T1, T2, T3 AND T4: TEST PADS

T1, T3 and T4 must be connected to V_{SS}, T2 is to be left open. Not accessible to user.

6.1.7 SDIN: SERIAL DATA LINE

Input for the data line.

6.1.8 SCLK: SERIAL CLOCK LINE

Input for the clock signal: 0.0 to 4.0 Mbits/s.

6.1.9 D/$\overline{C}$: MODE SELECT

Input to select either command/address or data input.

6.1.10 $\overline{SCE}$: CHIP ENABLE

The enable pin allows data to be clocked in. The signal is active LOW.

6.1.11 OSC: OSCILLATOR

When the on-chip oscillator is used, this input must be connected to V_{DD}. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to V_{SS}, the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.

6.1.12 $\overline{RES}$: RESET

This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD}. An external clock signal, if used, is connected to this input.

7.2 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X-address X_6 to X_0 and the Y-address Y_2 to Y_0 are set separately. After a write operation, the address counter is automatically incremented by 1, according to the V flag.

7.3 Display Data RAM (DDRAM)

The DDRAM is a 48 × 84 bit static RAM which stores the display data. The RAM is divided into six banks of 84 bytes (6 × 8 × 84 bits). During RAM access, data is transferred to the RAM through the serial interface. There is a direct correspondence between the X-address and the column output number.

7.4 Timing generator

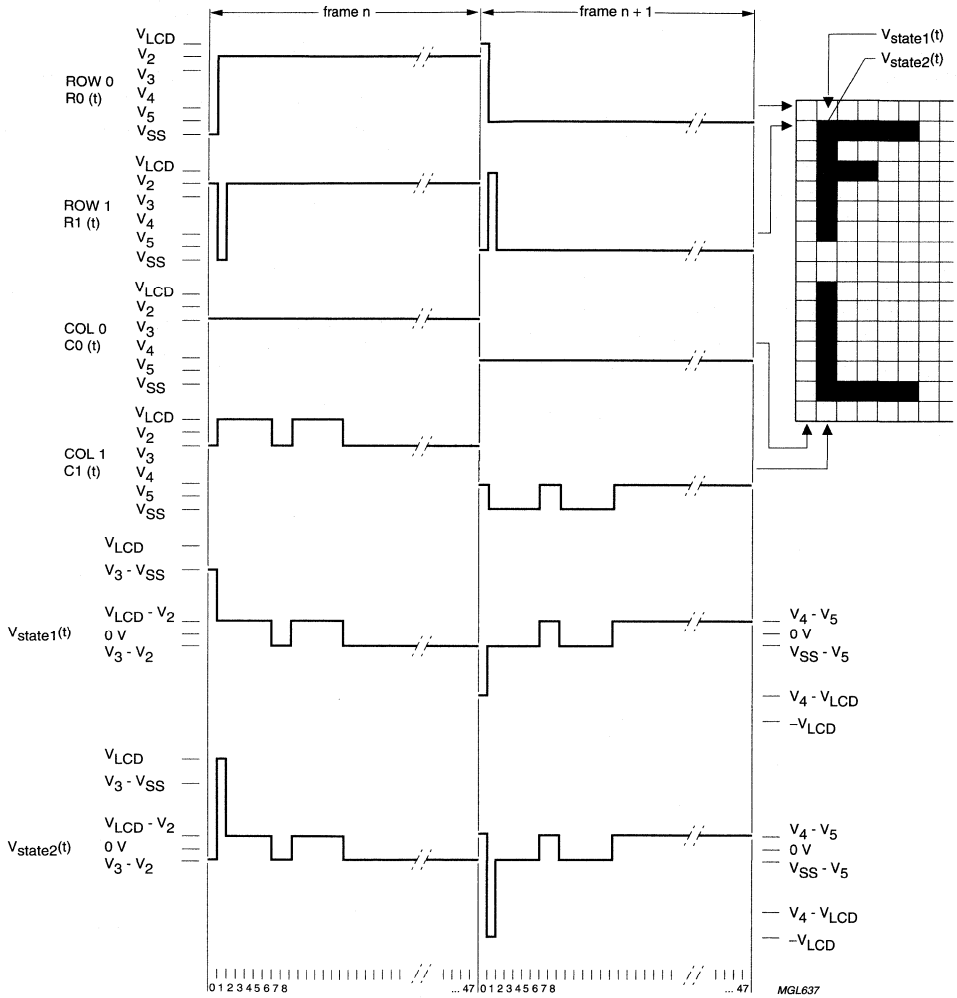
The timing generator produces the various signals required to drive the internal circuits. Internal chip operation is not affected by operations on the data buses.

7.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD through the column outputs. The display status (all dots on/off and normal/inverse video) is set by bits E and D in the 'display control' command.

7.6 LCD row and column drivers

The PCD8544 contains 48 row and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

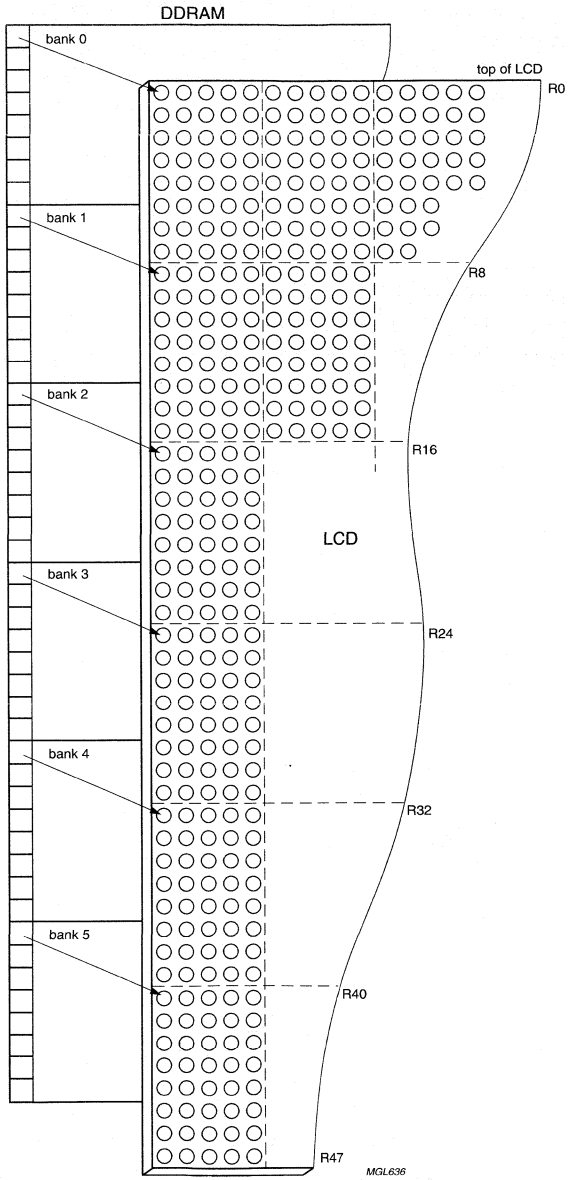


Fig.3 DDRAM to display mapping.

7.7 Addressing

Data is downloaded in bytes into the 48 by 84 bits RAM data display matrix of PCD8544, as indicated in Figs. 3, 4, 5 and 6. The columns are addressed by the address pointer. The address ranges are: X 0 to 83 (1010011), Y 0 to 5 (101). Addresses outside these ranges are not allowed. In the vertical addressing mode (V = 1), the Y address increments after each byte (see Fig.5). After the last Y address (Y = 5), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0), the X address increments after each byte (see Fig.6). After the last X address (X = 83), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 83 and Y = 5), the address pointers wrap around to address (X = 0 and Y = 0).

7.7.1 DATA STRUCTURE

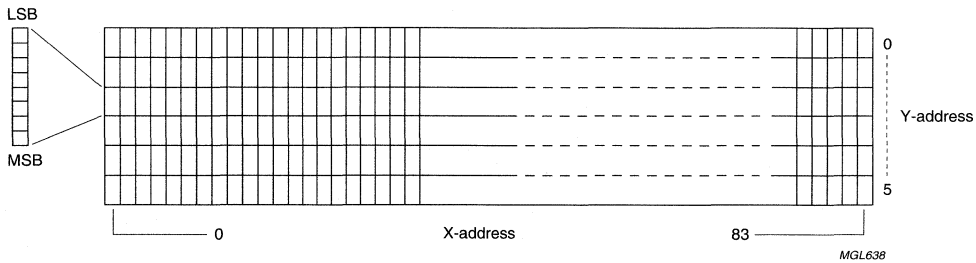


Fig.4 RAM format, addressing.

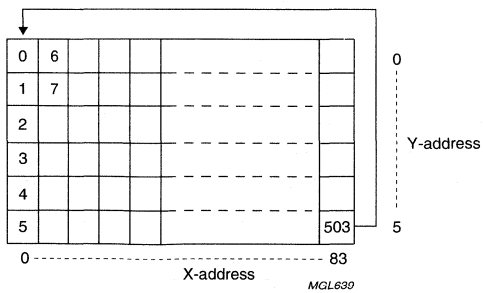


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

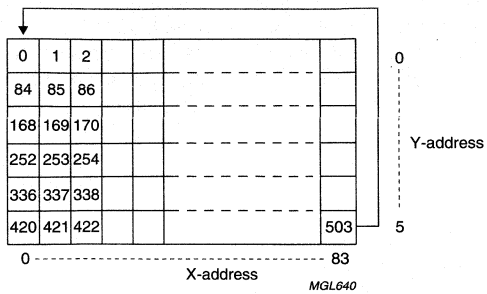
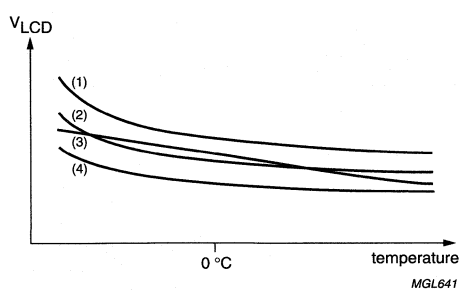


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

7.8 Temperature compensation

Due to the temperature dependency of the liquid crystals' viscosity, the LCD controlling voltage V_{LCD} must be increased at lower temperatures to maintain optimum contrast. Figure 7 shows V_{LCD} for high multiplex rates. In the PCD8544, the temperature coefficient of V_{LCD}, can be selected from four values (see Table 2) by setting bits TC_1 and TC_0.



(1) Upper limit.
(2) Typical curve.
(3) Temperature coefficient of IC.
(4) Lower limit.

Fig.7 V_{LCD} as function of liquid crystal temperature (typical values).

8 INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ (mode select) is set LOW, the current byte is interpreted as command byte (see Table 1). Figure 8 shows an example of a serial data stream for initializing the chip. If D/$\overline{C}$ is set HIGH, the following bytes are stored in the display data RAM. After every data byte, the address counter is incremented automatically.

The level of the D/$\overline{C}$ signal is read during the last bit of data byte.

Each instruction can be sent in any order to the PCD8544. The MSB of a byte is transmitted first. Figure 9 shows one possible command stream, used to set up the LCD driver.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

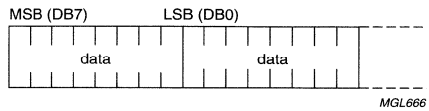


Fig.8 General format of data stream.

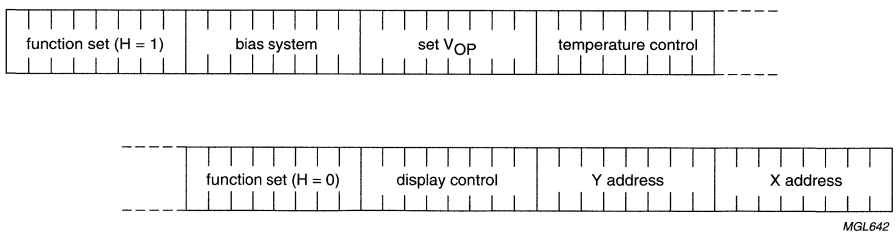


Fig.9 Serial data stream, example.

Figures 10 and 11 show the serial bus protocol.

- When $\overline{SCE}$ is HIGH, SCLK clock signals are ignored; during the HIGH time of $\overline{SCE}$, the serial interface is initialized (see Fig.12)
- SDIN is sampled at the positive edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1); it is read with the eighth SCLK pulse
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects bit 7 of the next byte at the next positive edge of SCLK (see Fig.12)
- A reset pulse with $\overline{RES}$ interrupts the transmission. No data is written into the RAM. The registers are cleared. If $\overline{SCE}$ is LOW after the positive edge of $\overline{RES}$, the serial interface is ready to receive bit 7 of a command/data byte (see Fig.13).

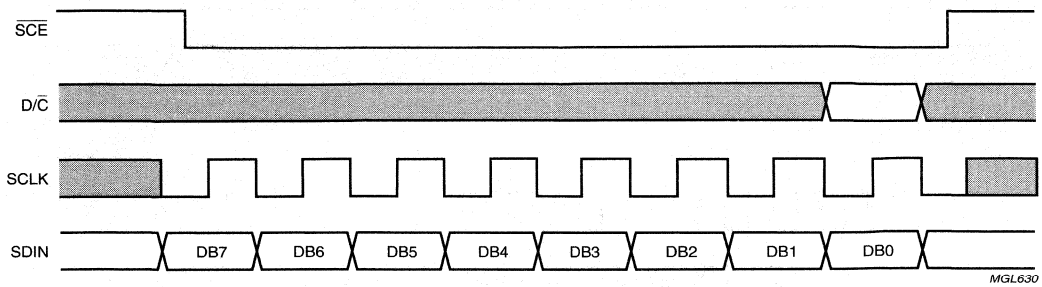


Fig.10 Serial bus protocol - transmission of one byte.

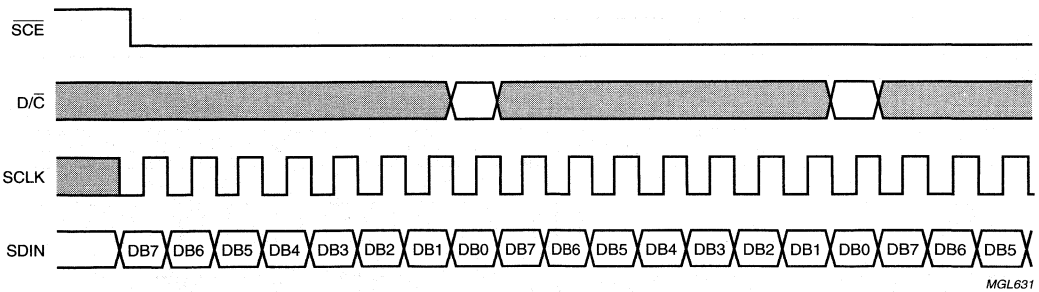


Fig.11 Serial bus protocol - transmission of several bytes.

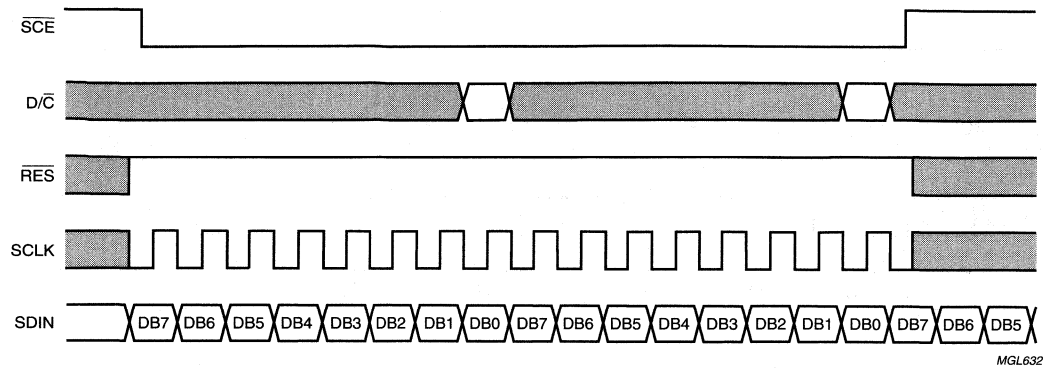


Fig.12 Serial bus reset function ($\overline{SCE}$).

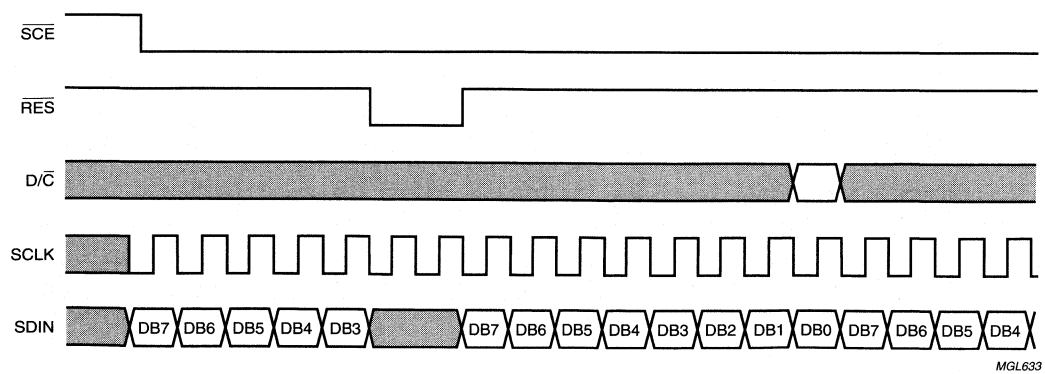


Fig.13 Serial bus reset function ($\overline{RES}$).

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
(H = 0 or 1)										
NOP	0	0	0	0	0	0	0	0	0	no operation
Function set	0	0	0	1	0	0	PD	V	H	power down control; entry mode; extended instruction set control (H)
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM
(H = 0)										
Reserved	0	0	0	0	0	0	1	X	X	do not use
Display control	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	1	0	0	0	Y_2	Y_1	Y_0	sets Y-address of RAM; $0 \leq Y \leq 5$
Set X address of RAM	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address part of RAM; $0 \leq X \leq 83$
(H = 1)										
Reserved	0	0	0	0	0	0	0	0	1	do not use
	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	1	TC_1	TC_0	set Temperature Coefficient (TC_x)
Reserved	0	0	0	0	0	1	X	X	X	do not use
Bias system	0	0	0	0	1	0	BS_2	BS_1	BS_0	set Bias System (BS_x)
Reserved	0	0	1	X	X	X	X	X	X	do not use
Set V_{OP}	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations of symbols in Table 1

BIT	0	1
PD	chip is active	chip is in Power-down mode
V	horizontal addressing	vertical addressing
H	use basic instruction set	use extended instruction set
D and E		
00	display blank	
10	normal mode	
01	all display segments on	
11	inverse video mode	
TC_1 and TC_0		
00	V_{LCD} temperature coefficient 0	
01	V_{LCD} temperature coefficient 1	
10	V_{LCD} temperature coefficient 2	
11	V_{LCD} temperature coefficient 3	

8.1 Initialization

Immediately following power-on, the contents of all internal registers and of the RAM are undefined. **A $\overline{RES}$ pulse must be applied**. Attention should be paid to the possibility that the **device may be damaged** if not properly reset.

All internal registers are reset by applying an external $\overline{RES}$ pulse (active LOW) at pad 31, within the specified time. However, the RAM contents are still undefined. The state after reset is described in Section 8.2.

The $\overline{RES}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher) within a maximum time of 100 ms after V_{DD} goes HIGH (see Fig.16).

8.2 Reset function

After reset, the LCD driver has the following state:

- Power-down mode (bit PD = 1)
- Horizontal addressing (bit V = 0) normal instruction set (bit H = 0)
- Display blank (bit E = D = 0)
- Address counter X_6 to X_0 = 0; Y_2 to Y_0 = 0
- Temperature control mode (TC_1 TC_0 = 0)
- Bias system (BS_2 to BS_0 = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{OP6} to V_{OP0} = 0)
- After power-on, the RAM contents are undefined.

8.3 Function set

8.3.1 Bit PD

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off, V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- Serial bus, command, etc. function
- Before entering Power-down mode, the RAM needs to be filled with '0's to ensure the specified current consumption.

8.3.2 Bit V

When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the DDRAM, as shown in Fig.5.

8.3.3 Bit H

When H = 0 the commands 'display control', 'set Y address' and 'set X address' can be performed; when H = 1, the others can be executed. The 'write data' and 'function set' commands can be executed in both cases.

8.4 Display control

8.4.1 Bits D and E

Bits D and E select the display mode (see Table 2).

8.5 Set Y address of RAM

Y_n defines the Y vector addressing of the display RAM.

Table 3 Y vector addressing

Y_2	Y_1	Y_0	BANK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

8.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 83 (53H).

8.7 Temperature control

The temperature coefficient of V_{LCD} is selected by bits TC_1 and TC_0.

8.8 Bias value

The bias voltage levels are set in the ratio of R - R - nR - R - R, giving a 1/(n + 4) bias system. Different multiplex rates require different factors n (see Table 4). This is programmed by BS_2 to BS_0. For Mux 1 : 48, the optimum bias value n, resulting in 1/8 bias, is given by:

$$n = \sqrt{48} - 3 = 3.928 = 4 \quad (1)$$

Table 4 Programming the required bias system

BS_2	BS_1	BS_0	n	RECOMMENDED MUX RATE
0	0	0	7	1 : 100
0	0	1	6	1 : 80
0	1	0	5	1 : 65/1 : 65
0	1	1	4	1 : 48
1	0	0	3	1 : 40/1 : 34
1	0	1	2	1 : 24
1	1	0	1	1 : 18/1 : 16
1	1	1	0	1 : 10/1 : 9/1 : 8

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGE FOR 1/8 BIAS
V1	V_{LCD}	V_{LCD}
V2	(n + 3)/(n + 4)	$^7/_8 \times V_{LCD}$
V3	(n + 2)/(n + 4)	$^6/_8 \times V_{LCD}$
V4	2/(n + 4)	$^2/_8 \times V_{LCD}$
V5	1/(n + 4)	$^1/_8 \times V_{LCD}$
V6	V_{SS}	V_{SS}

8.9 Set V_{OP} value

The operation voltage V_{LCD} can be set by software. The values are dependent on the liquid crystal selected. V_{LCD} = a + (V_{OP6} to V_{OP0}) × b [V]. In the PCD8544, a = 3.06 and b = 0.06 giving a program range of 3.00 to 10.68 at room temperature.

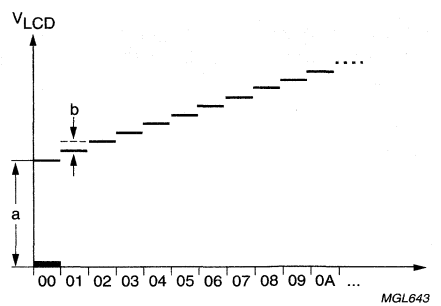
Note that the charge pump is turned off if V_{OP6} to V_{OP0} is set to zero.

For Mux 1 : 48, the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{48}}{\sqrt{2\cdot\left(1-\frac{1}{\sqrt{48}}\right)}} \cdot V_{th} = 6.06 \cdot V_{th} \qquad (2)$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Caution, as V_{OP} increases with lower temperatures, care must be taken not to set a V_{OP} that will exceed the maximum of 8.5 V when operating at −25 °C.



a = 3.06.
b = 0.06.
V_{OP6} to V_{OP0} (programmed) [00 to 7FH].

Fig.14 V_{OP} programming.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 3	−0.5	+7	V
V_{LCD}	supply voltage LCD	note 4	−0.5	+10	V
V_I	all input voltages		−0.5	V_{DD} + 0.5	V
I_{SS}	ground supply current		−50	+50	mA
I_I, I_O	DC input or output current		−10	+10	mA
P_{tot}	total power dissipation		−	300	mW
P_O	power dissipation per output		−	30	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_j	operating junction temperature		−65	+150	°C
T_{stg}	storage temperature		−65	+150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. With external LCD supply voltage externally supplied (voltage generator disabled). V_{DDmax} = 5 V if LCD supply voltage is internally generated (voltage generator enabled).
4. When setting V_{LCD} by software, take care not to set a V_{OP} that will exceed the maximum of 8.5 V when operating at −25 °C, see Caution in Section 8.9.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 DC CHARACTERISTICS

V_{DD} = 2.7 to 3.3 V; V_{SS} = 0 V; V_{LCD} = 6.0 to 9.0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1	LCD voltage externally supplied (voltage generator disabled)	2.7	–	3.3	V
V_{DD2}	supply voltage 2	LCD voltage internally generated (voltage generator enabled)	2.7	–	3.3	V
V_{LCD1}	LCD supply voltage	LCD voltage externally supplied (voltage generator disabled)	6.0	–	9.0	V
V_{LCD2}	LCD supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	6.0	–	8.5	V
I_{DD1}	supply current 1 (normal mode) for internal V_{LCD}	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; note 2	–	240	300	µA
I_{DD2}	supply current 2 (normal mode) for internal V_{LCD}	V_{DD} = 2.70 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; note 2	–	–	320	µA
I_{DD3}	supply current 3 (Power-down mode)	with internal or external LCD supply voltage; note 3	–	1.5	–	µA
I_{DD4}	supply current external V_{LCD}	V_{DD} = 2.85 V; V_{LCD} = 9.0 V; f_{SCLK} = 0; notes 2 and 4	–	25	–	µA
I_{LCD}	supply current external V_{LCD}	V_{DD} = 2.7 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T = 25 °C; display load = 10 µA; notes 2 and 4	–	42	–	µA
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
Column and row outputs						
$R_{o(C)}$	column output resistance C0 to C83		–	12	20	kΩ
$R_{o(R)}$	row output resistance R0 to R47		–	12	20	kΩ
$V_{bias(tol)}$	bias voltage tolerance on C0 to C83 and R0 to R47		−100	0	+100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LCD supply voltage generator						
V_{LCD}	V_{LCD} tolerance internally generated	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA; note 5	–	0	300	mV
TC0	V_{LCD} temperature coefficient 0	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	1	–	mV/K
TC1	V_{LCD} temperature coefficient 1	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	9	–	mV/K
TC2	V_{LCD} temperature coefficient 2	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	17	–	mV/K
TC3	V_{LCD} temperature coefficient 3	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	24	–	mV/K

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. RAM contents equal '0'. During power-down, all static currents are switched off.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
5. Tolerance depends on the temperature (typically zero at 27 °C, maximum tolerance values are measured at the temperate range limit).

12 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency		20	34	65	kHz
$f_{clk(ext)}$	external clock frequency		10	32	100	kHz
f_{frame}	frame frequency	f_{OSC} or $f_{clk(ext)}$ = 32 kHz; note 1	–	67	–	Hz
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW	Fig.16	0[2]	–	30	ms
$t_{WL(RES)}$	$\overline{RES}$ LOW pulse width	Fig.16	100	–	–	ns
Serial bus timing characteristics						
f_{SCLK}	clock frequency	V_{DD} = 3.0 V ±10%	0	–	4.00	MHz
T_{cy}	clock cycle SCLK	All signal timing is based on 20% to 80% of V_{DD} and maximum rise and fall times of 10 ns	250	–	–	ns
t_{WH1}	SCLK pulse width HIGH		100	–	–	ns
t_{WL1}	SCLK pulse width LOW		100	–	–	ns
t_{su2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{h2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{WH2}	$\overline{SCE}$ min. HIGH time		100	–	–	ns
t_{h5}	$\overline{SCE}$ start hold time; note 3		100	–	–	ns
t_{su3}	D/$\overline{C}$ set-up time		100	–	–	ns
t_{h3}	D/$\overline{C}$ hold time		100	–	–	ns
t_{su4}	SDIN set-up time		100	–	–	ns
t_{h4}	SDIN hold time		100	–	–	ns

Notes

1. $T_{frame} = \frac{f_{clk(ext)}}{480}$
2. $\overline{RES}$ may be LOW before V_{DD} goes HIGH.
3. t_{h5} is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$ (see Fig.15).

12.1 Serial interface

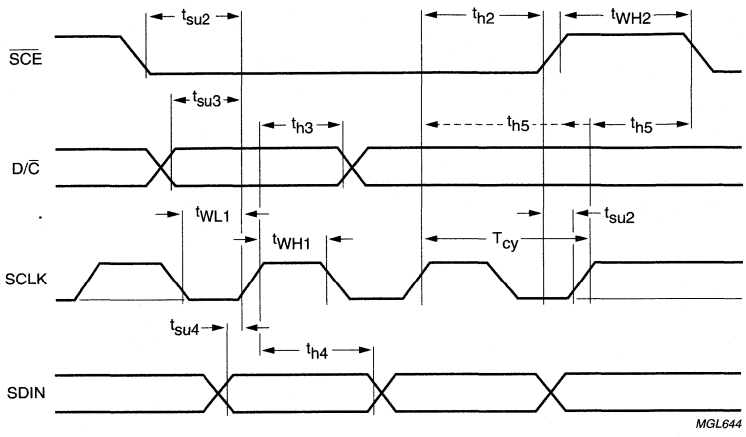


Fig.15 Serial interface timing.

12.2 Reset

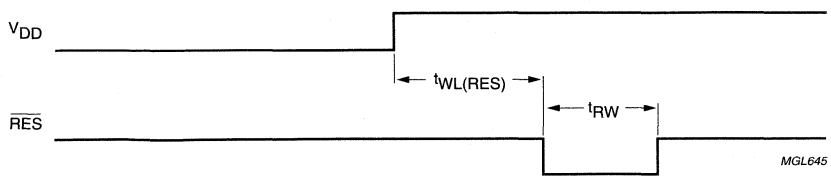
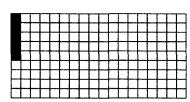
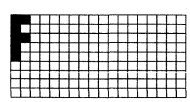
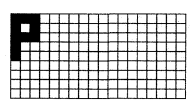
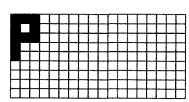
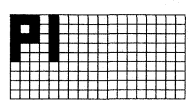
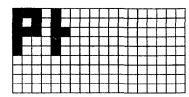
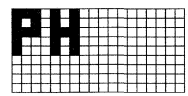
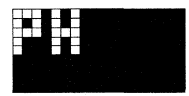
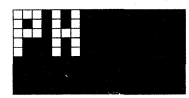


Fig.16 Reset timing.

13 APPLICATION INFORMATION

Table 6 Programming example

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	start										$\overline{SCE}$ is going LOW
2	0	0	0	1	0	0	0	0	1		function set PD = 0 and V = 0, select extended instruction set (H = 1 mode)
3	0	1	0	0	1	0	0	0	0		set V_{OP}; V_{OP} is set to a +16 × b [V]
4	0	0	0	1	0	0	0	0	0		function set PD = 0 and V = 0, select normal instruction set (H = 0 mode)
5	0	0	0	0	0	1	1	0	0		display control set normal mode (D = 1 and E = 0)
6	1	0	0	0	1	1	1	1	1	 MGL673	data write Y and X are initialized to 0 by default, so they are not set here
7	1	0	0	0	0	0	1	0	1	 MGL674	data write
8	1	0	0	0	0	0	1	1	1	 MGL675	data write
9	1	0	0	0	0	0	0	0	0	 MGL675	data write
10	1	0	0	0	1	1	1	1	1	 MGL676	data write

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
11	1	0	0	0	0	0	1	0	0	 MGL677	data write
12	1	0	0	0	1	1	1	1	1	 MGL678	data write
13	0	0	0	0	0	1	1	0	1	 MGL679	display control; set inverse video mode (D = 1 and E = 1)
14	0	1	0	0	0	0	0	0	0	 MGL679	set X address of RAM; set address to '0000000'
15	1	0	0	0	0	0	0	0	0	 MGL680	data write

The pinning is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 48 × 84 pixels.

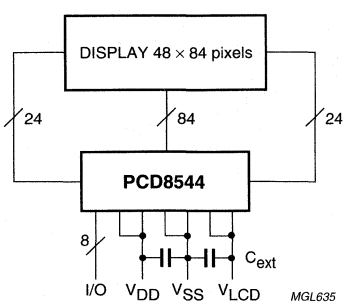


Fig.17 Application diagram.

The required minimum value for the external capacitors is: C_{ext} = 1.0 µF.

Higher capacitor values are recommended for ripple reduction.

14 BONDING PAD LOCATIONS

14.1 Bonding pad information (see Fig.18)

PARAMETER	SIZE
Pad pitch	min. 100 µm
Pad size, aluminium	80 × 100 µm
Bump dimensions	59 × 89 × 17.5 (±5) µm
Wafer thickness	max. 380 µm

14.2 Bonding pad location

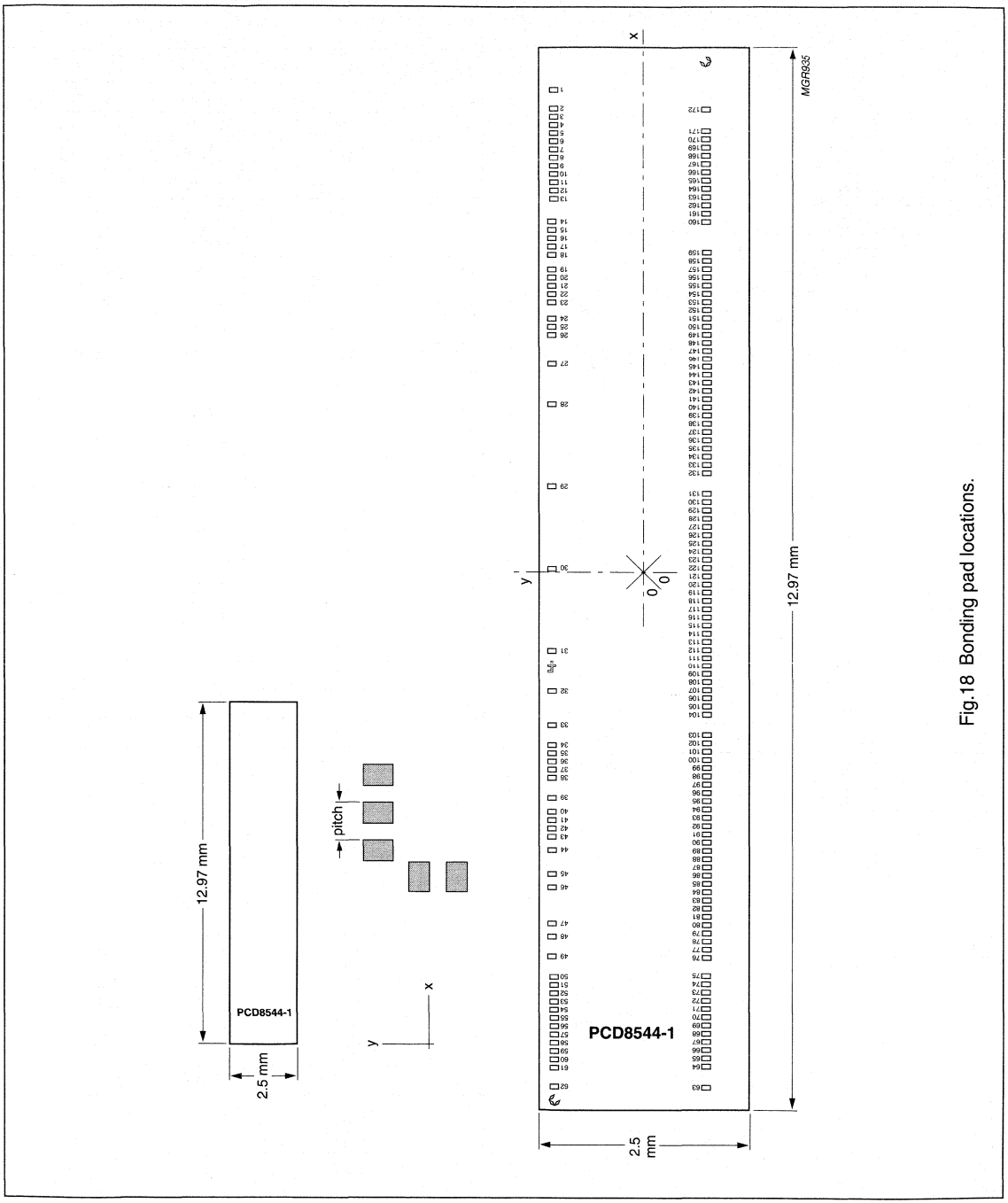


Fig.18 Bonding pad locations.

Table 7 Bonding pad locations (dimensions in μm). All X/Y coordinates are referenced to the centre of chip (see Fig.18)

PAD	PAD NAME	x	y
1	dummy1	+5932	+1060
2	R36	+5704	+1060
3	R37	+5604	+1060
4	R38	+5504	+1060
5	R39	+5404	+1060
6	R40	+5304	+1060
7	R41	+5204	+1060
8	R42	+5104	+1060
9	R43	+5004	+1060
10	R44	+4904	+1060
11	R45	+4804	+1060
12	R46	+4704	+1060
13	R47	+4604	+1060
14	V_{DD1}	+4330	+1085
15	V_{DD1}	+4230	+1085
16	V_{DD1}	+4130	+1085
17	V_{DD1}	+4030	+1085
18	V_{DD1}	+3930	+1085
19	V_{DD2}	+3750	+1085
20	V_{DD2}	+3650	+1085
21	V_{DD2}	+3550	+1085
22	V_{DD2}	+3450	+1085
23	V_{DD2}	+3350	+1085
24	V_{DD2}	+3250	+1085
25	V_{DD2}	+3150	+1085
26	V_{DD2}	+3050	+1085
27	SCLK	+2590	+1085
28	SDIN	+2090	+1085
29	D/$\overline{C}$	+1090	+1085
30	$\overline{SCE}$	+90	+1085
31	$\overline{RES}$	−910	+1085
32	OSC	−1410	+1085
33	T3	−1826	+1085
34	V_{SS2}	−2068	+1085
35	V_{SS2}	−2168	+1085
36	V_{SS2}	−2268	+1085
37	V_{SS2}	−2368	+1085
38	V_{SS2}	−2468	+1085
39	T4	−2709	+1085
40	V_{SS1}	−2876	+1085
41	V_{SS1}	−2976	+1085
42	V_{SS1}	−3076	+1085
43	V_{SS1}	−3176	+1085
44	T1	−3337	+1085
45	V_{LCD2}	−3629	+1085
46	V_{LCD2}	−3789	+1085
47	V_{LCD1}	−4231	+1085
48	V_{LCD1}	−4391	+1085
49	T2	−4633	+1085
50	R23	−4894	+1060
51	R22	−4994	+1060
52	R21	−5094	+1060
53	R20	−5194	+1060
54	R19	−5294	+1060
55	R18	−5394	+1060
56	R17	−5494	+1060
57	R16	−5594	+1060
58	R15	−5694	+1060
59	R14	−5794	+1060
60	R13	−5894	+1060
61	R12	−5994	+1060
62	dummy2	−6222	+1060
63	dummy3	−6238	−738
64	R0	−5979	−738
65	R1	−5879	−738
66	R2	−5779	−738
67	R3	−5679	−738
68	R4	−5579	−738
69	R5	−5479	−738
70	R6	−5379	−738
71	R7	−5279	−738
72	R8	−5179	−738
73	R9	−5079	−738
74	R10	−4979	−738
75	R11	−4879	−738
76	C0	−4646	−746

PAD	PAD NAME	x	y
77	C1	−4546	−746
78	C2	−4446	−746
79	C3	−4346	−746
80	C4	−4246	−746
81	C5	−4146	−746
82	C6	−4046	−746
83	C7	−3946	−746
84	C8	−3846	−746
85	C9	−3746	−746
86	C10	−3646	−746
87	C11	−3546	−746
88	C12	−3446	−746
89	C13	−3346	−746
90	C14	−3246	−746
91	C15	−3146	−746
92	C16	−3046	−746
93	C17	−2946	−746
94	C18	−2846	−746
95	C19	−2746	−746
96	C20	−2646	−746
97	C21	−2546	−746
98	C22	−2446	−746
99	C23	−2346	−746
100	C24	−2246	−746
101	C25	−2146	−746
102	C26	−2046	−746
103	C27	−1946	−746
104	C28	−1696	−746
105	C29	−1596	−746
106	C30	−1496	−746
107	C31	−1396	−746
108	C32	−1296	−746
109	C33	−1196	−746
110	C34	−1096	−746
111	C35	−996	−746
112	C36	−896	−746
113	C37	−796	−746
114	C38	−696	−746
115	C39	−596	−746
116	C40	−496	−746
117	C41	−396	−746

PAD	PAD NAME	x	y
118	C42	−296	−746
119	C43	−196	−746
120	C44	−96	−746
121	C45	+4	−746
122	C46	+104	−746
123	C47	+204	−746
124	C48	+304	−746
125	C49	+404	−746
126	C50	+504	−746
127	C51	+604	−746
128	C52	+704	−746
139	C53	+804	−746
130	C54	+904	−746
131	C55	+1004	−746
132	C56	+1254	−746
133	C57	+1354	−746
134	C58	+1454	−746
135	C59	+1554	−746
136	C60	+1654	−746
137	C61	+1754	−746
138	C62	+1854	−746
139	C63	+1954	−746
140	C64	+2054	−746
141	C65	+2154	−746
142	C66	+2254	−746
143	C67	+2354	−746
144	C68	+2454	−746
145	C69	+2554	−746
146	C70	+2654	−746
147	C71	+2754	−746
148	C72	+2854	−746
149	C73	+2954	−746
150	C74	+3054	−746
151	C75	+3154	−746
152	C76	+3254	−746
153	C77	+3354	−746
154	C78	+3454	−746
155	C79	+3554	−746
156	C80	+3654	−746
157	C81	+3754	−746
158	C82	+3854	−746

PAD	PAD NAME	x	y
159	C83	+3954	−746
160	R35	+4328	−738
161	R34	+4428	−738
162	R33	+4528	−738
163	R32	+4628	−738
164	R31	+4728	−738
165	R30	+4828	−738
166	R29	+4928	−738
167	R28	+5028	−738
168	R27	+5128	−738
169	R26	+5228	−738
170	R25	+5328	−738
171	R24	+5428	−738
172	dummy4	+5694	−738

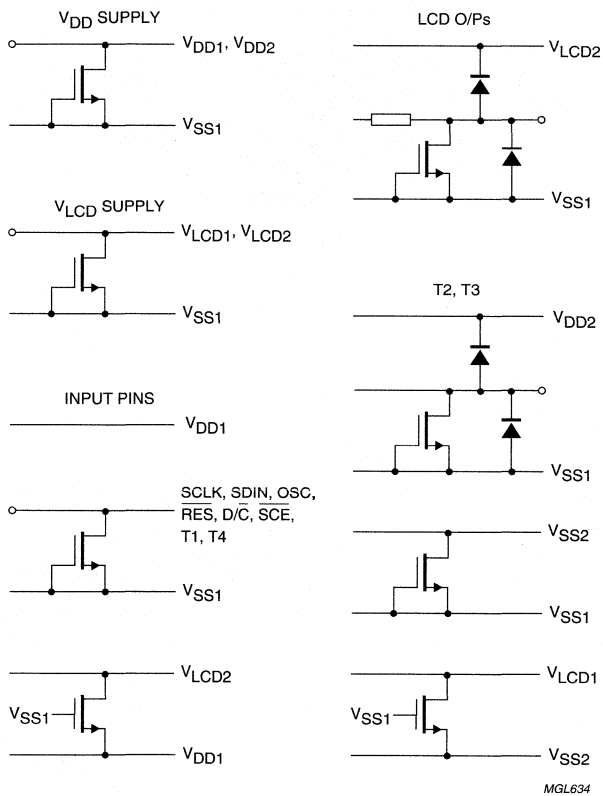
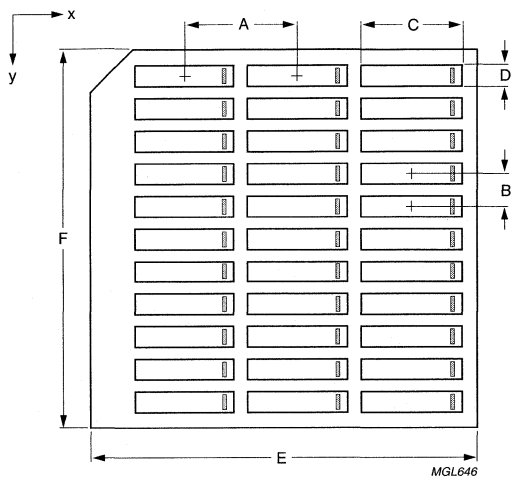


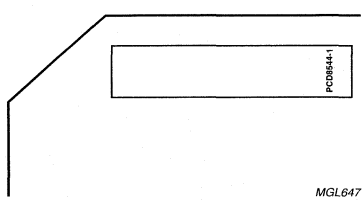
Fig.19 Device protection diagram.

15 TRAY INFORMATION



For the dimensions of x, y and A to F, see Table 8.

Fig.20 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the die surface.

Fig.21 Tray alignment.

Table 8 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, in the x direction	14.82 mm
B	pocket pitch, in the y direction	4.39 mm
C	pocket width, in the x direction	13.27 mm
D	pocket width, in the y direction	2.8 mm
E	tray width, in the x direction	50.67 mm
F	tray width, in the y direction	50.67 mm
x	no. of pockets in the x direction	3
y	no. of pockets in the y direction	11

Threshold detector and reset generator PCF1252-X family

FEATURES

- Very low current consumption, typically 10 μA
- 10 factory programmed threshold voltages available covering trip voltages from 4.75 to 2.55 V
- ±50 mV trip point accuracy over full temperature range
- Variable RESET delay
- RESET pulse polarity selection
- Defined outputs at 0.6 V (typ.)
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power fail
- Operating temperature range –40 to +85 °C.

GENERAL DESCRIPTION

The PCF1252-Xs are low-power CMOS voltage threshold detectors designed especially for supervision of microcontroller/microprocessor systems for detection of power-on/off conditions and generation of a system reset pulse. The PCF1252-X also provides a $\overline{\text{POWF}}$ (power fail) output which is activated at a precise factory-programmed trip point. A system RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}).

A second comparator (comparator 2) has been included to enable the possibility of a second monitoring point in the system.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1252-XP[1]	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF1252-XT[1]	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Note

1. X = 0 to 9; depending on threshold voltage.

BLOCK DIAGRAM

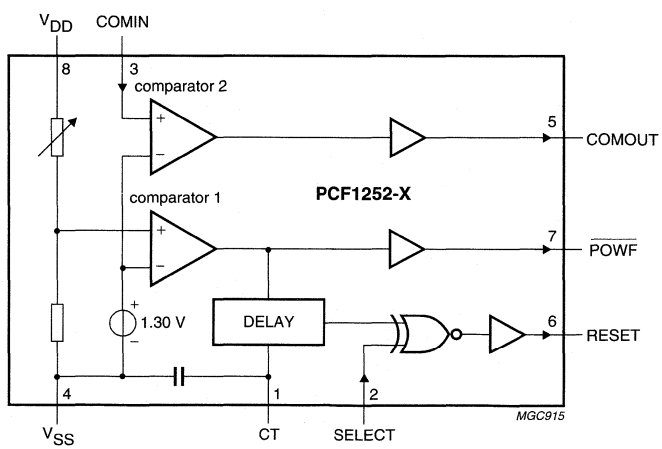


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	connection for the external capacitor
SELECT	2	select polarity or external reset input
COMIN	3	comparator input
V_{SS}	4	ground (0 V)
COMOUT	5	comparator output
RESET	6	reset output
$\overline{POWF}$	7	power failure signal output
V_{DD}	8	supply voltage

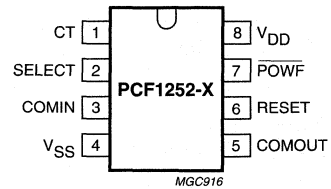


Fig.2 Pinning diagram.

LCD controllers/drivers PCF2103 family

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- Mux rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 5.5 V; chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 120 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2.5 μA.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2103 family is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 or 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2103 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'X' in PCF2103X characterizes the built-in character set. Various character sets can be manufactured on request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2103EU/2/F2	–	chip with bumps in tray	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

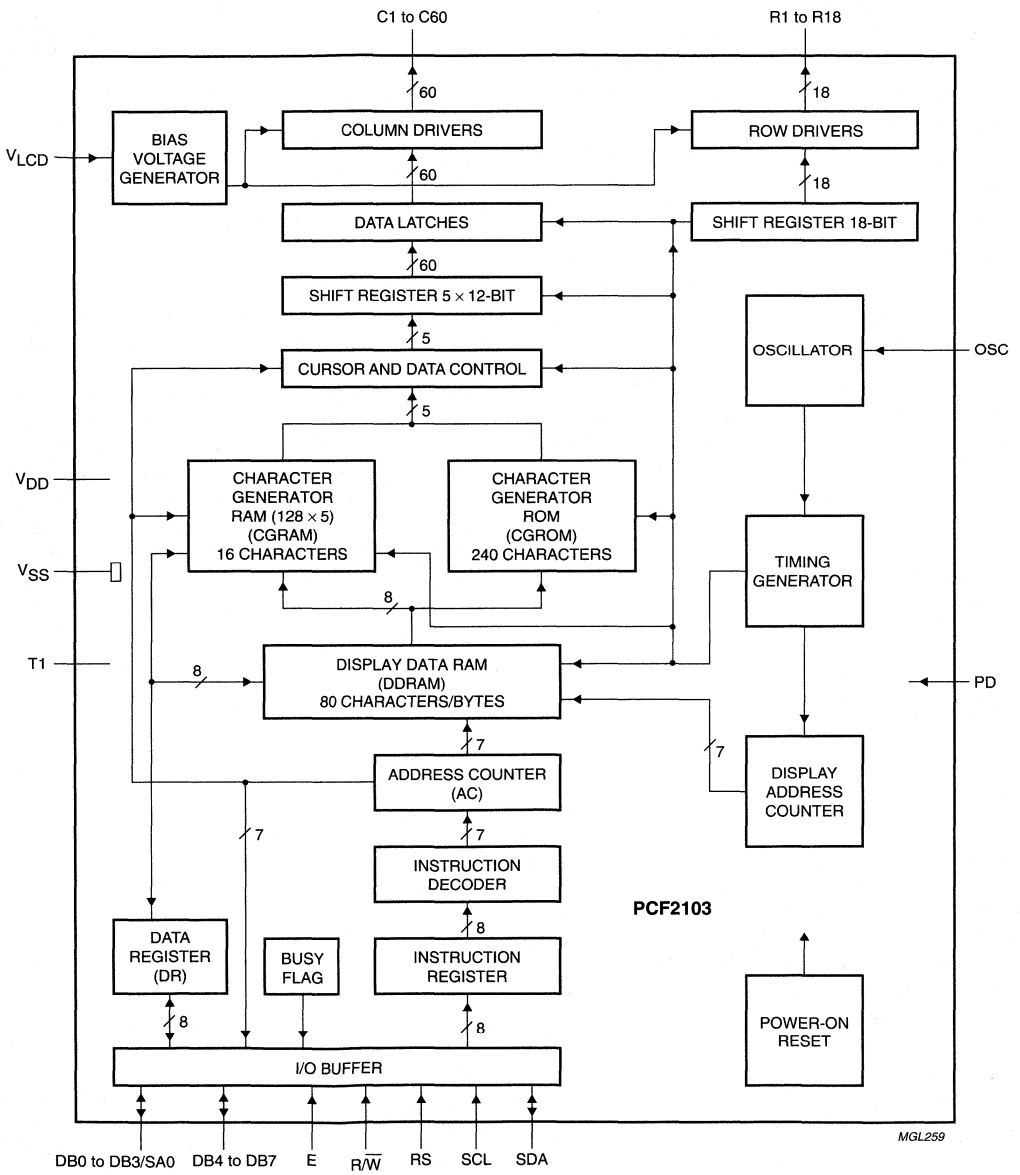


Fig.1 Block diagram.

PINNING

SYMBOL	DIE PAD	DESCRIPTION
V_{DD}	1	supply voltage
OSC	2	oscillator/external clock input
PD	3	power-down pad input
T1	4	test pad (connected to V_{SS})
V_{SS}	5	ground
V_{LCD}	6	V_{LCD} input; note 1
R9 to R16	7 to 14	LCD row driver outputs 9 to 16
R18	15	LCD row driver output 18
C60 to C1	16 to 23, 26 to 50, 53 to 77, 80, 81	LCD column driver outputs 60 to 1
R8 to R1	82 to 89	LCD row driver outputs 8 to 1
R17	90	LCD row driver output 17
SCL	91	I^2C-bus serial clock input
SDA	92	I^2C-bus serial data input/output
E	93	data bus clock input
RS	94	register select input
R/$\overline{W}$	95	read/write input
DB7	96	bit of bi-directional data bus
DB6	97	bit of bi-directional data bus
DB5	98	bit of bi-directional data bus
DB4	99	bit of bi-directional data bus
DB3/SA0	100	bit of bi-directional data bus/I^2C-bus address pin
DB2	101	bit of bi-directional data bus
DB1	102	bit of bi-directional data bus
DB0	103	bit of bi-directional data bus

Note

1. This is the voltage used for the generation of LCD bias levels.

Table 1 Pin functions; note 1

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write; there is an internal pull-up on this pin RS = 0 selects the instruction register for write and the busy flag and address counter for read RS = 1 selects the data register for both read and write
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation; there is an internal pull-up on this pin
E	data bus clock	pin E is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock
DB7 to DB0	data bus	the bi-directional, 3-state data bus transfers data between the system controller and the PCF2103; DB7 may be used as the busy flag, signalling that internal operations are not yet completed; in 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit; there is an internal pull-up on each of the data lines
C1 to C60	column driver outputs	these pins output the data for columns
R1 to R18	row driver outputs	these pins output the row select waveforms to the display; R17 and R18 drive the icons
V_{LCD}	LCD power supply	positive power supply for the liquid crystal display
OSC	oscillator	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
SCL	serial clock line	input for the I²C-bus clock signal
SDA	serial data line	I/O for the I²C-bus data line
SA0	address pin	the hardware sub-address line is used to program the device sub-address for two different PCF2103s on the same I²C-bus
T1	test pad	must be connected to V_{SS}; not user accessible
PD	power-down pad	PD selects chip power-down mode; for normal operation PD = 0

Note

1. When the I²C-bus is used, the parallel interface pin E must be defined as E = 0. In I²C-bus read mode DB7 to DB0 should be connected to V_{DD} or left open-circuit.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS} or V_{DD}; they may not be left unconnected.
   b) If the 4-bit interface is used without reading out from the PCF2103 (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

LCD controllers/drivers PCF2104x

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.
- I²C-bus address: 011101 SA0.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2104x integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

The PCF2104x is optimized for chip-on-glass applications. The 'x' in 'PCF2104x' represents a specific letter code for a character set in the character generator ROM (CGROM).

Two standard character sets are currently available, specified by the letters 'C' and 'L'. Other character sets are available on request.

The PCF2104x is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104x interfaces to most microcontrollers via a 4 or 8-bit bus, or via the 2-wire I²C-bus.

Packages

- PCF2104xU/2; chip with bumps in tray
- PCF2104xU/7; chip with bumps on tape.

Available types

- PCF2104CU/x: character set 'C' in CGROM
- PCF2104LU/x: character set 'L' in CGROM
- PCF2104NU/x: character set 'N' in CGROM.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2104CU/2	–	chip with bumps in tray	–
PCF2104CU/7	–	chip with bumps on tape	–
PCF2104LU/2	–	chip with bumps in tray	–
PCF2104LU/7	–	chip with bumps on tape	–
PCF2104NU/2	–	chip with bumps in tray	–
PCF2104NU/7	–	chip with bumps on tape	–

BLOCK DIAGRAM

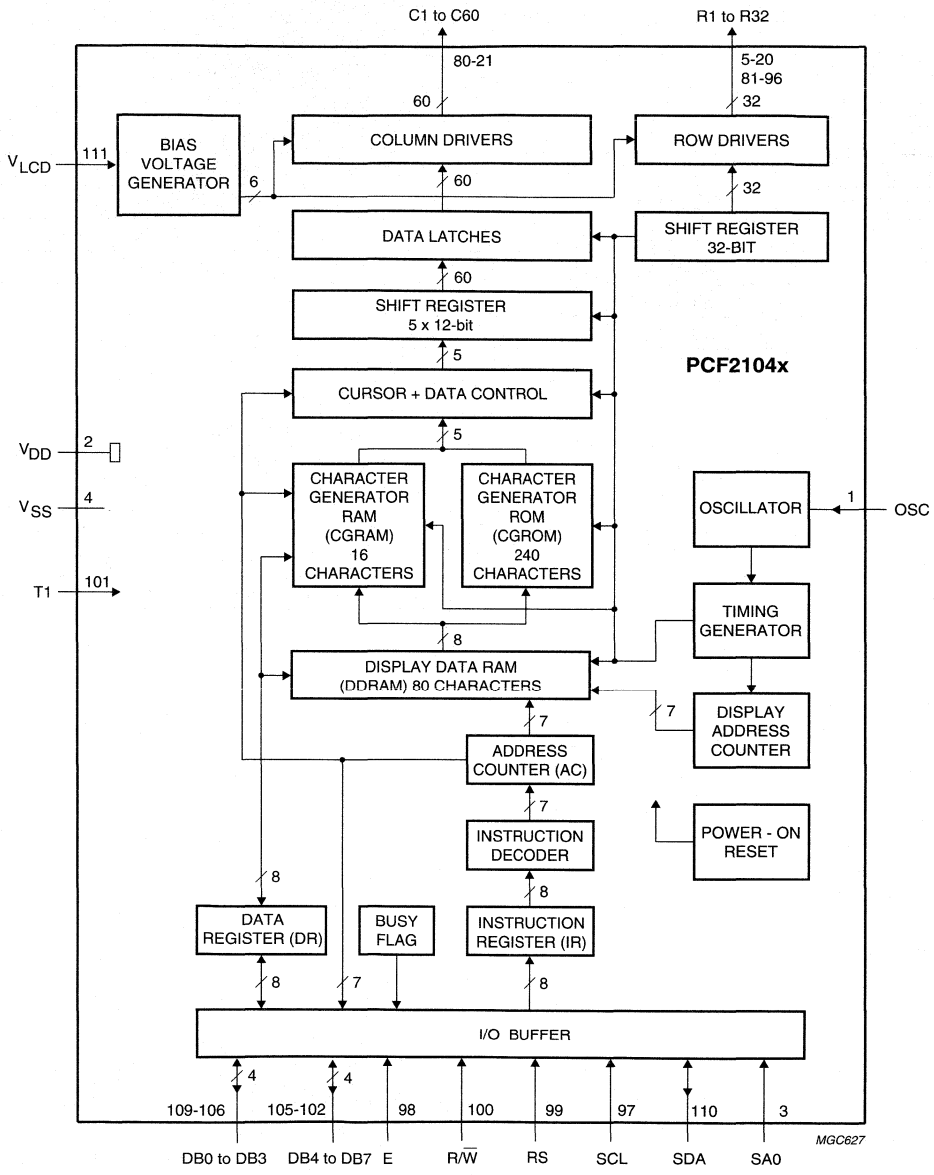


Fig.1 Block diagram.

PINNING

SYMBOL	FFC PAD	TYPE	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	P	logic supply voltage
SA0	3	I	I^2C-bus address pin input
V_{SS}	4	P	ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I^2C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
$R/\overline{W}$	100	I	read/write input
T1	101	I	test pad input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I^2C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

LCD controller/driver PCF2105

FEATURES

- Single chip Liquid Crystal Display (LCD) controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4-line display of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip generation of intermediate LCD bias voltages
- On-chip oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface (400 kHz)
- CMOS and TTL compatible
- 32 row, 60 column outputs
- Multiplex (MUX) rates 1 : 32 and 1 : 16
- Uses common 11-code instruction set
- Logic supply voltage range: $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range: $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption
- I²C-bus address selection (SA0): 011101.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2105 integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device. Furthermore, a fast I²C-bus interface (400 kHz) is provided.

The PCF2105 is optimized for chip-on-glass applications.

A specific letter code 'M' for a character set is programmed in the Character Generator ROM (CGROM).

The PCF2105 is a low power CMOS LCD controller/driver, designed to drive a split screen dot matrix LCD of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pads does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2105 interfaces to most microcontrollers via a 4 or 8-bit parallel bus, or via the 2-wire I²C-bus.

Packages

- PCF2105MU/2: chip with bumps in tray.

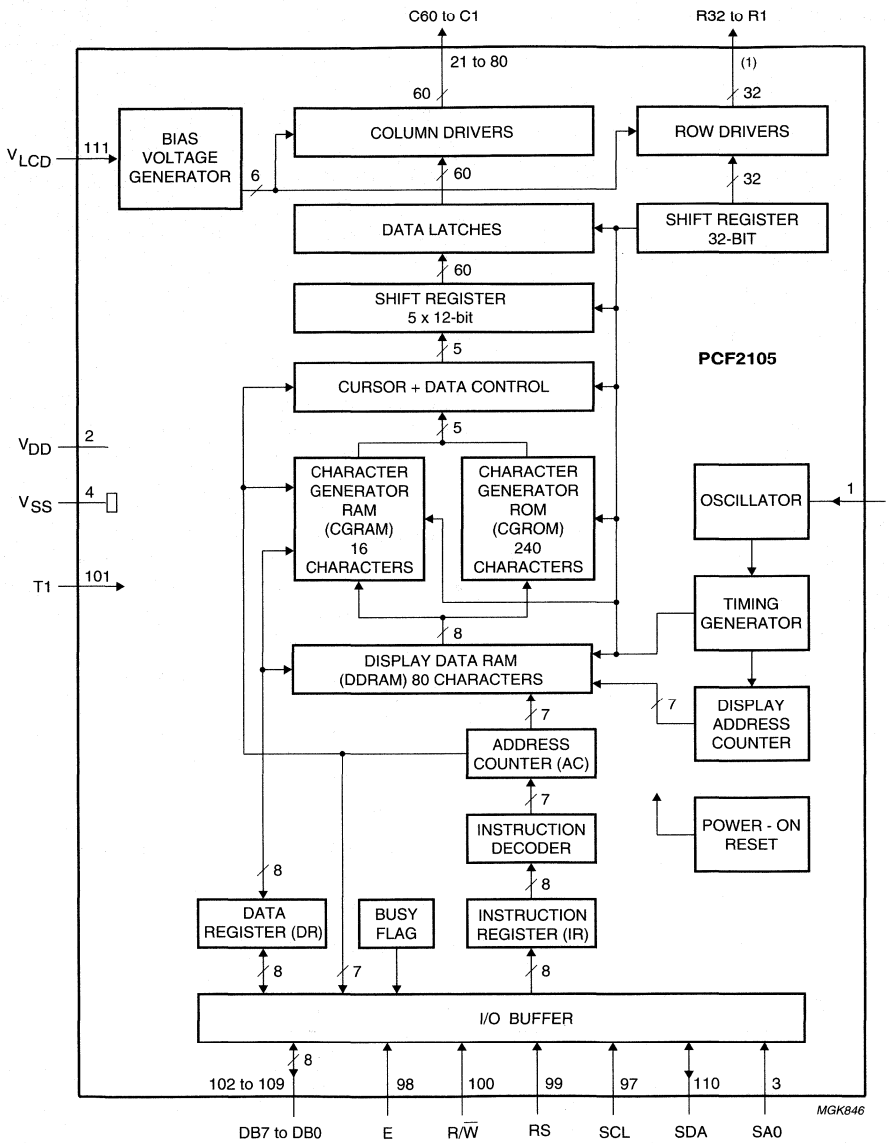
Available types

- PCF2105MU/2: character set 'M' in CGROM.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2105MU/2	–	chip with bumps in tray	–

BLOCK DIAGRAM



(1) Pads 5 to 8 and 9 to 12 correspond with symbols R8 to R5 and R32 to R29.
Pads 13 to 20 and 81 to 88 correspond with symbols R24 to R17 and R9 to R16.
Pads 89 to 92 and 93 to 96 correspond with symbols R25 to R28 and R1 to R4.

Fig.1 Block diagram.

PINNING

SYMBOL	PAD	I/O	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	–	logic supply voltage
SA0	3	I	I^2C-bus address selection input
V_{SS}	4	–	logic ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to 12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I^2C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I^2C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

LCD controller/driver PCF2113x

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: −8 to −12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- MUX rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - icon mode: <25 μA
  - power-down mode: <2.5 μA.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2113x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 and 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip co cter sets (A, D and E) are currently available. Various other character sets can be manufactured on request.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}. Never use the voltage generator in icon mode.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2113AU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/F2	–	chip in tray	–
PCF2113DH/F2	LQFP100	plastic low profile quad flat package; 100 leads; body $14 \times 14 \times 1.4$ mm	SOT407-1
PCF2113EU/2/F2	–	chip with bumps in tray	–

BLOCK DIAGRAM

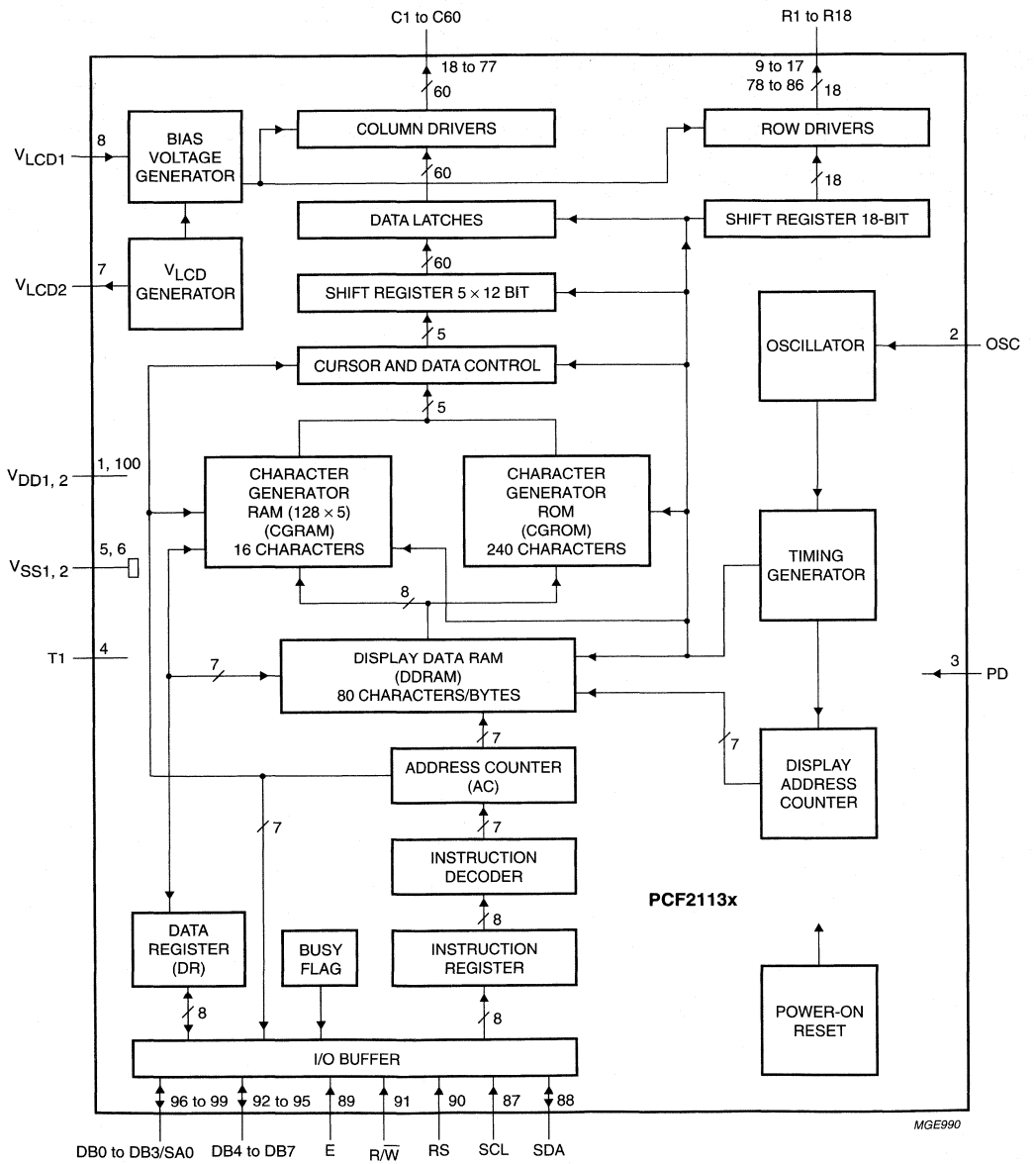


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DD1}	1	P	supply voltage for all except high voltage generator
OSC	2	I	oscillator/external clock input
PD	3	I	power-down pad input
T1	4	I	test pad (connected to V_{SS})
V_{SS1}	5	P	ground for all except high voltage generator
V_{SS2}	6	P	ground for high voltage generator
V_{LCD2}	7	O	V_{LCD} output; note 1
V_{LCD1}	8	I	V_{LCD} input; note 2
R9 to R16	9 to 16	O	LCD row driver outputs 9 to 16
R18	17	O	LCD row driver output 18
C60 to C1	18 to 77	O	LCD column driver outputs 60 to 1
R8 to R1	78 to 85	O	LCD row driver outputs 8 to 1
R17	86	O	LCD row driver output 17
SCL	87	I	I^2C serial clock input
SDA	88	I/O	I^2C serial data input/output
E	89	I	data bus clock input
RS	90	I	register select input
R/$\overline{W}$	91	I	read/write input
DB7	92	I/O	1 bit of 8-bit bidirectional data bus
DB6	93	I/O	1 bit of 8-bit bidirectional data bus
DB5	94	I/O	1 bit of 8-bit bidirectional data bus
DB4	95	I/O	1 bit of 8-bit bidirectional data bus
DB3/SA0	96	I/O	1 bit of 8-bit bi-directional data bus/I^2C address pin
DB2	97	I/O	1 bit of 8-bit bidirectional data bus
DB1	98	I/O	1 bit of 8-bit bidirectional data bus
DB0	99	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	100	P	supply voltage for high voltage generator; note 3

Notes

1. This is the V_{LCD} output pin, if V_{LCD} is generated internally and has to be connected to V_{LCD1}. If V_{LCD1} is generated externally, V_{LCD2} has to be left open or connected to ground.
2. This is the voltage used for the generation of LCD bias levels.
3. This is the supply for the high voltage generator. If V_{LCD} is generated externally, connect V_{DD2} to V_{SS}.

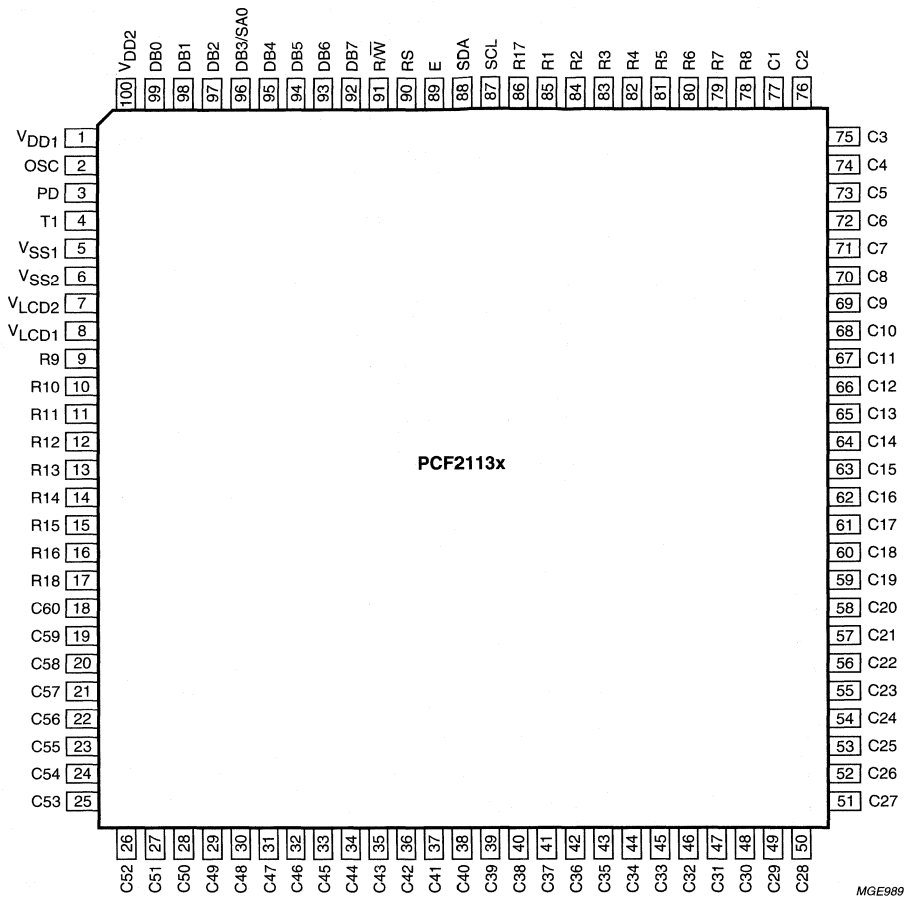


Fig.2 Pin configuration (LQFP100).

PIN FUNCTIONS

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. There is an internal pull-up on this pin. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write.
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when the device is controlled by the parallel interface. There is an internal pull-up on this pin.
E	data bus clock	The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.
DB7 to DB0	data bus	The parallel interface of the device. This bi-directional, 3-state data bus transfers data between the system controller and the PCF2113x. There is an internal pull-up on each of the data lines. DB7 to DB0 must be connected to V_{DD} or left open circuit when I^2C-bus control is used. Note that DB3 shares the same pin as SA0. In 4-bit operations only DB7 to DB4 are used, and DB3 to DB0 must be left open circuit. See note 1. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed.
C1 to C60	column driver outputs	These pins output the data for columns.
R1 to R18	row driver outputs	These pins output the row select waveforms to the display. R17 and R18 drive the icons.
V_{LCD}	LCD power supply	Positive power supply for the liquid crystal display. This may be generated on-chip or supplied externally.
OSC	oscillator	When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.
SCL	serial clock line	Input for the I^2C-bus clock signal. SCL must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SDA	serial data line	I/O for the I^2C-bus data line. SDA must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SA0	address pin	The hardware sub-address line is used to program the device sub-address for two different PCF2113xs on the same I^2C bus. Note that SA0 shares the same pin as DB3.
T1	test pad	T1 must be connected to V_{SS} and is not user accessible.
PD	power-down pad	PD selects chip power-down mode. For normal operation PD = logic 0.

Note

1. If the 4-bit interface is used without reading out from the PCF2113x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The specific differences are expressed in separate paragraphs for PCF2116X and PCF2114X respectively.

The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J. Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

The PCF2116K differs from the existing PCF2116 family only in the V_{LCD}/V_{OP} generation section.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116K; LQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2114XU/2116XU	116	FFC116	–
PCF2116KH/KHZ	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

BLOCK DIAGRAM

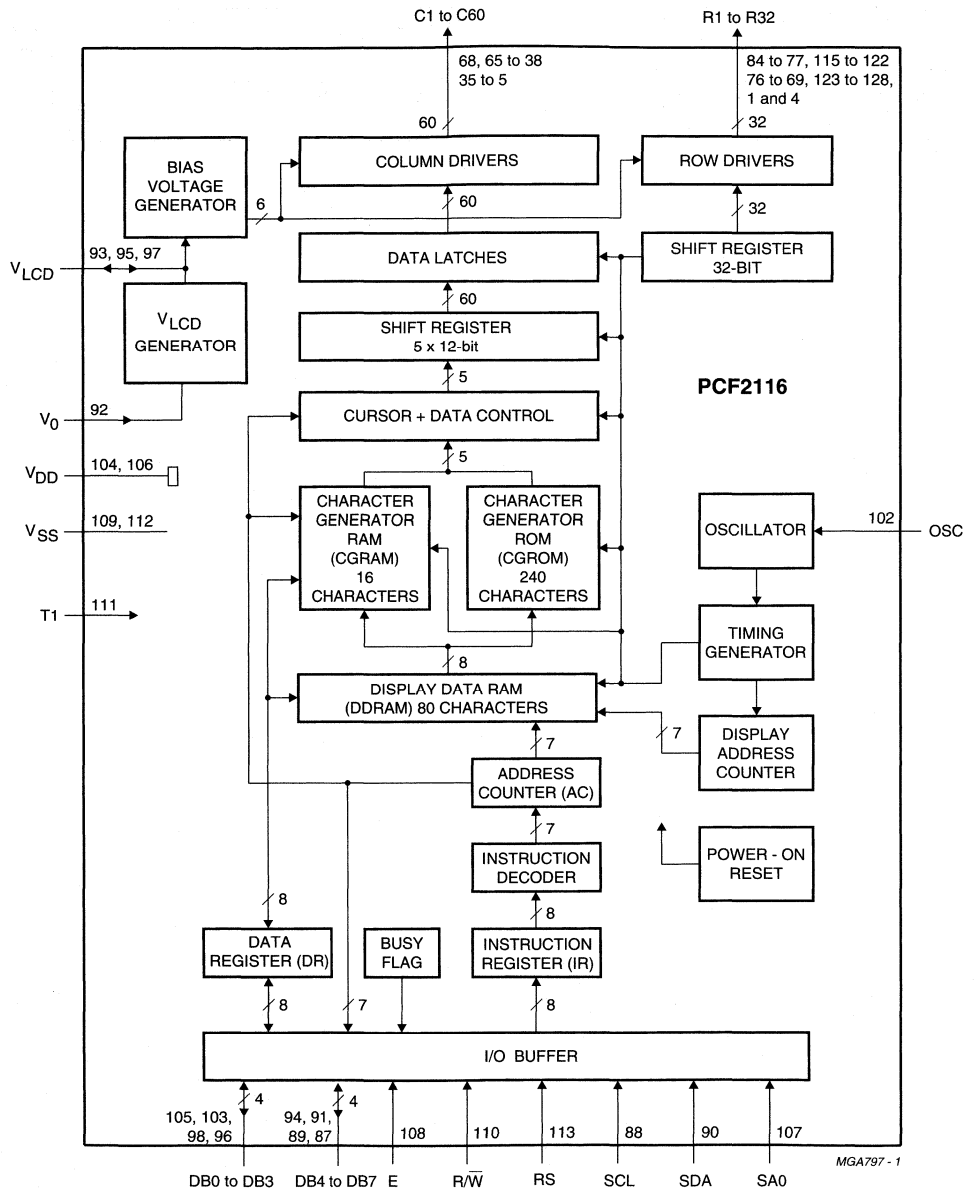


Fig.1 Block diagram.

PINNING

SYMBOL	LQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^2C-bus serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^2C-bus serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^2C-bus address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

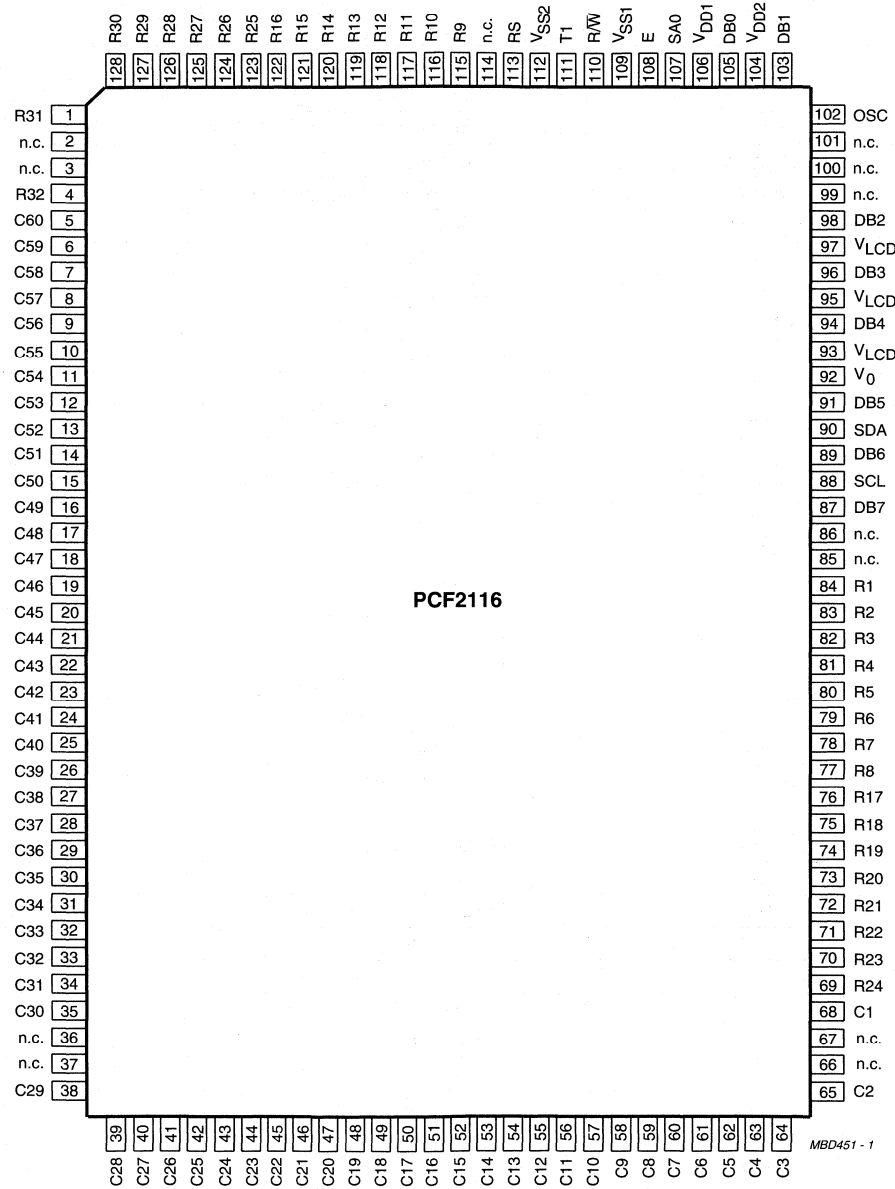


Fig.2 Pin configuration.

LCD controllers/drivers PCF2119X

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, or 1-line display of up to 32 characters + 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - Generation of LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: −8 to −12 mV/K at 5.0 V (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- Display Data RAM: 80 characters
- Character Generator ROM: 240, 5 × 8 characters
- Character Generator RAM: 16, 5 × 8 characters; 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row and 80 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 2.2 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2 μA.

Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2119x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 16 or 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PC2119RU/2	–	chip with bumps in tray	–
PC2119SU/2	–	chip with bumps in tray	–
PC2119VU/2	–	chip with bumps in tray	–

BLOCK DIAGRAM

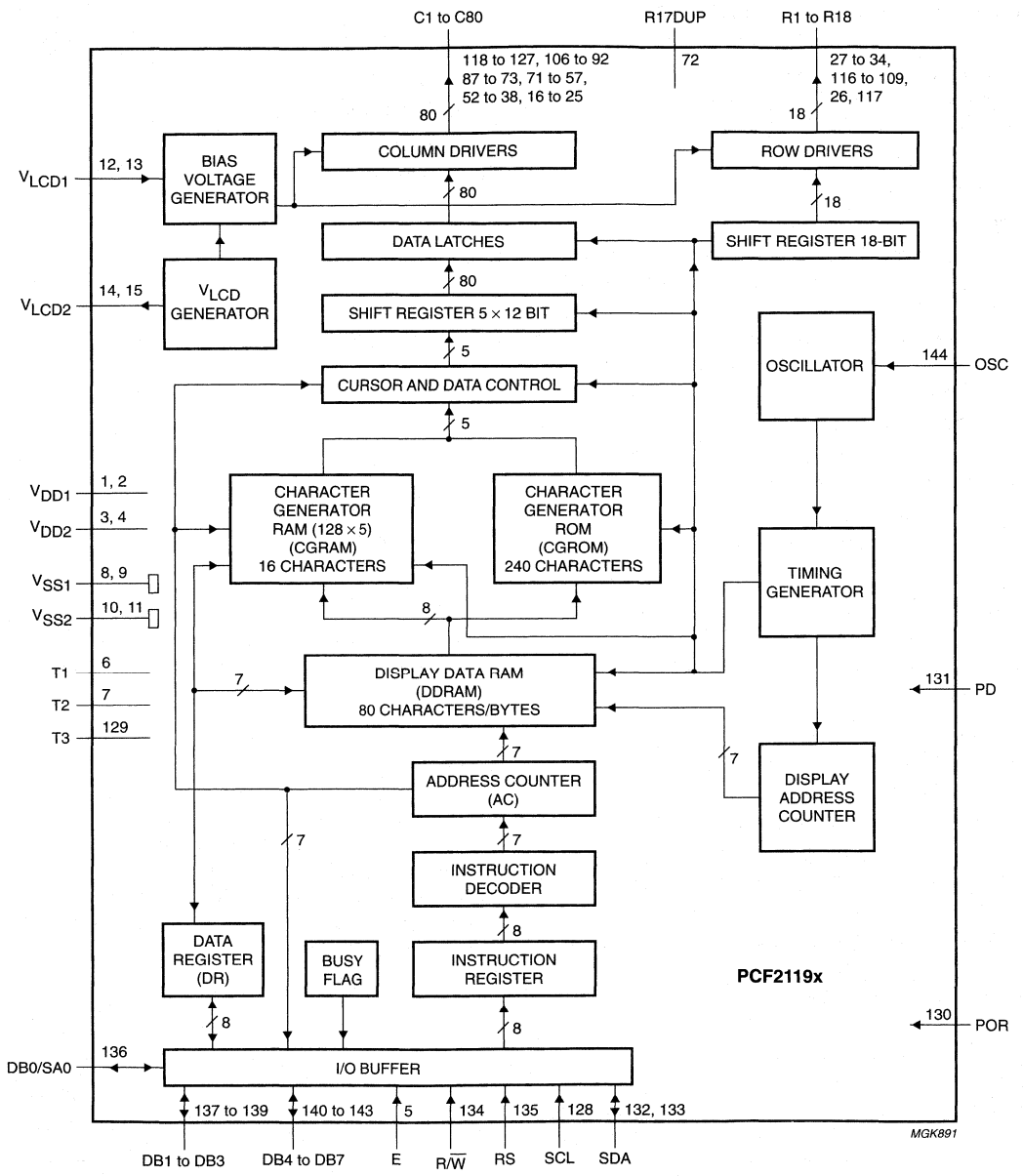


Fig.1 Block diagram.

PAD INFORMATION

Pad functions

Table 1 Pad function description

SYMBOL	DESCRIPTION
V_{DD1}	Supply voltage for all except the high voltage generator.
V_{DD2}	Supply voltage for the high voltage generator.
V_{SS1}	This is the ground pad for all except the high voltage generator.
V_{SS2}	This is the ground pad for the high voltage generator.
V_{LCD1}	This input is used for the generation of the LCD bias levels.
V_{LCD2}	This is the V_{LCD} output pad if V_{LCD} is generated internally. This pad must be connected to V_{LCD1}.
E	The data bus clock input is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock; note 1.
T1	These are three test pads. T1 and T2 must be connected to V_{SS1}; T3 is left open-circuit and is not user accessible.
T2	
T3	
R1 to R18; R17DUP	LCD row driver outputs R1 to R18; these pads output the row select waveforms to the display; R17 and R18 drive the icons. R17 has two pads R17 and R17DUP.
C1 to C80	LCD column driver outputs C1 to C80.
SCL	I²C-bus serial clock input; note 1.
POR	External power-on reset input.
PD	PD selects the chip power-down mode; for normal operation PD = 0.
SDA	I²C-bus serial data input/output; note 1.
R/$\overline{W}$	This is the read/write input. R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation. This pad has an internal pull-up resistor.
RS	The RS input selects the register to be accessed for read and write. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write. This pad has an internal pull-up resistor.
DB0 to DB7	The 8-bit bidirectional data bus (3-state) transfers data between the system controller and the PCF2119x. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit. Data bus line DB3 has an alternative function (SA0), when selected this is the I²C-bus address pad. Each data line has its own internal pull-up resistor; note 1.
OSC	Oscillator or external clock input. When the on-chip oscillator is used this pad must be connected to V_{DD1}.

Note

1. When the I²C-bus is used, the parallel interface pad E must be at logic 0. In the I²C-bus read mode DB7 to DB0 should be connected to V_{DD1} or left open-circuit.
   a) When the parallel bus is used, pads SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open-circuit.
   b) If the 4-bit interface is used without reading out from the PCF2119x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

LCD drivers PCF21xxC family

FEATURES

- Supply voltage 2.25 to 6.0 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments
  - 40 (PCF2100C)
  - 64 (PCF2111C)
  - 32 (PCF2112C)
- Multiplex rate
  - 1 : 2 (PCF2100C)
  - 1 : 2 (PCF2111C)
  - 1 : 1 (PCF2112C)
- Word length
  - 22 bits (PCF2100C)
  - 34 bits (PCF2111C)
  - 34 bits (PCF2112C).

GENERAL DESCRIPTION

The PCF21xxC family are single-chip, silicon gate CMOS LCD driver circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The devices have the same function and performance as those of the PCF21xx family, which they supersede. The maximum operating voltage required is reduced from 6.5 to 6.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	μA
I_{DD2}	supply current 2	outputs open; CBUS inactive; T_{amb} = 25 °C	–	20	30	μA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAMS

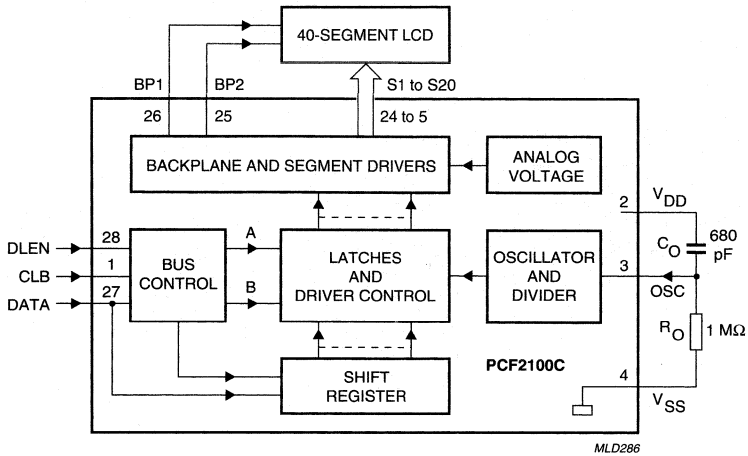


Fig.1 Block diagram; PCF2100C.

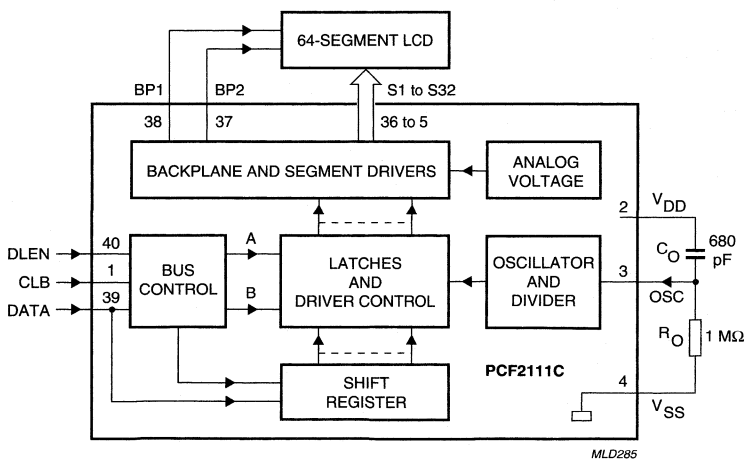


Fig.2 Block diagram; PCF2111C.

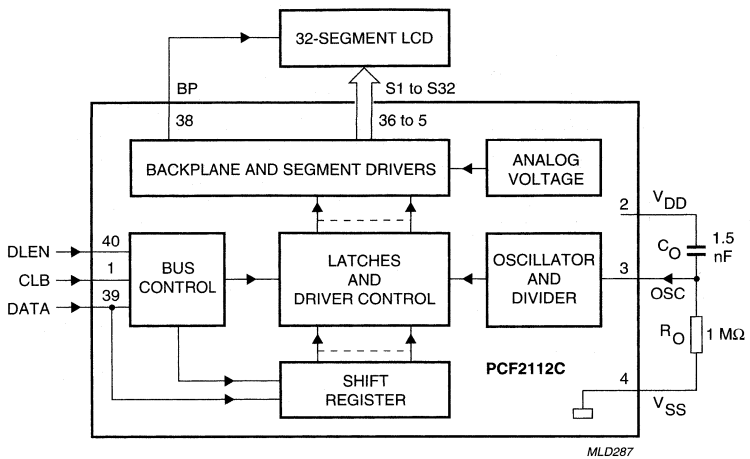


Fig.3 Block diagram; PCF2112C.

PINNING

PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	data input line (CBUS)
DLEN	28	data input line enable (CBUS)

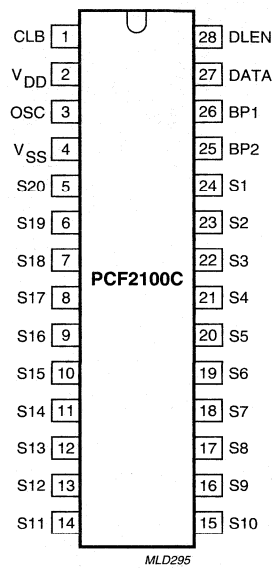


Fig.4 Pin configuration; SOT117-1 and SOT136-1.

PCF2111C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

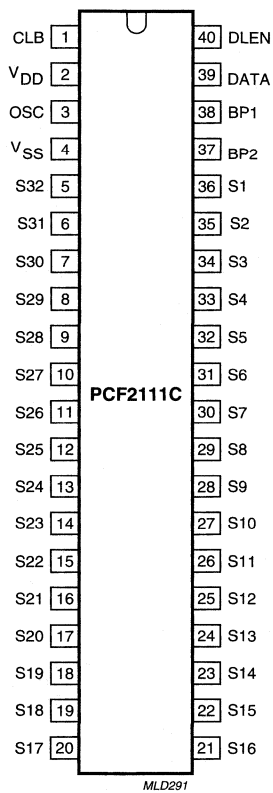


Fig.5 Pin configuration; SOT129-1 and SOT158-1.

PCF2112C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

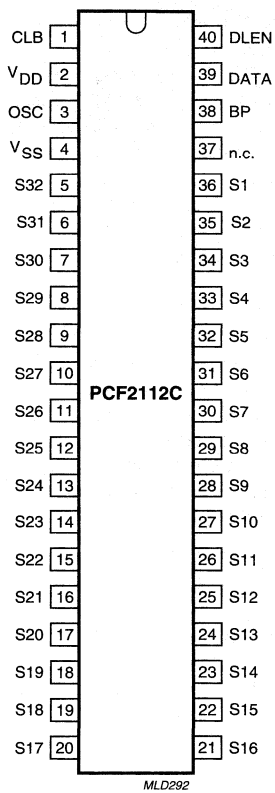


Fig.6 Pin configuration; SOT129-1 and SOT158-1.

CONTENTS

POCSAG Paging Decoder PCF5001

1 FEATURES

- Wide operating supply voltage range (1.5 to 6.0 V)
- Extended temperature range: −40 to +85 °C (between −40 to −10 °C, minimum supply voltage restricted to 1.8 V)
- Very low supply current (60 µA typ. with 76.8 kHz crystal)
- *"CCIR radio paging Code No 1"* (POCSAG) compatible
- Programmable call termination conditions
- 512 and 1200 bits/s data rates (2400 bits/s with some restrictions), see Section 7.4
- Improved ACCESS® synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2050T, UAA2080 and UAA2082 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

2 APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

3 GENERAL DESCRIPTION

The PCF5001 is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 (POCSAG-Code) at 512 and 1200 bits/s data rates. The PCF5001 is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5001T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF5001H	LQFP32(1)	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9397 750 00192) are followed.

5 BLOCK DIAGRAMS

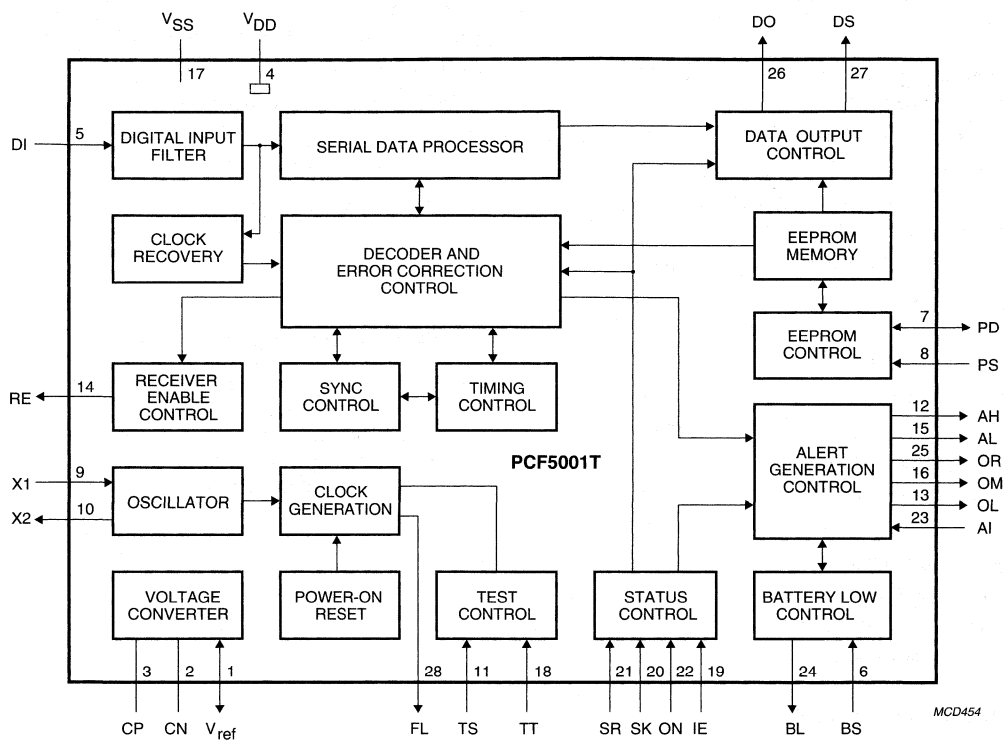


Fig.1 Block diagram (SO28; SOT136-1).

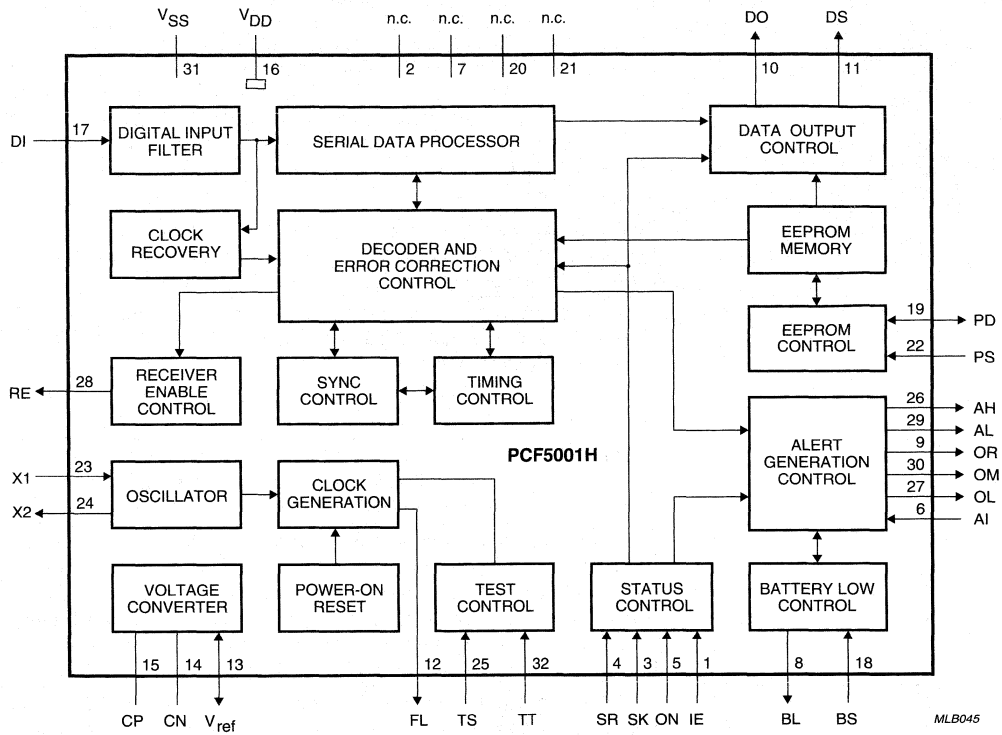


Fig.2 Block diagram (LQFP32; SOT358-1).

6 PINNING

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
V_{ref}	1	13	Microcontroller interface reference voltage input/output. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{ref}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a doubled negative output voltage.
CN	2	14	Voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3	15	Voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4	16	Main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	17	Serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	18	Battery-low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery-low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery-low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.
PD	7	19	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bidirectional data and control signal.
PS	8	22	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a unidirectional control input.
X1	9	23	Crystal oscillator input. Connect a 32768 Hz or 76800 Hz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	24	Crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	25	Scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	26	Alert HIGH-level output. This output can directly drive an external bipolar transistor to control HIGH-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	27	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of an LED. It may also be used for visual indication of received call data during call reception.

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
RE	14	28	Receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH-level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	29	Alert LOW-level output. Open drain alert output in anti-phase to AH, to provide LOW-level alerting. HIGH-level alerting is generated in conjunction with AH.
OM	16	30	Vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17	31	Main negative supply voltage.
TT	18	32	Test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	1	Interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made high-impedance. In **alert-only pager** mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	3	SILENT state control input. The SILENT control input selects the decoder ON status (LOW-level) or SILENT status (HIGH-level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for 'alert-only pager' mode, whereby the pull-up is disabled for **display pager** mode. In 'display pager' mode status change is possible if the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	4	Status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery-low alert, if active or (c) triggers the call store re-alert facility, if **repeat** mode is active. In 'display pager' mode operation of SR is possible only if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.
ON	22	5	On/off control input. The on/off control input selects the decoder ON status (HIGH-level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for 'alert-only pager' mode, but the pull-up resistor is disabled for 'display pager' mode. In 'display pager' mode, status change is possible if the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	6	Alarm input. A HIGH-level on this input causes generation of a continuous HIGH-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in 'alert-only pager' mode by operation of an on-chip pull-down.

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
BL	24	8	Battery-low indication output. If the decoder encounters a battery-low condition a battery-low output latch is set HIGH. The battery-low output latch may be tested for a battery-low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery-low output is made high-impedance. The battery-low output latch is reset only, by switching the decoder to OFF status.
OR	25	9	Out-of-range indication output. Whenever the decoder detects an out-of-range condition an out-of-range output latch is set HIGH after expiry of the programmed out-of-range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made high-impedance. The out-of- range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	10	Serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	11	Serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	12	Frequency reference output. When programmed for 'display pager' mode, this output provides a clock reference with 16384 or 32768 Hz per second, selected by SPF32. See Chapter 7.
n.c.	–	2, 7, 20, 21	Not connected.

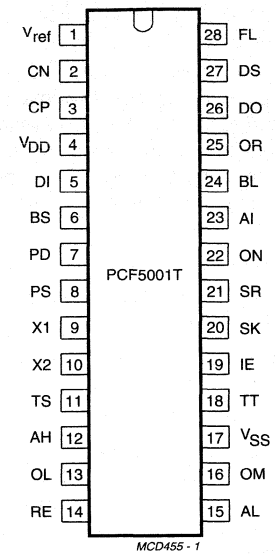


Fig.3 Pin configuration PCF5001T (SOT136-1).

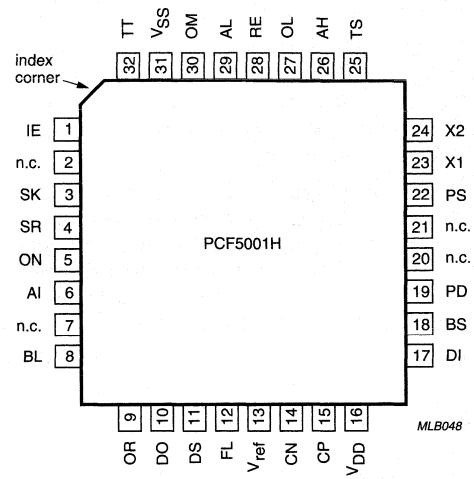


Fig.4 Pin configuration PCF5001H (SOT358-1).

7 FUNCTIONAL DESCRIPTION

The PCF5001 is a very low power Decoder and Pager Controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001 allows for flexible application in a wide variety of radio pager designs.

The PCF5001 is fully compatible with *"CCIR radio paging Code Number 1"* (also known as the POCSAG code) operating at the originally specified 512 bits/s data rate, and also at the newly specified 1200 bits/s data rate (2400 bits/s operation is also possible). The PCF5001 also offers features which extend the basic flexibility and efficiency of this code standard.

7.1 The PCF5001 supports two basic modes of operation

In **alert-only pager** mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is achieved using a slider switch interface.

In **display pager** mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS® algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

7.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.5).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or to separate messages.

Address codewords are identified by an MSB at logic 0 and are coded as shown in Fig.5. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different call types ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished. The call type is determined by two function bits in the address codeword (bits 20 and 21).

Alert-only calls consist only of a single address codeword. Numeric and alphanumeric calls have message codewords following the address. A message causes the frame structure to be temporarily suspended. Message codewords are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message codewords are identified by an MSB at logic 1 and are coded as shown in Fig.5. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

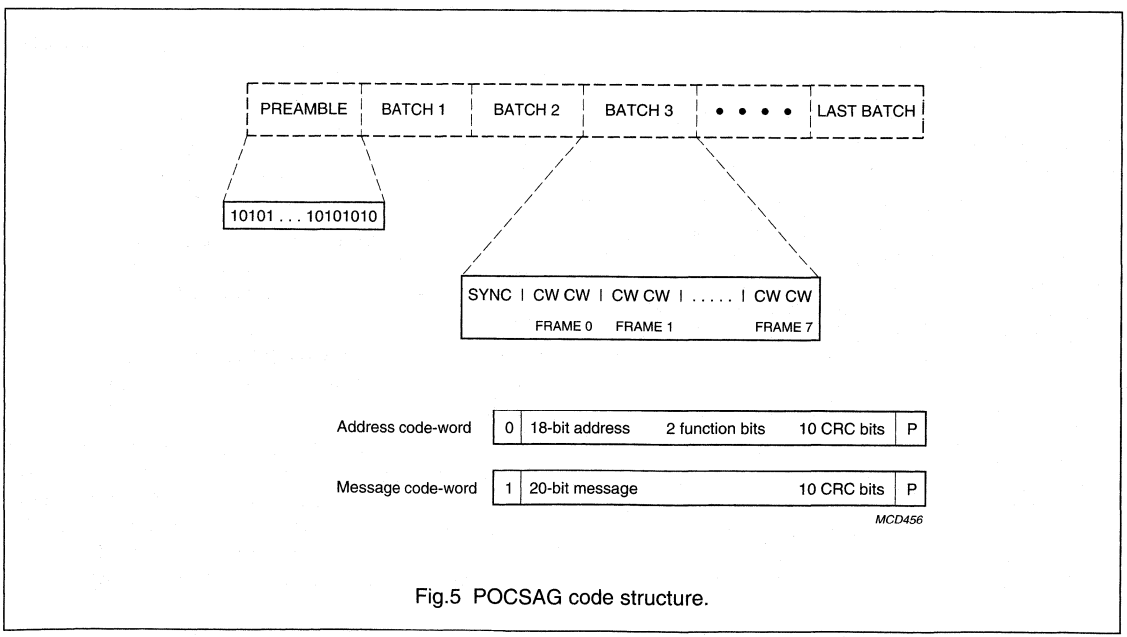


Fig.5 POCSAG code structure.

7.3 Modes and states of the decoder

The PCF5001 supports two basic operating modes:

- 'Alert-only pager' mode
- 'Display pager' mode.

Two further modes, the **programming** mode and the **test** mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In 'alert-only pager' mode no external microcontroller is required, see Fig.22. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in SILENT status and to recall cadences upon 'repeat' mode operation.
The voltage doubler and the frequency reference output are disabled in this mode.

In 'display pager' mode the PCF5001 operates as decoder and pager controller in combination with an external microcontroller (see Fig.23). The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The SILENT status is the same as the ON status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as 'alert-only pager', the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the ON status. However, special SILENT override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for 'alert-only pager' a switch debounce period is applied to the status inputs. For status change and status interrogation in 'display pager' mode, see Figs 6 and 7.

Table 1 Truth table for decoder operating status

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note

1. The EEPROM transfer mode applies to 'display pager' mode only.

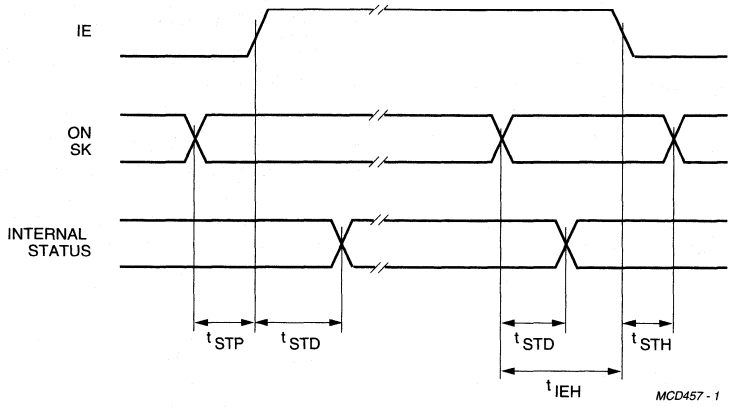


Fig.6 Status change in display pager mode.

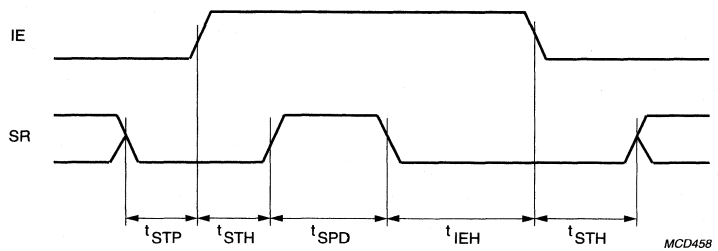


Fig.7 Status interrogation in display pager mode.

7.4 Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001 supports 512 bits/s and 1200 bits/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS® algorithm, which employs a state machine with six internal states.

A data rate of 2400 bits/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then −1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed. The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns.

This is carried out for the duration of 3 batches in **power-on** mode or 1 batch (=preamble duration) in **preamble receive** mode. Error correction algorithms are applied to the data before it is compared with preamble and synchronization codeword patterns.
The synchronization process is terminated and thus **data receive** mode is entered as soon as synchronization codewords are seen at the beginning of each batch.

The decoder handles loss of synchronization in three steps:

1. If the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This **data fail** mode is signalled in the message output when an address codeword was received, as shown in Table 4.
2. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the **fade recovery** mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended.
3. If it fails to re-synchronize in the 'fade recovery' mode, the **carrier off** mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In 'data receive' mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame.

On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Table 2 Call termination on error

SPF12	SPF13	CALL TERMINATION EVENT
0	X[1]	Any two consecutive codewords or the codeword directly following the address codeword uncorrectable.
1	0	Any single codeword uncorrectable.
1	1	Any two consecutive codewords uncorrectable.

Note

1. X = don't care.

7.5 Generation of output signals

The PCF5001 provides output indications for call alert, repeat mode alert, out of range alert, battery-low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM.

Table 3 shows the outputs which are used for special output indications, if the decoder operates in ON status.

Remark: reception of special SILENT override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 3 Output signals

ALERT FUNCTION	OUTPUT ACTIVE(1)					
	AL	AH	OL	OM	OR	BL
Start-up	(yes)	–	yes	yes	–	–
Status indication	yes	–	–	–	–	–
Call reception	(yes)	(yes)	yes	SPF11	–	–
Repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
Out-of-range	–	–	SPF15	–	yes	–
Battery-low	(yes)	(yes)	–	–	–	yes
Alarm input	(yes)	(yes)	yes	–	–	–

Note

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

7.6 Alerter

The PCF5001 provides the AL and AH outputs for acoustical LOW-level and HIGH-level signalling. LOW-level alerting is provided by the AL output only. For HIGH-level alerting both, AL and AH are active in anti-phase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001 generates call alert cadences. The first four seconds are generated at LOW-level, a further twelve seconds are generated at HIGH-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.8. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.9.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

ON status interrogation by the status request and reset input (SR) the PCF5001 generates a status cadence at LOW-level, in accordance with the present internal decoder status (see Fig.10).

When detecting a battery-low condition the PCF5001 provides a battery-low indication. Operating in ON status causes generation of a battery-low alert at HIGH-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or 'repeat' mode the battery-low alert is stored and inhibited until switching to ON status.

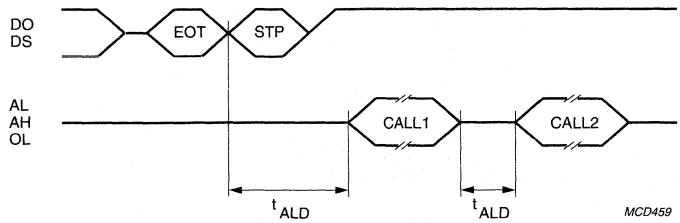


Fig.8 Call alert delay.

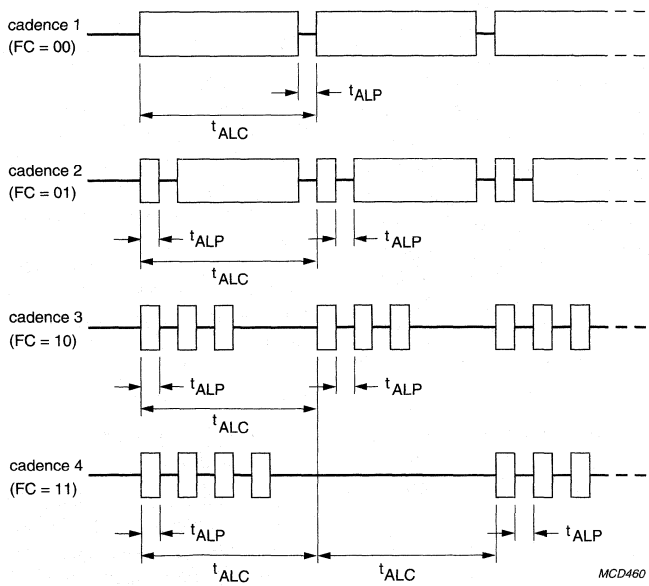


Fig.9 Call alert cadences.

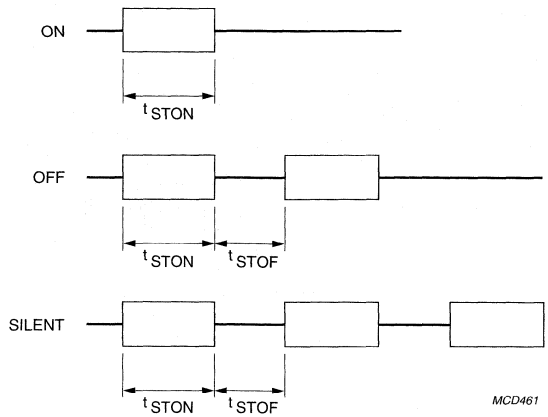


Fig.10 Status indication cadences.

7.7 Silent call storage and repeat mode

When programmed for alert only pager the PCF5001 provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter **repeat** mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time-out by expiration of a sixteen second alert operation causes the 'repeat' mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When 'repeat' mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When SILENT override calls are received, which entered the 'repeat' mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the 'repeat' mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever 'repeat' mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at HIGH-level and warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.11. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for 'display pager' mode.

7.8 Duplicate Call Suppression

The PCF5001 provides a Duplicate Call Suppression with time-out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001 inhibits any duplicate call alert in 'alert-only pager' mode.
In 'display pager' mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time-out is selectable by programming of SPF06 and SPF07.

7.9 LED indicator

The PCF5001 provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time-out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.12.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

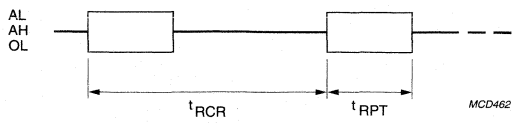


Fig.11 Repeat alert cadence.

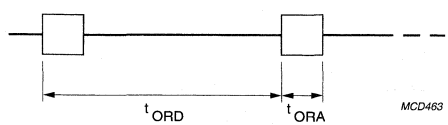


Fig.12 Out-of-range indication.

7.10 Vibrator output

The PCF5001 provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). SILENT override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

7.11 Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001 provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at LOW-level and on the LED output OL (see Fig.13).

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

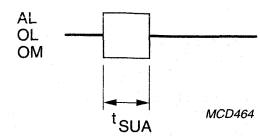


Fig.13 Start-up alert.

7.12 Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.14.

Upon interrogation the PCF5001 is also able to transfer EEPROM contents via the serial communication interface, see Section 7.21.

7.13 Message data transfer

The transfer of message data via DO and DS is organized in 8-bit words providing additional start and stop conditions as shown in Fig.15.

On reception of a valid call address the PCF5001 generates a start condition and outputs an address word as shown in Fig.15a.

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bits/s with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.15c.

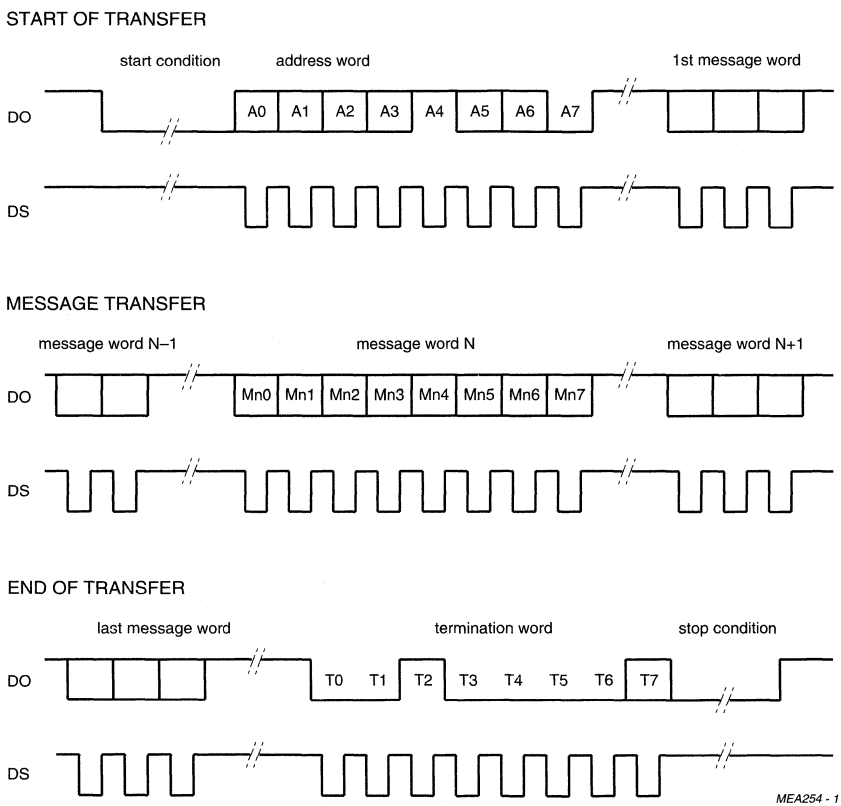
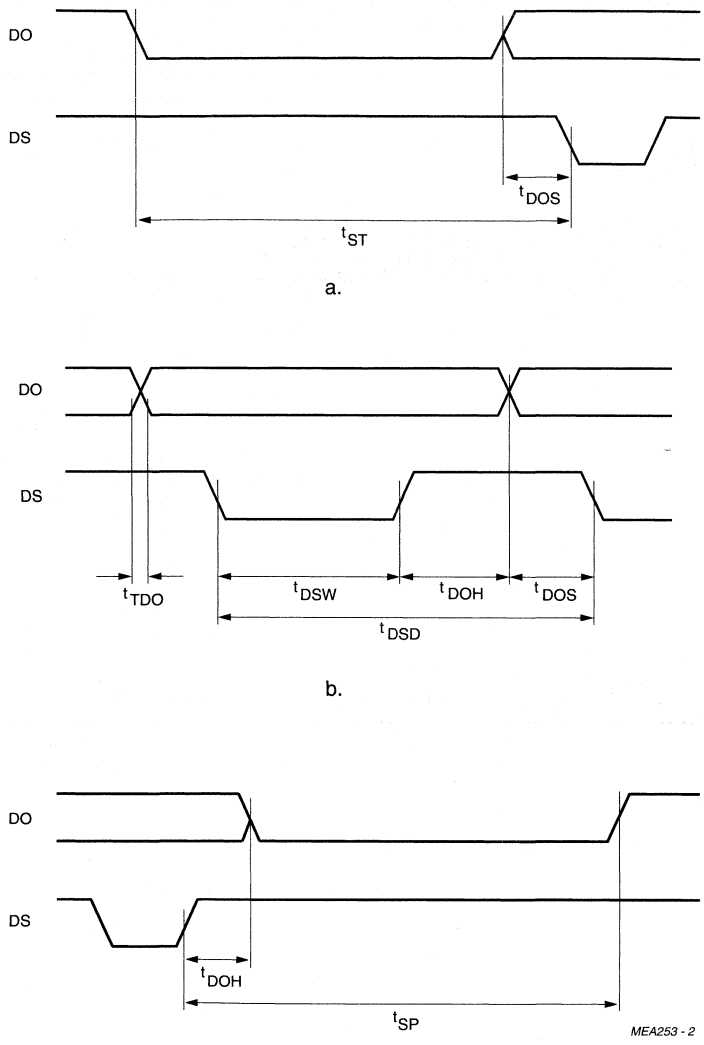


Fig.14 Call data transfer on the serial communication interface.



a. Start condition.
b. Data bit.
c. Stop condition.

Fig.15 Serial communication interface timing.

7.14 Call Data output on LED

When enabled by programming of SPF17 = 1, message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.16. No alert signals will appear on OL during message data transfer. Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

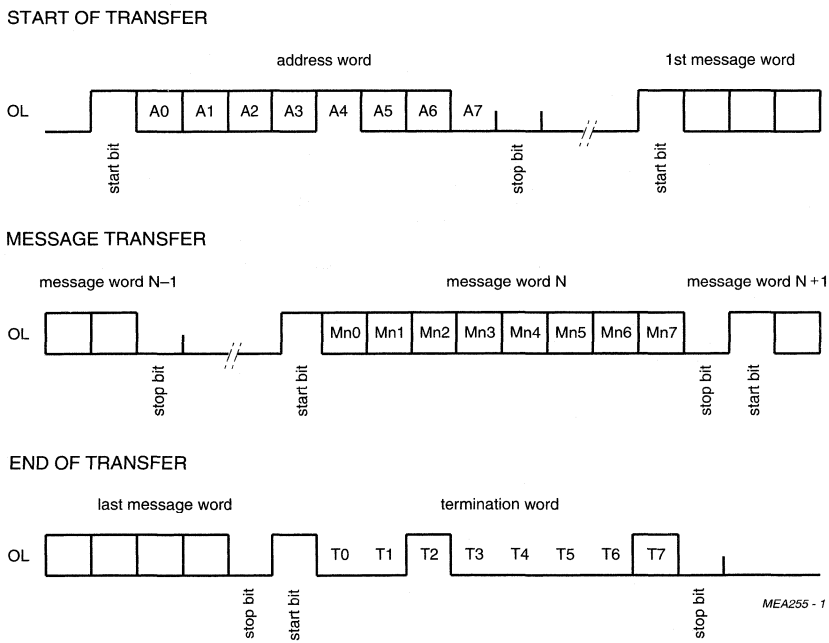


Fig.16 Call data transfer on the LED output.

7.15 Serial communication call data format

Table 4 Address word format

FUNCTION CODE		CALL ADDRESS			BIT 4	SYNC STATUS	DUPLEX CALL	BIT 7
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC		BIT 5	BIT 6	
Bit 21 of address codeword	bit 20 of address codeword	0	0	A	1	0 = Data Receive; 1 = Data fail	1 = Duplex Call time-out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
LSB			message bits			MSB	error flag

Note

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
0	0	1	0	0	0	0	error flag

Note

1. Bit 7 = 1, if call termination on error.

7.16 Data conversion

The PCF5001 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion

SPF13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	X[1]	X[1]	numeric
1	0	0	numeric
1	X[1]	1	alphanumeric
1	1	X[1]	alphanumeric

Note

1. X = don't care.

Table 8 Numeric format to ASCII conversion

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	'0'	0	0	0	0	1	1	0
1	0	0	0	'1'	1	0	0	0	1	1	0
0	1	0	0	'2'	0	1	0	0	1	1	0
1	1	0	0	'3'	1	1	0	0	1	1	0
0	0	1	0	'4'	0	0	1	0	1	1	0
1	0	1	0	'5'	1	0	1	0	1	1	0
0	1	1	0	'6'	0	1	1	0	1	1	0
1	1	1	0	'7'	1	1	1	0	1	1	0
0	0	0	1	'8'	0	0	0	1	1	1	0
1	0	0	1	'9'	1	0	0	1	1	1	0
0	1	0	1	'*'	0	1	0	1	0	1	0
1	1	0	1	'U'	1	0	1	0	1	0	1
0	0	1	1	' '	0	0	0	0	0	1	0
1	0	1	1	'–'	1	0	1	1	0	1	0
0	1	1	1	']'	1	0	1	1	1	0	1
1	1	1	1	'['	1	1	0	1	1	0	0

7.17 Memory Organization

The PCF5001 POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration.
The EEPROM is organized as three arrays of 38 bits each as shown in Fig.17.

A user address (or RIC) in POCSAG code comprises of 21 bits, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. In the PCF5001, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11 and FR12), addresses C and D reside in frame FR2 (FR20, FR21 and FR22). Figure 18 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{ENA}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{ENB}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{ENC}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{END}$

EEPROM ARRAY 3

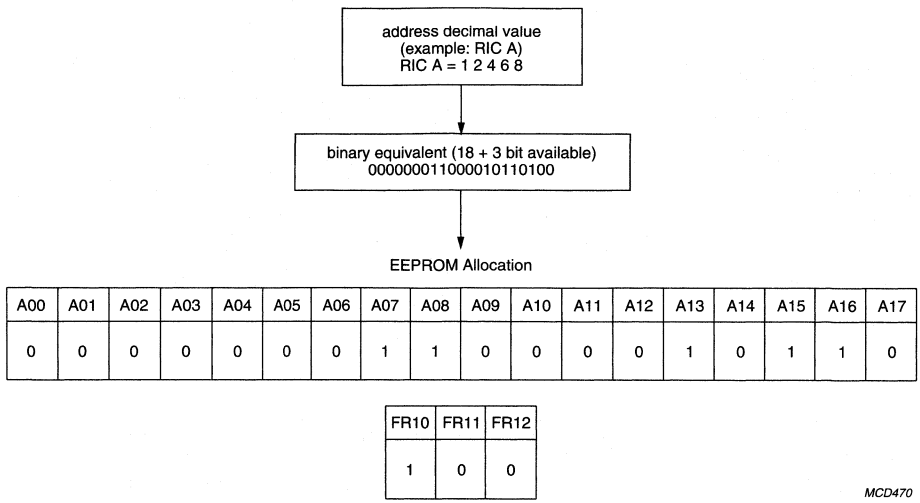
BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

MCD469

A00 represents the MSB of RIC A, B00 is the MSB of RIC C, etc.
FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.17 EEPROM memory organization.



A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.18 Decimal address to memory contents conversion example.

7.18 Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits

SPF	BIT	FUNCTION
SPF01	0	Alert-only pager mode.
	1	Display pager mode.
SPF02	0	512 bits/s data rate.
	1	1200 bits/s data rate, possible with 76.8 kHz crystal only.
SPF03	0	32768 Hz crystal configuration.
	1	76800 Hz crystal configuration.
SPF04, SPF05		Receiver establishment time (depending on data rate).
	00	7.8 ms/512 bits/s; 53.3 ms/1200 bits/s.
	01	15.6 ms/512 bits/s; 6.7 ms/1200 bits/s.
	10	31.3 ms/512 bits/s; 13.3 ms/1200 bits/s.
	11	62.5 ms/512 bits/s; 26.7 ms/1200 bits/s.

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time-out and out-of-range hold-off time-out.
	00	30 s.
	01	60 s.
	10	120 s.
	11	240 s.
SPF08	0	Voltage converter disabled, if SPF01 = 1 ('display pager' mode).
	1	Voltage converter enabled, if SPF01 = 1 ('display pager' mode).
SPF09	0	SILENT override on address C disabled.
	1	SILENT override on address C enabled.
SPF10	0	SILENT override on address D disabled.
	1	SILENT override on address D enabled.
SPF11	0	Vibrator output disabled.
	1	Vibrator output enabled.
SPF12	0	Call termination criteria combination method (note 1).
	1	Call termination criteria defined by SPF13.
SPF13	0	Numeric data deformatting, call termination on first uncorrectable codeword.
	1	Numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords.
SPF14	0	Duplicate call suppression disabled.
	1	Duplicate call suppression enabled.
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting.
	1	Out of range indication at OL output enabled, hold-off period is according to SPF06 and SPF07 setting.
SPF16	0	Repeat alert disabled.
	1	Repeat alert enabled.
SPF17	0	Call data output on OL disabled.
	1	Call data output on OL enabled.
SPF18	–	Spare.
SPF19	–	Program always 0.
SPF20 to SPF30	–	Spares.
SPF31	0	Alerter frequency 2048 Hz.
	1	Alerter frequency 2731 Hz.
SPF32	0	Frequency reference output 16384 Hz if SPF01 = 1 ('display pager' mode).
	1	Frequency reference output 32768 Hz if SPF01 = 1 ('display pager' mode).

Note

1. Call termination on:
   a) First codeword immediately following address codeword uncorrectable.
   b) Two consecutive codewords uncorrectable.

7.19 EEPROM Write operation

The **program** mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The 'program' mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The 'program' mode has to be left after programming of each array.

After entering the 'program' mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.19 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}. During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{ref} must not be exceeded. When the on-chip voltage converter is enabled a voltage regulator diode or a damping resistor of sufficiently low impedance has to be connected between V_{ref} and V_{SS} to limit the voltage level at V_{ref} during program operation.

7.20 EEPROM Read operation

After entrance to the 'program' mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.19 for timing during an EEPROM read operation.

7.21 Read-back operation via Microcontroller Interface

In 'display pager' mode, the PCF5001 is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is started by a logic HIGH level on SR. The HIGH level on SR must be removed before the end of the tenth output byte, otherwise the transfer is aborted and restarted. The minimum pulse duration corresponds with t_{SPD} in the status interrogation timing (see Fig.7). The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW-level on DS as shown in Fig.20.

During EEPROM Read-back operation, the PCF5001 configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001 will re-enter the programmed configuration.

7.22 Voltage converter

The PCF5001 contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 µF is connected to V_{ref} as shown in Fig.23. The voltage converter operates in 'display pager' mode only, when enabled by programming SPF08 (see Table 9).

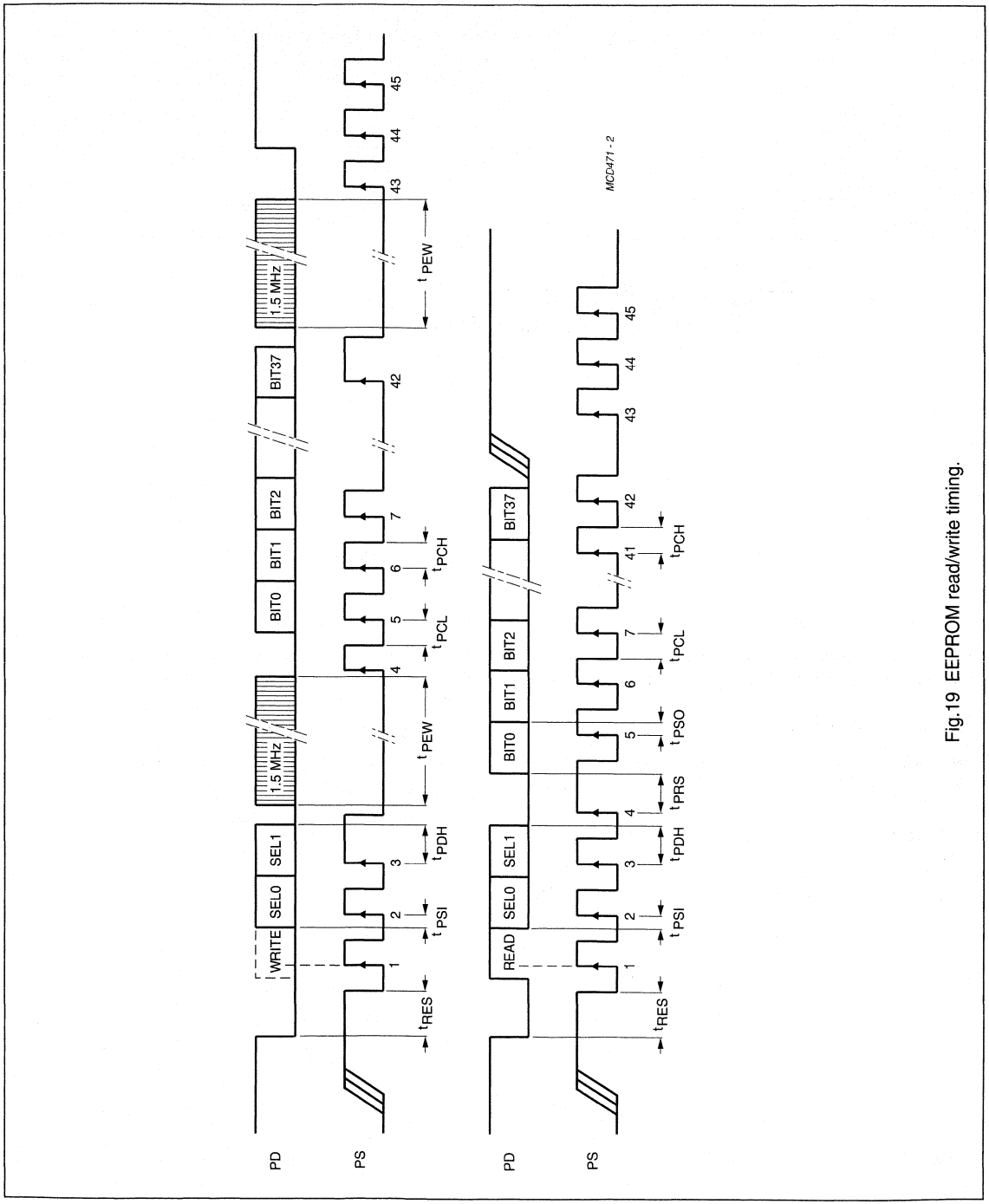


Fig.19 EEPROM read/write timing.

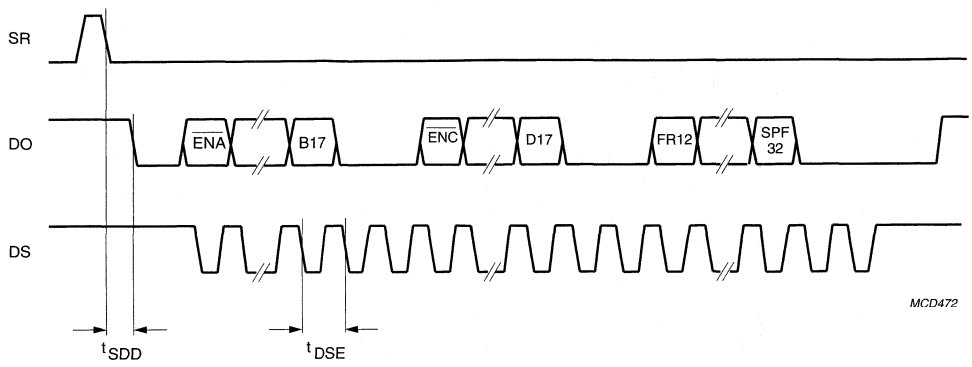


Fig.20 EEPROM data transfer to microcontroller timing.

7.23 Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

7.23.1 Board test mode

'Board test' mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH
2. Output AL is activated by a LOW-level on ON input
3. Output AH is activated by a HIGH-level on SR input
4. Outputs OL and OM are activated by a HIGH-level on SK input.

Exit from 'board test' mode is achieved by setting input PD HIGH.

7.23.2 Pager Test Mode (Type Approval Mode)

'Pager test' mode is entered by reception of a valid call while 'board test' mode is active, see above. In 'pager test' mode:

1. Call alert cadences are terminated after 2 seconds
2. Duplicate call suppression is disabled.

Exit from 'pager test' mode is achieved by disconnecting the power supply from the decoder.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	note 1	+0.5	−8.0	V
V_{PG}	programming supply voltage		−5.5	−	V
V_n	voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE		+0.8	V_{ref} − 0.8	V
V_{n1}	input voltage on any other pin		+0.8	V_{SS} − 0.8	V
P_{tot}	total power dissipation		−	250	mW
P_O	power dissipation per output		−	100	mW
$I_{I(max)}$	maximum input current (any input)		−	10	mA
$I_{O(max)}$	maximum output current				
	any output except AL		−	20	mA
	output AL		−	70	mA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. V_{DD} is connected to the substrate (see Fig.1), and is referred to as common, 0 V.

9 DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{ref} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Alert-only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage	voltage converter disabled; all outputs open-circuit				
		T_{amb} = −10 to +85 °C	−1.5	−2.7	−6.0	V
		T_{amb} = −40 to +85 °C	−1.8	−2.7	−6.0	V
I_{SS}	supply current	note 1	−	−60	−100	µA
V_{PG}	programming supply voltage	note 2	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		−	−500	−	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		$0.7V_{SS}$	–	–	V
V_{IL2}	LOW level input voltage AI, ON, SR, SK and IE		$0.7V_{ref}$	–	–	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		–	–	$0.3V_{SS}$	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		–	–	$0.3V_{ref}$	V
I_I	input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	µA
	PD	$V_I = V_{SS}$	–9.0	–	–24.0	µA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	µA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	µA
	ON and SK	$V_I = V_{SS}$	–0.5	–0.8	–1.1	µA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	µA
C_i	input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	$V_{OL} = -1.35$ V	100	–	–	µA
	DO, DS, BL, FL and OR	$V_{OL} = -1.35$ V	100	–	–	µA
	AL	$V_{OL} = -1.5$ V	17.5	–	–	mA
	RE	$V_{OL} = 2.2$ V	200	–	–	µA
I_{OH}	HIGH level output current					
	OL, OM and AH	$V_{OH} = -1.35$ V	–0.8	–	–1.8	mA
	DO, DS, BL, FL and OR	$V_{OH} = -1.35$ V	–100	–	–	µA
	AL	AL high-impedance	–	–	–0.2	µA
	RE	$V_{OH} = -0.5$ V	–1.0	–	–	mA
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
g_m	oscillator transconductance	$V_{SS} = -1.5$ V	15	29	43	µS
		$V_{SS} = -6.0$ V	25	39	55	µS
V_{PU}	power-up reset threshold voltage		–	–1.2	–	V

Notes

1. All inputs = V_{SS}; voltage converter off; all outputs open-circuit.
2. See Section 7.19 and Chapter 8 for limitations of V_{ref} when programming while the voltage converter is enabled.

10 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 0 V; V_{SS} = −3.0 V; V_{ref} = −6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_S = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		−1.5	–	−3.0	V
Voltage converter						
$V_{ref(0)}$	output voltage; no load	V_{SS} = −3.0 V	−5.8	–	−6.0	V
V_{ref}	output voltage	V_{SS} = −2.0 V; I_{ref} = 250 µA	−3.0	−3.5	–	V
I_{ref}	output current	V_{SS} = −2.0 V; V_{ref} = −2.7 V	400	600	–	µA
		V_{SS} = −3.0 V; V_{ref} = −4.5 V	600	900	–	µA
Inputs						
I_I	input current					
	AI, ON, SR and SK	$V_I = V_{ref}$	–	0	−0.5	µA
	ON and SK	$V_I = V_{DD}$	–	0	±0.5	µA
	SR	$V_I = V_{DD}$; V_{ref} = −6.0 V	–	17	–	µA

11 AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Alert frequency						
f_{AL}	alert frequency	SPF31 = 0	–	2048	–	Hz
f_{AWH}	high alert warble frequency		–	1024	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{AL}	alert frequency	SPF31 = 1	–	2731	–	Hz
f_{AWH}	high alert warble frequency		–	1365	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{FL}	output frequency reference at FL	SPF32 = 0	–	16384	–	Hz
		SPF32 = 1	–	32768	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Call alert duration						
t_{ALT}	time-out period		–	16	–	s
t_{ALL}	alert time LOW (AL output only)		–	4	–	s
t_{ALH}	alert time HIGH (AH and AL outputs)		–	12	–	s
t_{ALC}	call alert cycle time	see Fig.9	–	1	–	s
t_{ALP}	call alert pulse duration	see Fig.9	–	125	–	ms
t_{ALD}	call alert hold off period	see Fig.8	52	–	–	ms
t_{RPT}	repeat alert duration	see Fig.11	–	–	4	s
t_{RCR}	repeat alert recurrence time	see Fig.11	–	–	15	s
t_{RCP}	repeat alert cycle time		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert time	see Fig.10	–	–	62.5	ms
t_{STOF}	status alert delay	see Fig.10	–	–	62.5	ms
t_{SUA}	start-up alert time	SPF02 = 0; see Fig.13	–	–	500	ms
		SPF02 = 1; see Fig.13	–	–	453	ms
t_{ORA}	out-of-range alert pulse width	see Fig.12	–	–	62.5	ms
t_{ORD}	out-of-range alert time	see Fig.12	–	–	2	s
t_{BLAL}	battery LOW-level alert time		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bits/s
t_{DSD}	strobe period call data	see Fig.15	480	–	495	µs
t_{DSE}	strobe period EEPROM data	see Fig.20	200	488	1150	µs
t_{DSW}	data strobe pulse width	see Fig.15	230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF; see Fig.15	–	–	100	ns
t_{DOS}	data output set-up time	see Fig.15	–	–	135	µs
t_{DOH}	data output hold time	see Fig.15	115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bits/s numeric message	3420	–	–	µs
t_{ST}	start condition set-up time	see Fig.15	4750	–	–	µs
t_{SP}	stop condition set-up time	see Fig.15	595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay	see Fig.20	1	–	10	ms

12 TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{osc}	oscillator frequency	SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time	see Fig.21	–	–	100	µs
t_{DI1}	data input logic 1	see Fig.21	t_{BIT}	–	∞	
t_{DI0}	data input logic 0	see Fig.21	t_{BIT}	–	∞	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bits/s
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{osc} = 76800 Hz	–	1200	–	bits/s
t_{BIT}	bit period		–	833.3	–	ms
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms
Display pager mode (SPF01 = 1); see Figs 6 and 7						
t_{STP}	status set-up time	f_{osc} = 32768 Hz	35	–	–	µs
t_{STD}	status change delay		–	–	35	µs
t_{IEH}	interface enable hold time		35	–	–	µs
t_{STH}	status hold time		35	–	–	µs
t_{SPD}	status pulse duration		35	–	–	µs
t_{STP}	status set-up time	f_{osc} = 76800 Hz	15	–	–	µs
t_{STD}	status change delay		–	–	15	µs
t_{IEH}	interface enable hold time		15	–	–	µs
t_{STH}	status hold time		15	–	–	µs
t_{SPD}	status pulse duration		15	–	–	µs

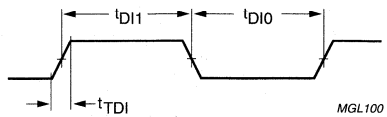


Fig.21 Data input timing.

13 PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = −5.0 V (see notes 1, 2 and 3); V_{ref} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming; see Fig.19						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
t_{EW}	erase/write cycles		1000	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	years
t_{PCH}	data clock HIGH time	note 4	65	–	–	µs
t_{PCL}	data clock LOW time	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.19), otherwise $V_{SS(min)}$ = −1.5 V.
2. Maximum voltage for programming (V_{PG}) is −5.5 V.
3. See Section 7.19 and Chapter 8 for limitations of V_{ref} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

14 APPLICATION INFORMATION

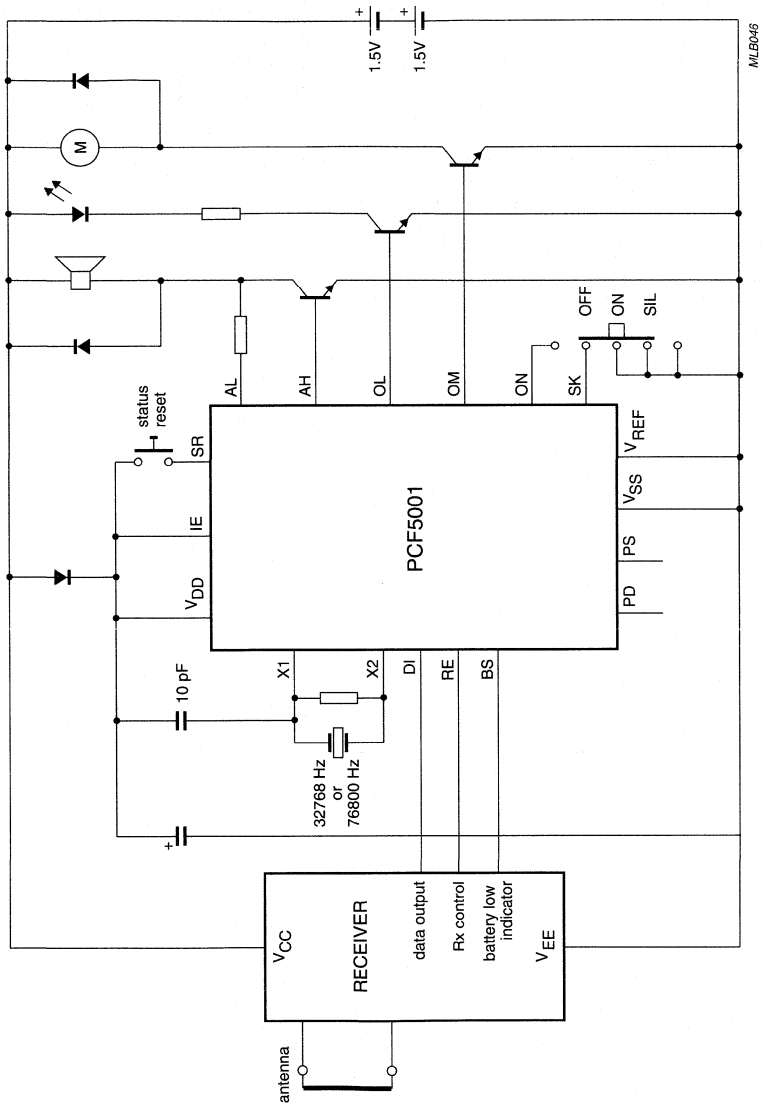


Fig.22 Alert-only pager application example.

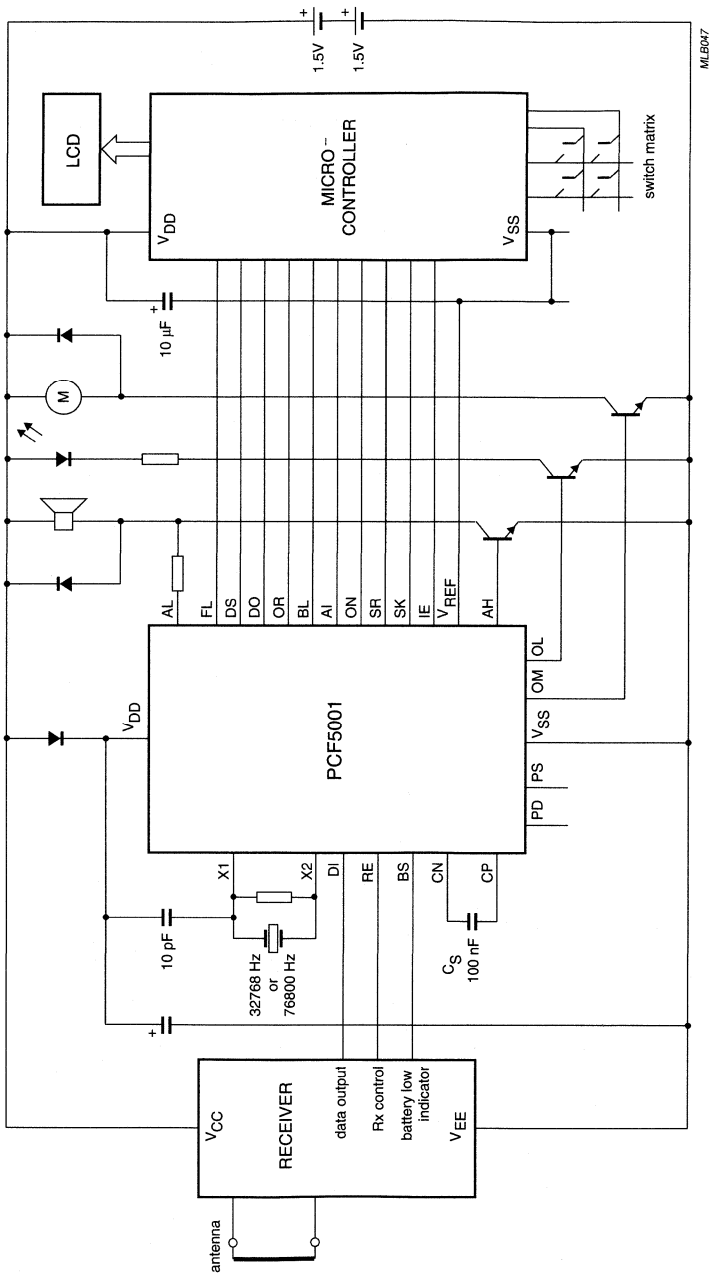


Fig.23 Display-pager application example.

Power amplifier controller for GSM and PCN systems

PCF5077T

FEATURES

- CMOS low-voltage, low-power
- Can be used in burst mode with power-down
- 3-wire serial bus interface with the bus available in Power-down mode
- On-chip ramp generator for 256 different power levels with two dynamic ranges
- Two programmable regulator start conditions (V_{KICK} and V_{HOME})
- Programmable analog output voltage limitation
- Ramping speed depending on the 13 MHz system frequency clock for Global System for Mobile communications (GSM) and Personal Communications Network (PCN)
- Low swing input buffer for the 13 MHz master clock
- Compatible to a large number of different RF power modules
- Programmable temperature matching
- Dual supply concept for analog and digital part
- No external filter for suppression of clock pulse feed through
- Direct power control with ramping function (control loop can be switched off)
- On-chip Power-on reset for all registers
- Serial bus is compatible to bus systems independent of additional clock pulse after rising edge of strobe signal
- Low operating current consumption
- TTL compatible interface
- Programmable gain factor for sensor signal at OP1
- Two different voltages for 1 LSB of the burst power Digital-to-Analog Converter (DAC) are programmable.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1	note 1	2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2 (for OP4)		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	note 2	–	9	18	mA
T_{amb}	operating ambient temperature		−40	–	+85	°C

Notes

1. The voltages V_{DDA1} and V_{DDD} must be equal and V_{DDA2} must be either equal or greater than $V_{DDA1} = V_{DDD}$.
2. $V_{DDA1} = V_{DDD} = 3$ V and $V_{DDA2} = 5$ V. The V_{DD} pins are: V_{DDA1}, V_{DDA2} and V_{DDD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5077T	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

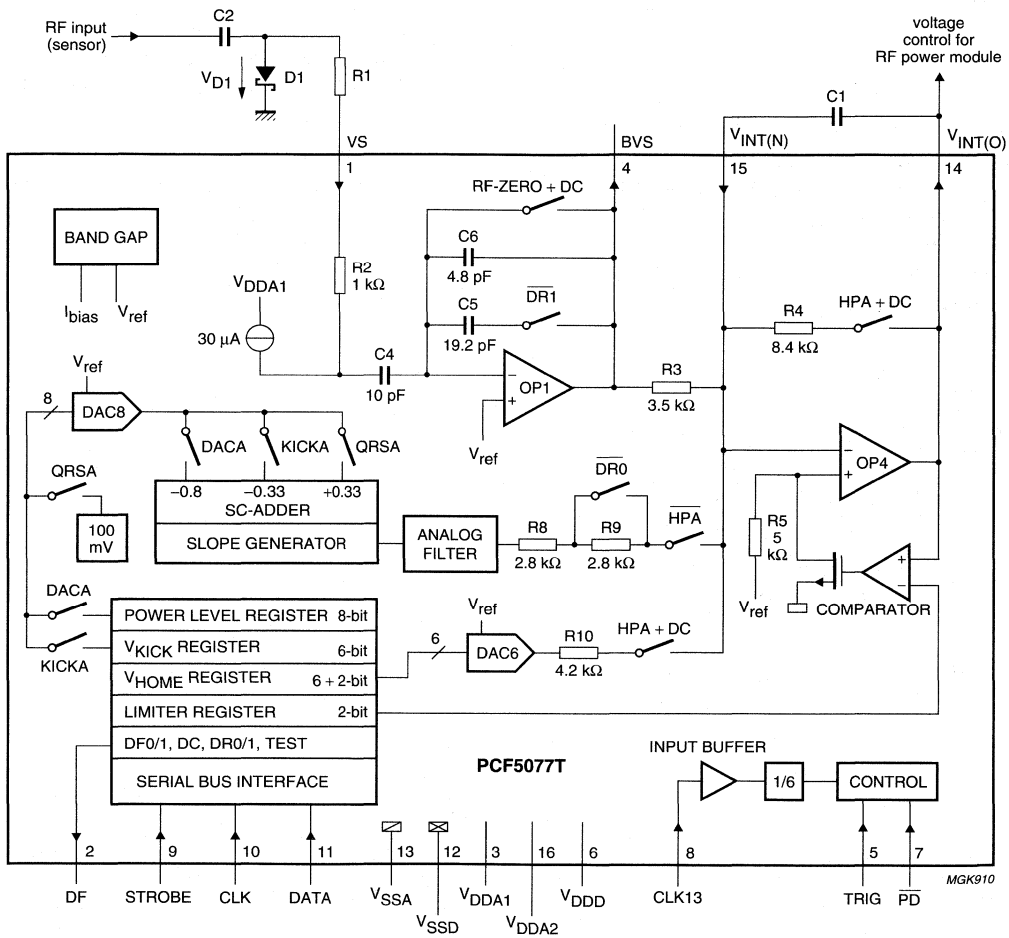


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VS	1	sensor signal input
DF	2	programmable 3-state output
V_{DDA1}	3	analog supply voltage 1
BVS	4	buffered sensor signal output
TRIG	5	trigger signal input
V_{DDD}	6	digital supply voltage
$\overline{PD}$	7	power-down input (active LOW)
CLK13	8	13 MHz master clock input (low-swing)
STROBE	9	serial bus strobe signal input
CLK	10	serial bus clock signal input
DATA	11	serial bus data signal input
V_{SSD}	12	digital ground
V_{SSA}	13	analog ground
$V_{INT(O)}$	14	integrator output
$V_{INT(N)}$	15	integrator inverting input
V_{DDA2}	16	analog supply voltage 2 (for OP4)

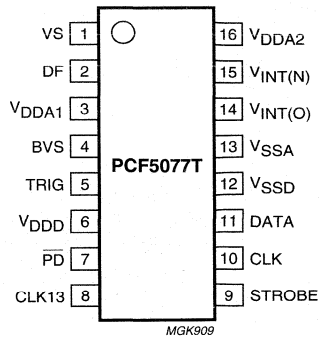


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

This CMOS device integrates operational amplifiers, two digital-to-analog converters and a serial bus interface to implement an 'Integrating-Controller' (see Fig.1). It is designed to control both the power level and the up- and down-ramping of GSM/PCN transmit bursts.

The GSM/PCN power-up and power-down ramping curves are generated on-chip, using an internal clock frequency of 2.166 MHz $\left(T_{cy} = \frac{1}{f_{clk}}\right)$, that is generated internally by dividing the external 13 MHz clock signal by six.

Generally, the power amplifier is ramped-up after a rising edge on pin TRIG and ramped-down after a falling edge.

The content of the power level register (bits PL7 to PL0) determines which of the 2×256 possible values the top of the burst will have.

To match the controller to different power modules and sensors several parameters must be adapted.
The following parameters influence the performance of the transmission system:

- The external capacitor C1 in Fig.1 determines the maximum bandwidth of the power control loop, depending on the highest steepness of the control curve of the power module and on the sensor attenuation.
- The maximum output voltage at pin $V_{INT(O)}$ to protect the power module: the limiting value of $V_{INT(O)}$ can be set to 4, 3.3 or 2.55 V, depending on the contents of the limiter register (bits Lim1 and Lim0). This limiting results in a ringing at $V_{INT(O)}$ (typ. 200 mV peak-to-peak value) but it will not be transferred to the antenna because the power module is in saturation. The limiter register bits Lim1 and Lim0 can be used to switch off the limiter option (see Table 5).
- The home position at $V_{INT(O)}$: the integrator output voltage at home position ($\overline{PD}$ = HIGH and TRIG = LOW) is programmed by means of the V_{HOME} register. Bits Vh5 to Vh0 are fed into a 6-bit DAC that generates a part of V_{HOME}.
- The temperature behaviour of the home position: bits DVh1 and DVh0 can be used to compensate temperature dependencies (–2 or –4 mV/K) of the control curves of the power module. This completes the setting of V_{HOME}.
- The KICK voltage: the 6 bits of the V_{KICK} register (Vk5 to Vk0) determine the differential integrator input voltage just after a ramp-up starting signal is detected.

The register information is written via a 3-wire serial bus (see Sections "Serial bus programming" and "Data format").

The output of pin DF is for general purpose which can have three different states (LOW, HIGH and 3-state), depending on the values of bits DF0 and DF1 in the serial register.

Dual supply pins are provided for the analog and digital blocks.

Reset function

After switching on the power supply, the on-chip reset is active for maximal 50 µs when the rising slope of V_{DDD} has reached 1.5 ±0.4 V. During this reset, all controllers are set to the home position and the registers are set to their default values. If the supply voltage drops below the reset threshold a constant reset will appear.

Operating conditions

$\overline{PD}$ = LOW

The serial bus interface is operating, e.g. all registers can be programmed but no effect will be seen on any pin. The contents of the registers are passed to the rest of the circuit only during power-up and with the 13 MHz master clock applied.

If the low-swing input buffer at pin CLK13 is switched off, neither the SC-adder nor the slope generator will function. This means that after the chip is powered-up, the outputs have to settle again to the programmed register values. The settling time is dominated by the slow power-up of the band gap of typically 50 µs.

When the chip is used in the burst mode, it is important to switch on the PCF5077T before the power module or the RF power. Otherwise it is possible that a positive spike at $V_{INT(O)}$ will open the power module.

A safe value is t_{ON} = 200 µs between the switching on of the PCF5077T and the switching on of the power module respectively the next TRIG (see Fig.3).

$\overline{PD}$ = HIGH

The whole chip is active. CLK13 clocks the internal state machine as well as the SC-adder and slope generator. Every change at TRIG is recognized if the master clock is running. The contents of the serial bus registers are processed. If the master clock is switched off during power-up, the state machine is stopped and the output of the SC-adder and slope generator becomes undefined. Nevertheless, by reactivating the master clock, the output of the SC-adder and slope generator will settle to the old values again.

The analog integrating controller

The analog integrating controller consists of two operational amplifiers (OP1 and OP4) and a comparator. OP1 amplifies the sensor signal and OP4 is used to form a differential integrator. The comparator is used to limit the integrator output voltage to the value selected by bits Lim1 and Lim0 in the limiter register.

A (Schottky) diode D1 as external rectifier is connected to pin VS. The SC-adder block generates the voltage for the ramping of the power module.The differential integrator integrates the difference of this voltage and the voltage detected at the diode. The integrator output voltage $V_{INT(O)}$ is used to control the power amplifier module.

Table 1 Definition of some voltages used in Figs 1 and 3

SYMBOL	DESCRIPTION
V_{ref}	reference voltage, typically 1.25 V
V_{D1}	voltage over the sensor diode D1
V_{PL}	voltage determining the power level; it is generated in the Switched Capacitor (SC)-adder block if switch DACA is closed (i.e. if the signal DACA is HIGH)
V_{VS}	voltage at pin VS when RF is rectified by the sensor diode D1
V_{BVS}	amplified voltage from pin VS
V_{KICK}	voltage determining the kick level; it is generated in the SC-adder block if switch KICKA is closed (i.e. if the signal KICKA is HIGH)
V_{HOME}	voltage determining the home position voltage; if HPA signal is active, the output of DAC6 plus temperature compensation is amplified and appears at the output of OP4 (pin $V_{INT(O)}$)
V_{QRS}	low voltage at the output of the SC-adder block which causes a ramp-down with a shortened tail if switch QRSA is closed (i.e. if the signal QRSA is HIGH)
V_{RFIN}	input signal to the power amplifier

Ramp generation (see Fig.3)

The circuit is activated with the $\overline{PD}$ signal going HIGH before time mask AS and deactivated after ramping down, e.g. at time GS to HS. For this usual 'power-down burst mode' application in GSM/PCN mobile stations, the RF input power at the power module must be activated between time AS and BS (when the home position at $V_{INT(O)}$ has already reached its stable value) and deactivated between time GS and HS. This is necessary for many types of power modules to meet the −70 dB margin.

A ramp-up is started by a rising edge of the TRIG signal. The TRIG signal and all other internal signals are delayed by two clock periods ($2T_{cy}$) with respect to the signal at pin TRIG.

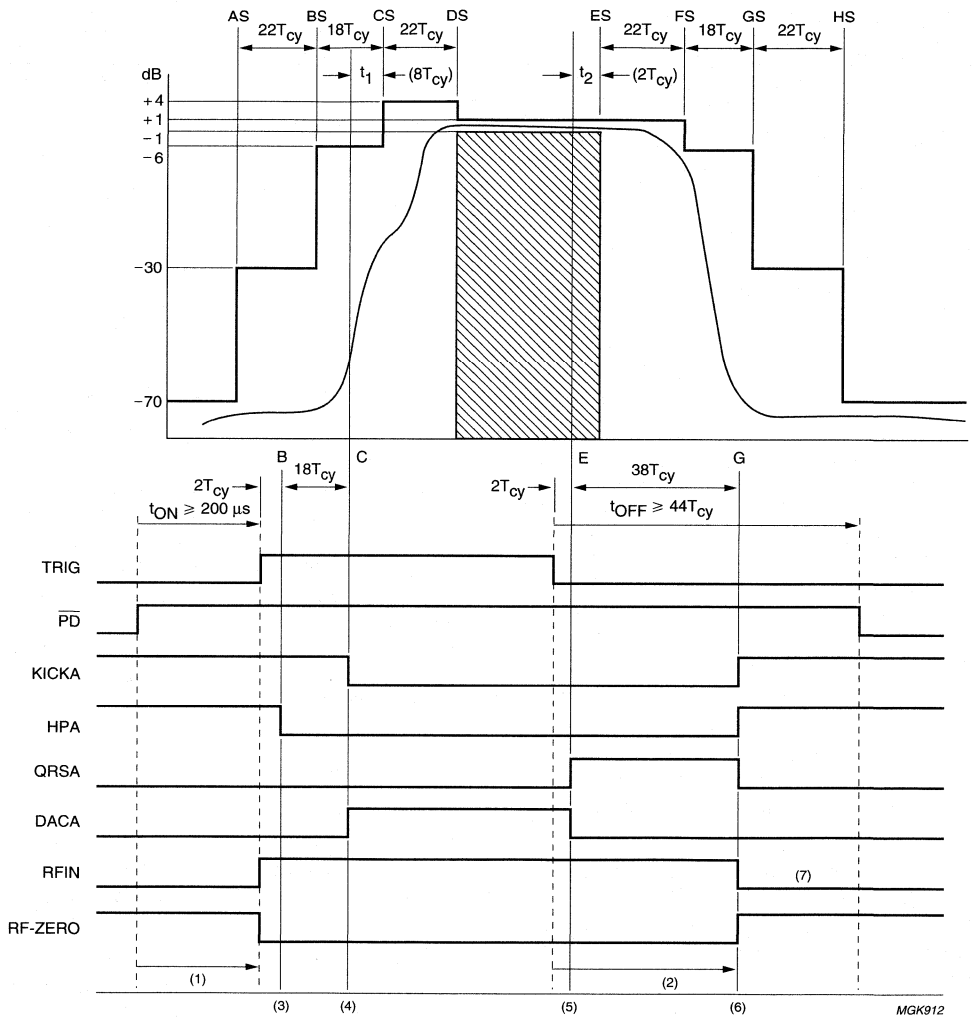
The timing diagram shows a possible relationship between the chip timing (time B to G) relative to the GSM-mask (AS to HS). However, the user is free to choose the rising and falling edge of TRIG independently so that the mask is not violated.

DESCRIPTION OF THE SIGNALS STARTING AT A STABLE HOME POSITION OF $V_{INT(O)}$ AT TIME B − $2T_{cy}$

The integrator output voltage is regulated to the value defined in the V_{HOME} register. The output of the slope generator is connected to the negative input $V_{INT(N)}$ of operational amplifier OP4 (V_{KICK} is defined by bits Vk5 to Vk0 in the V_{KICK} register). Two clock periods after a rising edge on pin TRIG, the integrator start condition circuitry is turned off and OP4 is switched into an integrator configuration (time B). The HPA switches will open (HPA + DC is either HPA switch or DC bit). Switch $\overline{HPA}$ is closed when there is no home position. Due to the negative differential input voltage V_{KICK}, the integrator output will start to rise. After $18T_{cy}$ (time C) the output of DAC8 is connected to the SC-adder and slope generator block. The input of the 8-bit DAC comes from bits PL7 to PL0 in the power level register. The slope generator will generate a smooth curve between the former and the new output value of the SC-adder block. The power amplifier is ramped-up via the integrator in approximately $22T_{cy}$.

This condition is stable as long as TRIG remains HIGH. Two clock periods after a falling edge at TRIG the ramp-down is started (time E). The SC-adder output voltage will change to V_{QRS} (−100 mV), because DACA becomes inactive and QRSA active. This causes a ramp-down with a shortened tail. The slope generator again generates a smooth curve between the new SC-adder output voltage and the old SC-adder output voltage.

The slope generator must have reached its final value at $38T_{cy}$ after the recognized falling edge of TRIG because the HPA signal is activated again and by that turning the integrator into its 'home position' (time G). The integrator output voltage will be regulated once more to the value defined in the V_{HOME} register.



(1) $t_{RFON} = t_{ON} - 12T_{cy}$ to $t_{ON} + 2T_{cy}$.
(2) $t_{RFOFF} = 44T_{cy}$ to $66T_{cy}$.
(3) V_{KICK} (start integrator) applied to integrator.
(4) V_{PL} applied to integrator.
(5) V_{QRS} applied to integrator.
(6) V_{HOME} at output of OP4.
(7) This timing of the RF input power (from the power module) ensures that the −70 dB margin is met, even if the isolation of the power module is bad.

Fig.3 Timing diagram of a typical ramp-up/ramp-down curve.

Serial bus programming

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires are DATA, CLK and STROBE. The data sent to the device is loaded in bursts framed by STROBE. Programming clock edges and their appropriate data bits are ignored until STROBE goes active LOW.

The last four address bits are decoded on the active STROBE edge. This produces an internal load pulse to store the data in one of the addressed registers. To avoid erroneous circuit operation, the STROBE pulse is not allowed during internal data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum STROBE pulse width after data transfer.

Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. The bus is also programmable during power-down.

Data format

Data is entered with the most significant bit (MSB) first. The leading 10 bits p15 to p6 are the data field, the following bits p5 and p4 form the subaddress, while the last 4 bits p3 to p0 are the device address field.
The PCF5077T uses only one of the available addresses. The format is given in Table 2.

The correspondence between data and address fields is given in Table 3 and the description in Table 4.

All three registers in Table 3 are set to 00H during reset.

Table 2 Programming register format

DATA BITS				SUBADDRESS		DEVICE ADDRESS			
MSB			LSB						
p15	p14 to p8	p7	p6	p5	p4	p3	p2	p1	p0
data9	data8 to data2	data1	data0	Sadd1	Sadd0	add3	add2	add1	add0

Table 3 Register bit allocation

DATA FIELD (D9 TO D0)										SUBADDRESS		DEVICE ADDRESS			
MSB									LSB						
p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
Vk5	Vk4	Vk3	Vk2	Vk1	Vk0	Lim1	Lim0	DC	Test	0	0	1	0	1	0
Vh5	Vh4	Vh3	Vh2	Vh1	Vh0	DVh1	DVh0	DR1	DR0	0	1	1	0	1	0
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DF1	DF0	1	1	1	0	1	0

Table 4 Description of bits used in Table 3

BITS	DESCRIPTION
Vk5 to Vk0	6 bits to control the kick voltage in 64 steps
Vh5 to Vh0	6 bits to control the home position voltage in 64 steps
PL7 to PL0	8 bits to control the power level in 256 steps
Lim1 and Lim0	2 bits to control the limiter voltage (see Table 5)
DC	direct control with ramping function (control loop is switched off when DC = 1)
Test	test mode (Test = 1); **must always be set to logic 0 in application**
DVh1 and DVh0	2 bits to set the temperature coefficient of V_{HOME} (see Table 6)
DR1	gain factor of OP1
DR0	gain factor for slope generator output
DF1	enable of the 3-state output on pin DF (for DF1 = 0, pin DF is in 3-state mode)
DF0	data output on pin DF

Table 5 Limiter voltage

Lim1	Lim0	LIMITER VOLTAGE (V)	TOLERANCE AT T_{amb} = 27 °C (mV)	TOLERANCE AT T_{amb} = 85 °C (mV)
0	0	limiter off	–	–
0	1	4.00	±250	±350
1	0	3.30	±250	±350
1	1	2.55	±250	±350

Table 6 Programmable temperature coefficient of V_{HOME}

DVh1	DVh0	V_{HOME}[1]
0	0	Vh ±0.4 mV/K
0	1	Vh – 2 mV/K ±20%
1	0	Vh – 4 mV/K ±20%
1	1	V_{SS}

Note

1. Vh = voltage programmed in V_{HOME} register bits Vh5 to Vh0 and generated by DAC6.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1	–0.5	+6.0[1]	V
V_{DDA2}	analog supply voltage 2	–0.5	+6.0[1]	V
V_{DDD}	digital supply voltage	–0.5	+6.0[1]	V
V_I	DC input voltage on all pins (except pin VS)	–0.5	V_{DD} + 0.5	V
$V_{I(VS)}$	DC input voltage on pin VS	–3.0	V_{DD} + 0.5	V
$I_{I(n)}$	DC input current on any signal pin	–10	+10	mA
P_{tot}	total power dissipation	–	83	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

Note

1. Pulses of 7 V are allowed for less than 100 ms.

OPERATING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and $V_{DDD} = V_{DD}$ = 2.7 to 6.0 V; $V_{DDD} = V_{DDA1} \leq V_{DDA2}$; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operational amplifier (OP1)						
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
GB	gain bandwidth product	V_{DDA1} = 3.0 V	2.0	–	–	MHz
G_{min}	minimum gain	DR1 = 0	–8.1	–7.6	–7.1	dB
G_{max}	maximum gain	DR1 = 1	5.9	6.4	6.9	dB
V_{offset}	offset voltage	no load at output	–20	0	+20	mV
Operational amplifier (OP4)						
V_{DDA2}	analog supply voltage 2		2.7	5.0	6[1]	V
GB	gain bandwidth product	C_L = 120 pF; V_{DDA2} = 5 V; note 2	4	–	–	MHz
PSRR	power supply rejection ratio	V_{DDA2} = 5 V, at 217 Hz	50[3]	55	–	dB
SR_{pos}	positive slew rate	V_{DDA2} = 5 V; note 4	3.5	15	–	V/µs
SR_{neg}	negative slew rate	V_{DDA2} = 5 V; note 4	3.5	6	–	V/µs
V_{offset}	voltage offset	no load at output	–20	0	+20	mV
$V_{o(min)}$	minimum output voltage		–	–	0.3	V
$V_{o(max)}$	maximum output voltage		$0.85V_{DDA2}$	–	–	V
I_o	output current	note 5	4.5	–	–	mA
Programmability and accuracy of V_{PL} (DAC8) at $V_{INT(O)}$						
INL	integral non-linearity		–	±1.5	±10	LSB
DNL	differential non-linearity		–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	–30	–	+60	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	2.72	–	3.15	V
STS	step size	DC = 1; DR0 = 1	–	6	–	mV
		DC = 1; DR0 = 0	–	11.7	–	mV
Programmability and accuracy of V_{KICK} (DAC8) at $V_{INT(O)}$						
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	–50	–	+50	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	270	–	400	mV
STS	step size	DC = 1; DR0 = 1	–	2.6	–	mV
		DC = 1; DR0 = 0	–	5.0	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programmability and accuracy of V_{HOME} (DAC6) at $V_{INT(O)}$						
INL	integral non-linearity	note 7	–	±1.0	±3	LSB
DNL	differential non-linearity	note 7	–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DVh1 = 0; DVh0 = 0	50	–	170	mV
$V_{o(max)}$	maximum output voltage	DVh1 = 0; DVh0 = 0	1.95	–	2.25	V
STS	step size		–	33	–	mV

Notes

1. Pulses of 7 V are allowed for less than 100 ms.
2. Minimum specified frequency at T_{amb} = 27 °C. For T_{amb} = 85 °C a typical value of 4 MHz is specified.
3. Not tested. Guaranteed by design.
4. Slew rates are measured between 10% and 90% of output voltage with a load of approximately 40 pF to ground.
5. Measured with R_L = 1.2 kΩ, C_L = 80 pF and V_{DDA2} = 5 V. The voltage drop at the output is less than 20 mV.
6. Referred to V_{HOME}; nominal operating condition, direct control (DC = 1), V_{HOME} programmed to 40.
7. The parameter is measured starting from code 4, due to a saturation effect for the first four codes.

DC CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = V_{DD} = 2.7 to 6.0 V; V_{DDD} = V_{DDA1} ≤ V_{DDA2}; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	f_{CLK13} = 13 MHz; see Fig.5	–	9	18	mA
$I_{DD(idle)(tot)}$	total idle current on the V_{DD} pins	$\overline{PD}$ = LOW	–	4	20	µA
Logic inputs (pins TRIG, STROBE, CLK and DATA)						
I_{LIL}	LOW-level input leakage current	V_{IL} = 0 V	−5	–	+5	µA
I_{LIH}	HIGH-level input leakage current	V_{IH} = 6 V	−5	–	+5	µA
C_i	input capacitance		–	10	–	pF
V_{IL}	LOW-level input voltage		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.5V_{DD}$	–	V_{DD}	V
3-state output (pin DF)						
V_{OL}	LOW-state output voltage	I_{OL} = I_{OH} = 3 mA	–	–	0.4	V
V_{OH}	HIGH-state output voltage	I_{OL} = I_{OH} = 3 mA	$0.7V_{DD}$	–	–	V
I_{LO}	3-state output leakage current	V_{DF} = 0 to V_{DD}	−5	–	+5	µA
Low-swing master clock input (pin CLK13)						
I_{LI}	input leakage current		−5	–	+5	µA
C_i	input capacitance		–	10	–	pF
$\lvert Z_i \rvert$	input impedance	f_{CLK13} = 13 MHz; note 1	–	5	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)	note 2	0.35	–	V_{DD}	V
Sensor input voltage (pin VS)						
$V_{i(VS)}$	input voltage at pin VS		−3.0	–	V_{DD}	V
Band gap						
I_{bias}	bias current (source for D1)	V_{VS} = 0 V; T_{amb} = 25 °C; TC = −0.08 µA/K	21	28	35	µA
V_{ref}	reference voltage	T_{amb} = 25 °C	1.18	1.25	1.32	V
TC	temperature coefficient for V_{ref}		–	±170	–	ppm/K
t_{pu}	power-up time for V_{ref}	note 3	–	5	50	µs
Power-on reset, threshold voltage V_{th}; see Fig.4						
V_{th}	threshold voltage	T_{amb} = 25 °C; TC = −4 mV/K	1.2	1.5	1.8	V
t_{rst}	reset time		–	–	50	µs

Notes

1. An AC coupling with 33 pF is recommended.
2. Tested at nominal working condition (V_{DDD} = V_{DDA1} = 3 V; V_{DDA2} = 5 V). AC coupling = 33 pF.
3. The necessary start-up time t_{ON} = 200 µs (see Fig.3) between $\overline{PD}$ and TRIG is more than t_{pu}.

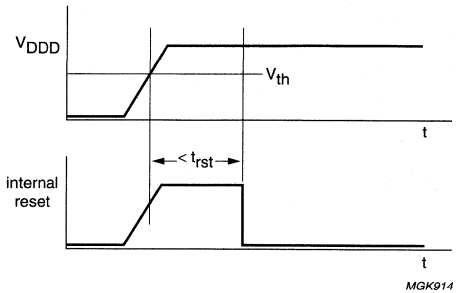
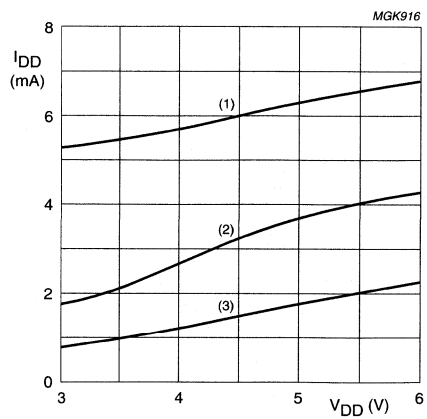


Fig.4 Timing diagram for on-chip reset function.



(1) I_{DDA1}. (2) I_{DDA2}. (3) I_{DDD}.

Fig.5 Operating current I_{DD} as a function of V_{DD}.

TIMING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = 2.7 to 6.0 V; $V_{DDD} = V_{DDA1} \leq V_{DDA2}$; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	UNIT
Controller timing; see Fig.3				
$t_{d(TRIG-B)}$	delay from positive TRIG edge to time B = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(B-C)}$	delay from time B to time C = $18T_{cy}$	–	8.31	µs
$t_{d(TRIG-E)}$	delay from negative TRIG edge to time E = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(E-G)}$	delay from time E to time G = $38T_{cy}$	–	17.54	µs
Serial bus timing; see Fig.6				
SERIAL PROGRAMMING CLOCK (PIN CLK)				
t_r	rise time	–	10	ns
t_f	fall time	–	10	ns
T_{cy}	clock period	100	–	ns
ENABLE PROGRAMMING (PIN STROBE)				
t_{start}	strobe start time to first clock edge	0	–	ns
t_{end}	strobe end time after last clock edge	40	–	ns
REGISTER SERIAL INPUT DATA (PIN DATA)				
t_{su}	input data to CLK set-up time	20	–	ns
t_h	input data to CLK hold time	20	–	ns

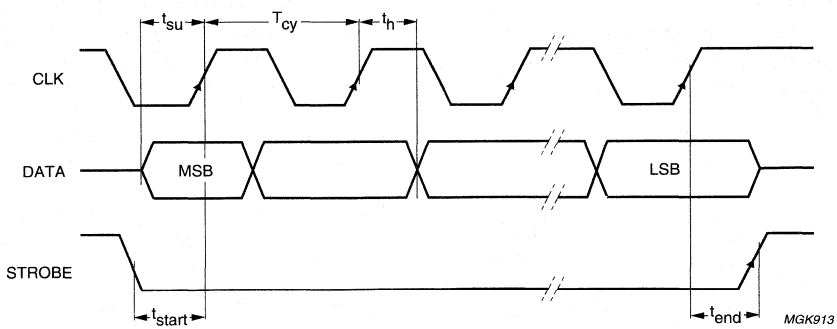


Fig.6 Serial bus timing diagram.

APPLICATION INFORMATION

Direct power control with ramping function (DC = 1)

The circuit offers a useful feature to control power levels close to the saturation region of the external power module.

This flexibility consists in the direct control on the power level by setting bit DC to logic 1.

In this condition, the external control loop is switched off by disabling the gain path from OP1. The ramping shape of the signal to be transmitted as well as its final level are driven only by the internally generated control signal from the slope generator. In this way transient effects to recover active components from deep saturation are avoided. The relative error on the absolute value of output power is quite limited, as a power amplifier is less sensitive to temperature variation in its saturated region. However, this way of operating may increase the phase error.

Increased dynamic range

The PCF5077T is able to control a dynamic range of 30 dBm by switching the gain factor of the sensor amplifier and the resolution of DAC8. This range corresponds to a maximum peak-to-peak voltage of 3 V measured at the sensor diode. Figure 7 shows the voltage at the sensor diode (V_S) versus the output power (P) of the Power Amplifier (PA) with a directional coupler of 20 dB attenuation. The maximum voltage of 3 V is reached when the output power is 35 dBm.

The sensor voltage for power level lower than 13 dBm, as necessary for GSM Phase 2 and DCS1800, is lower than 200 mV. An 8-bit DAC would not be sufficient to cover the complete dynamic range. Therefore bits DR0 and DR1 are used to switch the power range that can be controlled with the controller (see Table 7).

Reduced voltage steps of power level DAC8 (DR0 = 1)

The DR0 bit is used to switch resistor R9 (switch $\overline{DR0}$ is closed) at the integrator input (OP4). The ratio of the DAC8 range to the sensor signal voltage is therefore halved and the power corresponding to one LSB of DAC8 is reduced by 3 dB. With this setting the power module can be controlled more accurately for low output power levels.

Gain factor of OP1 (DR1)

Bit DR1 switches (switch $\overline{DR1}$ is closed) the ratio of the capacitances at OP1. The gain factor for the sensor amplifier is five times higher when DR1 is in high state.

When DR1 = 1, the control loop regulates the output power of the PA to a lower power level. A dynamic range of about 10 dBm can be switched by this manner.

$V_s : V_{peak}$ is the ratio of sensor signal to slope generator output voltage effective at the integrator output (OP4).

Table 7 Gain factors

DR1	DR0	$V_S : V_{peak}$
0	0	1 : 1
0	1	2 : 1
1	0	5 : 1
1	1	10 : 1

Additional application information

Evaluation kits with software and demonstration board are available for the PCF5077T together with Philips power modules BGY206, CGY2010, CGY2020 and CGY2021 for GSM and PCN, which will provide help for applications.

Very little bus traffic is required for the PCF5077T because the ramping curves are generated on-chip. V_{KICK} and V_{HOME} define the start conditions for up-ramping. V_{PL} determines the power levels. TRIG is the trigger for up and down-ramping.

The non-linear behaviour of the control curves of the power modules have a big influence on the loop. Start conditions in the flat area of the control curve are critical and need some attention. Initially $V_{INT(O)}$ will be at the home position. The HPA switches release the regulator. The integrator is moved into the active part of the control curve. This is achieved by integrating V_{KICK}. When $V_{INT(O)}$ has reached the active region of the control curve the loop is closed and the circuit is able to follow the ramping function generated by a voltage step to the slope generator. The step height V_{PL} determines the power of the transmit burst. Down-ramping is started at the slope generator input by a voltage step from V_{PL} back to V_{QRS}. The loop follows the leading function for down-ramping until the RF sensor measures zero. The reason for V_{QRS} is to shorten the tail of the slope.

Figures 8 and 9 show the results of measurements on the up and down-ramping where REF is the reference level of the power in the time slot, ATTEN is the attenuation of the input instrument for not to destroy the instrument itself, RES BW is the resolution bandwidth, VBW is the video bandwidth, CENTER is the carrier frequency for the burst that has been measured and SWP is the sweep time used for the measurement.

ADJUSTMENT OF THE HOME POSITION

The 6-bit DAC for V_{HOME} determines the start point of the burst in the time template. Curve 2 in Fig.8 shows what happens when V_{HOME} is too low. The burst starts too late and the up-ramping of the power is too steep. The steep up-ramping results in a wide transient spectra. The RF input power shall be switched off when the TRIG signal is LOW to keep the −70 dB margin before the burst.

The home position has to be adjusted for each mobile phone because of DAC tolerances and individual PA characteristics.

The temperature coefficients for V_{HOME} (−2 and −4 mV/K) are used to compensate the temperature shift of the PA control curve. Therefore the PA and the controller shall be placed nearby on the printed-circuit board. Additionally it has to be considered that the temperature of the PA and PCF5077T are different because the PA heats up itself. Software may help to adapt V_{HOME} to different temperatures.

ADJUSTMENT OF V_{KICK}

After the falling edge of HPA the integrator starts to increase the control voltage up to the position of V_{KICK} where the PA should have reached its active region. Increasing V_{KICK} at high power level makes the up ramping of the burst smoother and improves the transient spectra.

V_{KICK} must be reduced for low level of V_{PL} to avoid that both voltages become equal. Setting V_{KICK} to minimum value for the lowest power level can be sufficient.

At low power level the burst will start later because of the bend sensor curve (see Fig.7). The trigger pulse has to be started up to 3 bits earlier for the lowest power level to avoid that the power is ramped up too late for the first data bits of the burst.

LIMIT FOR CORRECT DOWN-RAMPING

The maximum RF power that the power module in saturation is able to deliver depends on RF input power, transmit frequency, supply voltage, temperature and load impedance. The maximum V_{PL} must be matched to the worst case output power and then reduced by 1 dB when the PCF5077T is used in closed loop mode.

Curve 2 in Fig.9 shows what happens when the PA is driven into saturation. The down-ramping of the power is getting too steep and therefore the transient spectra will be too wide. The 1 dB margin is necessary because of the flat PA control curve at high power level. The loop needs more time to reduce the power during the down-ramping and the control voltage increases. The high control voltage forces the power quickly down when the steep region of the control curve is achieved. The steep down-ramping results in a wide transient spectra.

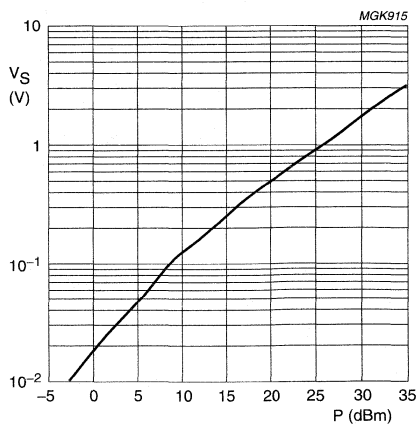
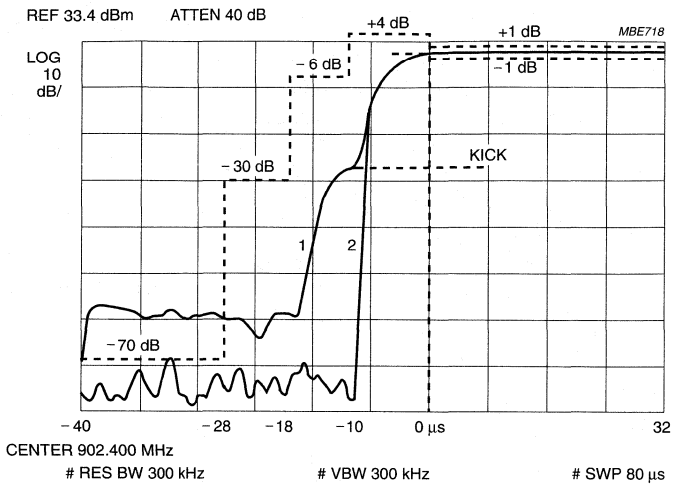
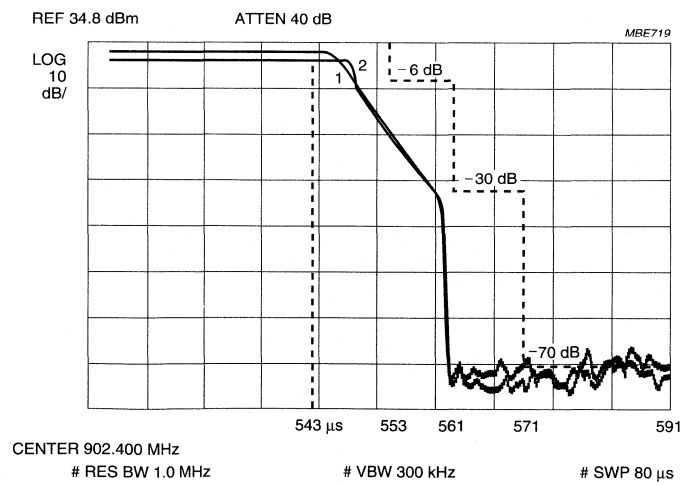


Fig.7 Sensor voltage as a function of output power (diode BAT62).



(1) Highest usable value.
(2) Lowest usable value.

Fig.8 Power as a function of time; rising edge (behaviour at different worst case home positions of $V_{INT(O)}$).



(1) Correct behaviour.
(2) Unusable behaviour with wrong V_{PL} value.

Fig.9 Power as a function of time; falling edge.

Application in mobile stations

Using a directional coupler with 16.5 dB attenuation produces a sensor signal between 100 mV and 3 V below the diode forward voltage at pin VS for the PA output power range of 8 to 36 dBm.

The sensor voltage of 3 V at pin VS corresponds to the maximum DAC output voltage. The power range that can be controlled is therefore not limited by the sensor voltage input VS and higher power levels can be controlled with the control loop switched on.

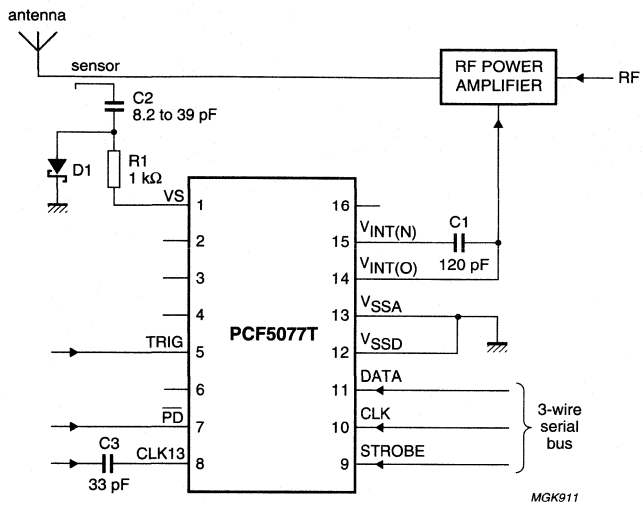


Fig.10 Application diagram for mobile stations.

Power amplifier controller for GSM and PCN systems

PCF5078

FEATURES

- Compatible with baseband interface family PCF5073x
- Two power sensor inputs
- Temperature compensation of sensor signal
- Active filter for DAC input
- Power Amplifier (PA) protection against mismatching
- Bias current source for detector diodes
- Generation of pre-bias level for PA at start of burst (home position)
- Possibility to adapt home position by external components
- Applicable for a wide range of silicon and GaAs power amplifiers.

APPLICATIONS

- Global System for Mobile communication (GSM)
- Personal Communications Network (PCN) systems.

GENERAL DESCRIPTION

This CMOS device integrates an amplifier for the detected RF voltage from the sensor, an integrator and an active filter to build a PA control loop for cellular systems with a small amount of passive components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	2.4	3.6	5.0	V
$I_{DD(tot)}$	total supply current	–	–	6	mA
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5078T	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3.0 mm	SOT505-1

BLOCK DIAGRAM

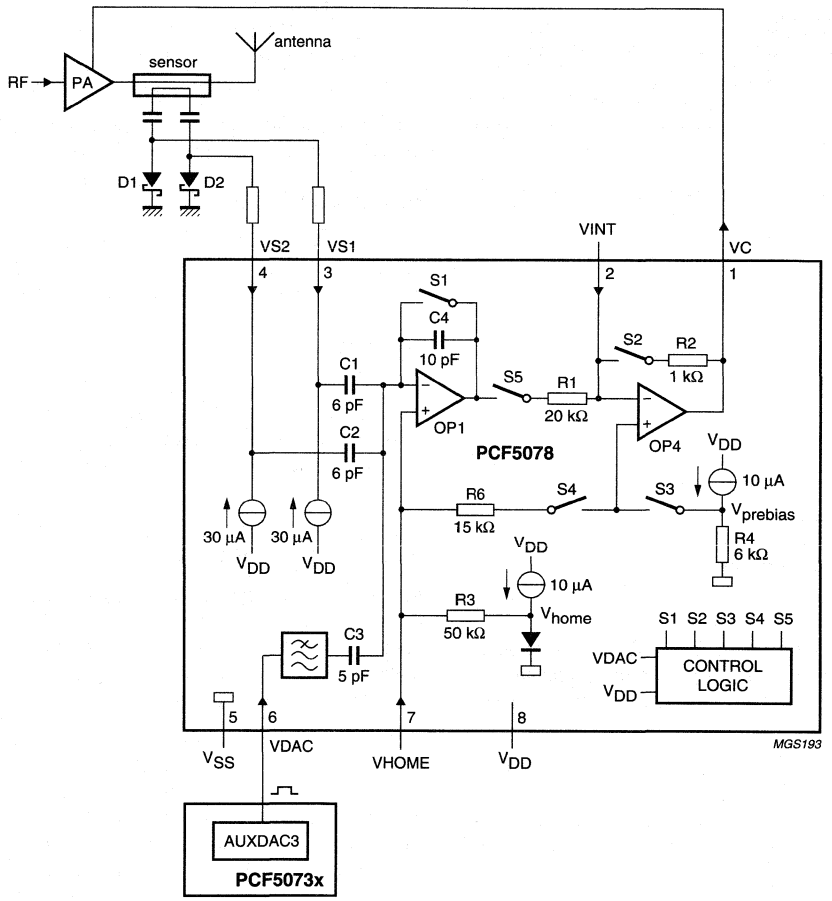


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VC	1	PA control output voltage
VINT	2	negative integrator input
VS1	3	sensor signal input 1
VS2	4	sensor signal input 2
V_{SS}	5	ground supply
VDAC	6	DAC input voltage
VHOME	7	home position input voltage
V_{DD}	8	supply voltage

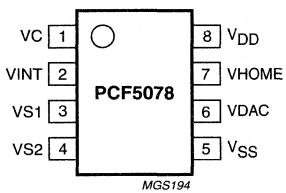


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The PCF5078 integrates an amplifier for the detected RF voltage from the sensor, an integrator and an active filter to build a PA control loop with a small amount of passive components.

The sensor amplifier is able to amplify signals from a RF power detector in a range of −20 to +15 dBm. This complies to the PA output power range of GSM and PCN systems when a directional coupler with 20 dB attenuation is used.

The Schottky diode for power detection (sensor) is biased by an integrated current source of 30 μA. Variations of the forward voltage of the diodes with the temperature have no influence on the measured signal, because they are cancelled by sampling around the switched capacitor operational amplifier OP1 (see Fig.1).

An external Digital-to-Analog Converter (DAC) with10-bit resolution is necessary to control the loop e.g. the AUXDAC3 of the baseband interface family PCF5073x.

An integrated active filter smooths the voltage steps of the DAC and avoids a feedthrough of the DAC harmonics into the modulation spectra of the PA.

The DAC signal and the sensor signal are added by operational amplifier OP1. The voltage difference of both signals is integrated by operational amplifier OP4, which provides the PA control voltage on pin VC. The integration is performed by means of an external capacitance C_{VINT} connected between pins VINT and VC.

The shape of the rising and falling power burst edges can be determined by means of the DAC voltage (see Fig.3).

Power-down mode

During the not used time slots in Time Division Multiple Access (TDMA) systems, the PCF5078 must be turned off by switching off the supply voltage on pin V_{DD}.

Initial conditions and start-up

The PCF5078 has been designed to operate in bursts as required in TDMA systems. For each time slot to be transmitted it must be powered-up by switching on the supply voltage. This allows a proper initialization of switches S1 to S5.

During start-up switches S1, S2 and S3 are closed and switches S4 and S5 are opened (see Fig.4).

The forward voltages on the Schottky diodes are sampled on capacitors C1 and C2, respectively, because switch S1 is closed. Moreover, the control voltage on pin VC is initially forced to pre-bias level $V_{prebias}$ because switches S2 and S3 are closed and switch S4 is opened.

Switch S1 is opened after a fixed time the supply voltage has been switched on and then the circuit is ready. This time is defined on-chip and can be maximum 45 μs. Once switch S1 is open, a ramp signal with a minimum amplitude of 25 mV applied on pin VDAC determines opening of switch S3 and closing of switch S4 with a delay of maximum 3 μs with respect to the start of the ramp.

After opening switch S3, the control voltage on pin VC rises in a fixed amount of time to the home position level so biasing the PA to the beginning of the active range of its control curve. Switch S2 remains closed during this typical time of 2 μs. When switch S2 is opened, switch S5 is closed allowing the transfer of any signal coming from amplifier OP1.

After this preset, the control voltage is free to increase according to the control loop if RF input is present (see Fig.3).

For higher DAC ramp steps the delay time of opening switch S3 (and closing switch S4) is reduced. On the contrary, the delay time between opening switch S2 with respect to opening switch S3 (and closing switch S4) remains unchanged.

For a correct start-up it is required that the rising time of the supply voltage is maximum 20 µs.

End of a burst

For a proper down ramp, the final value of the DAC input voltage should be below the value at the beginning of the burst and so be able to really shut-off the PA (see Fig.5). This means the code programmed for the last bit of the DAC down ramp ($CODE_{END}$) has to be lower than the initial value of the up ramp ($CODE_{START}$). Moreover, the last code must be maintained until the supply voltage has been switched off.

When the voltage on pin VC is detected to be lower than V_{VHOME} a built-in mechanism forces the voltage on pin VC to $V_{prebias}$ by closing switches S1, S2 and S3 and by opening switches S4 and S5.

For proper operation, the supply voltage should be switched off at least 15 µs later with respect to the end of the down ramp on pin VDAC.

PA protection against mismatching

A second sensor amplified input is integrated into the PCF5078 for measuring the reflected wave of the directional coupler. The signal is added to the measured RF power signal (see Fig.3). When mismatching at the output of the PA occurs the power is reduced. A high Voltage Standing Wave Ratio (VSWR) at the output of the PA often occurs in systems where the PA is connected to the antenna via switches with low attenuation instead of using a duplex filter.

Home position voltage

A forward voltage of an on-chip silicon diode is provided as the default home position voltage V_{home}. This voltage matches the requirements at the control input of most PAs and exhibits the same temperature coefficient.

However, if another value is needed for a certain PA the level can be adjusted by connecting external components to pin VHOME (see Figs 10 and 11). The home position voltage can be set between 200 and 1000 mV when using a capacitor of 50 pF connected between pins VINT and VC.

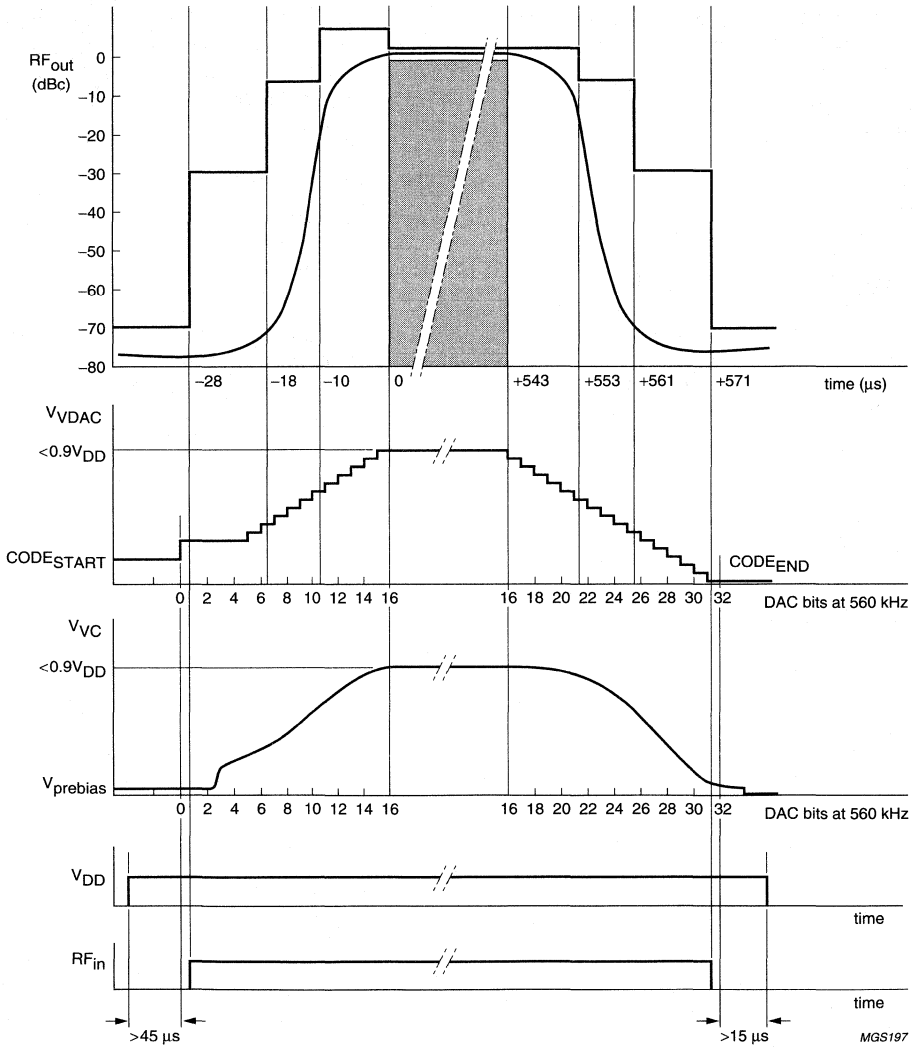


Fig.3 Timing diagram.

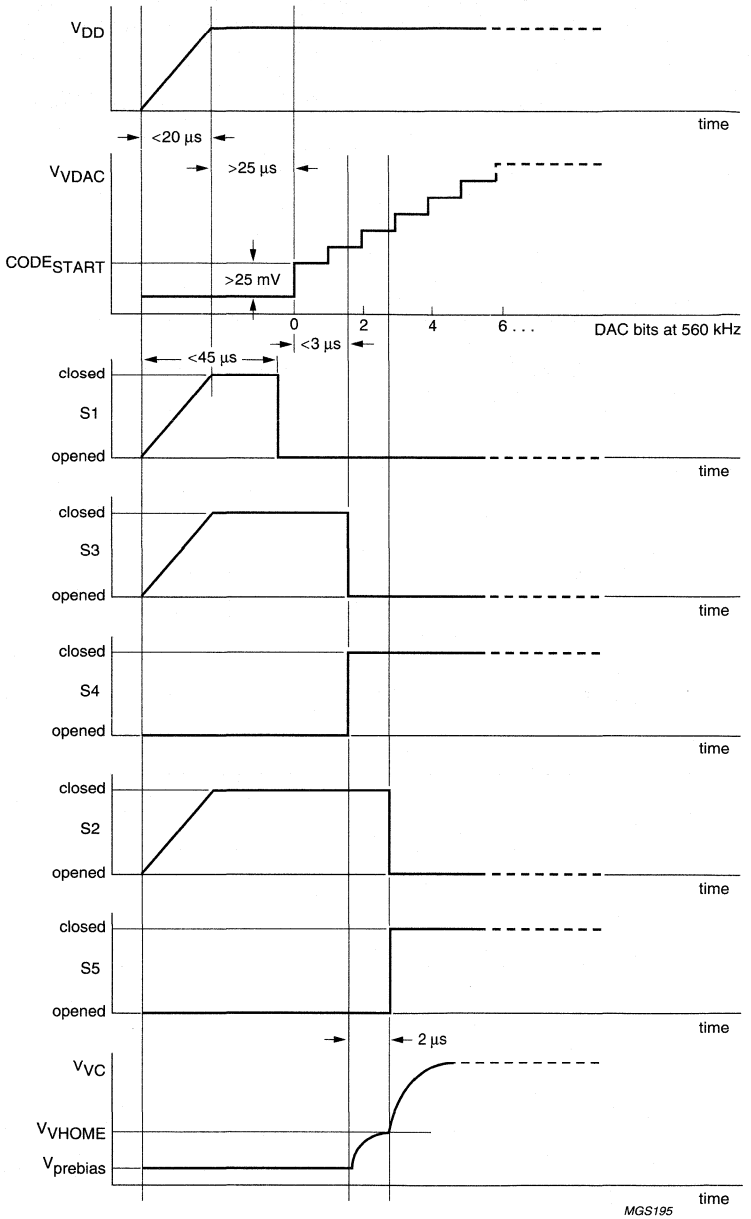


Fig.4 Initialization and start of a burst diagram.

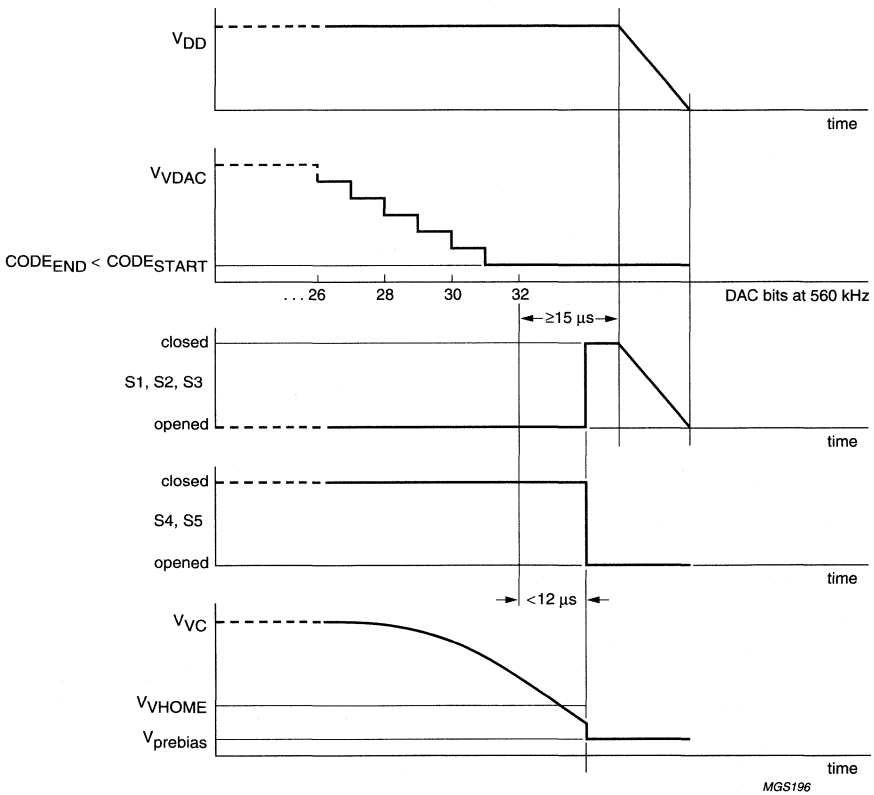


Fig.5 End of a burst diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	2.4	6.0	V
V_n	DC voltage on			
	pins VS2 and VS2	−3.0	+6.0	V
	all other pins	−0.5	+6.0	V
I_n	DC current on any signal pin	−10	+10	mA
P_{tot}	total power dissipation	–	315	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

CHARACTERISTICS

V_{DD} = 2.4 to 5 V; T_{amb} = −40 to +85 °C; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.4	3.6	5.0	V
$I_{DD(tot)}$	total supply current		–	–	6	mA
Sensor input voltage						
$V_{I(n)}$	input voltage on pins VS1 and VS2		−3	–	V_{DD}	V
Bias current source						
I_{bias}	detector diode bias current	no input signal; T_{amb} = 25 °C; see Fig.7				
		V_{DD} = 2.4 V	17	28	39	µA
		V_{DD} = 5.0 V	21	33	45	µA
TC_{bias}	temperature coefficient of bias current source		–	0.07	–	µA/K
Home position voltage						
V_{home}	internal home position voltage	T_{amb} = 25 °C	0.550	0.600	0.650	V
TC_{home}	temperature coefficient of internal home position voltage source		–	−2.1	–	mV/K
R3	resistor for internal home position voltage		–	50	–	kΩ
$V_{I(VHOME)}$	home position input voltage		200	–	1000[1]	mV
Low pass filter for DAC signal (3rd-order Bessel)						
f_{3dB}	corner frequency		70	100	130	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Integrator (OP4)						
B_G	gain bandwidth	C_L = 120 pF; note 2	–	4	–	MHz
PSRR	power supply rejection ratio	at 217 Hz; V_{DD} = 3 V; note 2	50	55	–	dB
SR_{pos}	positive slew rate	V_{DD} = 3 V; note 3	3.5	4.5	–	V/µs
SR_{neg}	negative slew rate	V_{DD} = 3 V; note 3	3.5	4.5	–	V/µs
$V_{O(min)}$	minimum output voltage	T_{amb} = 25 °C; see Fig.8	–	–	0.2	V
$V_{O(max)}$	maximum output voltage	R_L = 700 Ω; see Fig.6	0.85V_{DD}	–	–	V
Capacitors C1, C2, C3 and C4						
M	matching ratio accuracy between capacitances		–	1	–	%

Notes

1. For C_{VINT} = 50 pF.
2. Guaranteed by design.
3. Slew rates are measured between 10% and 90% of output voltage level with an load of approximately 40 pF to ground.

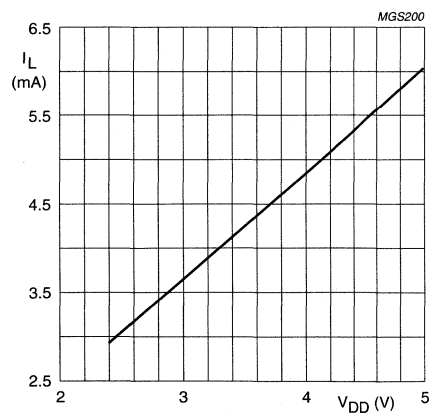
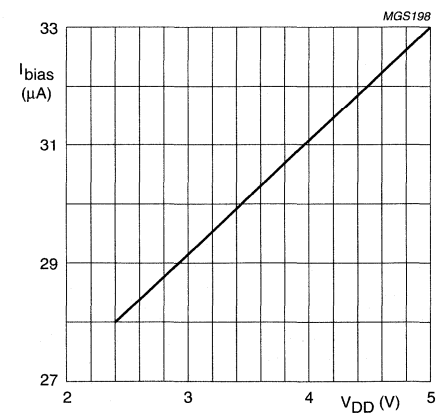


Fig.6 Minimum load current as a function of the supply voltage.



T_{amb} = 25 °C.

Fig.7 Typical bias current as a function of the supply voltage.

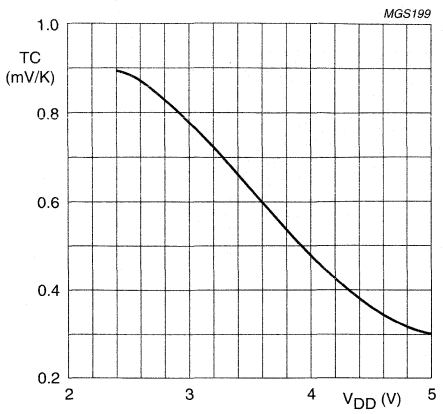


Fig.8 Temperature coefficient of the minimum output voltage as a function of the supply voltage.

APPLICATION INFORMATION

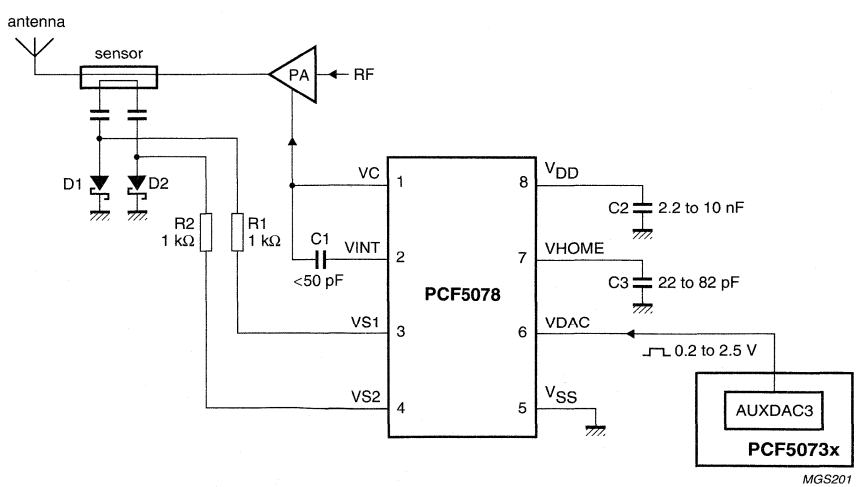
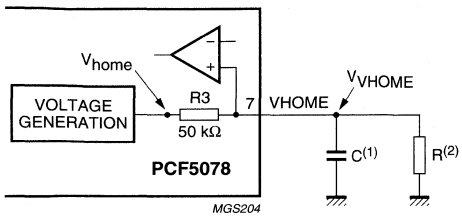


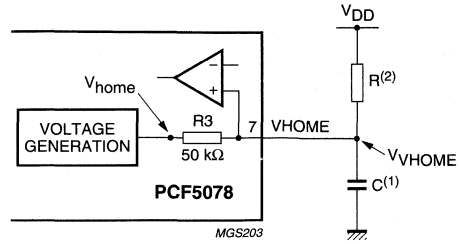
Fig.9 Application diagram for mobile station with PA protection against mismatching.



(1) C = 22 to 82 pF.

(2) $R = \frac{V_{VHOME}}{V_{home} - V_{VHOME}} \times R3$

Fig.10 Suggested method to force externally $V_{VHOME} < V_{home}$.



(1) C = 22 to 82 pF.

(2) $R = \frac{V_{DD} - V_{VHOME}}{V_{VHOME} - V_{home}} \times R3$

Fig.11 Suggested method to force externally $V_{VHOME} > V_{home}$.

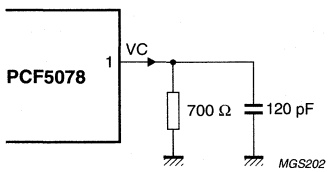


Fig.12 Typical output load on pin VC.

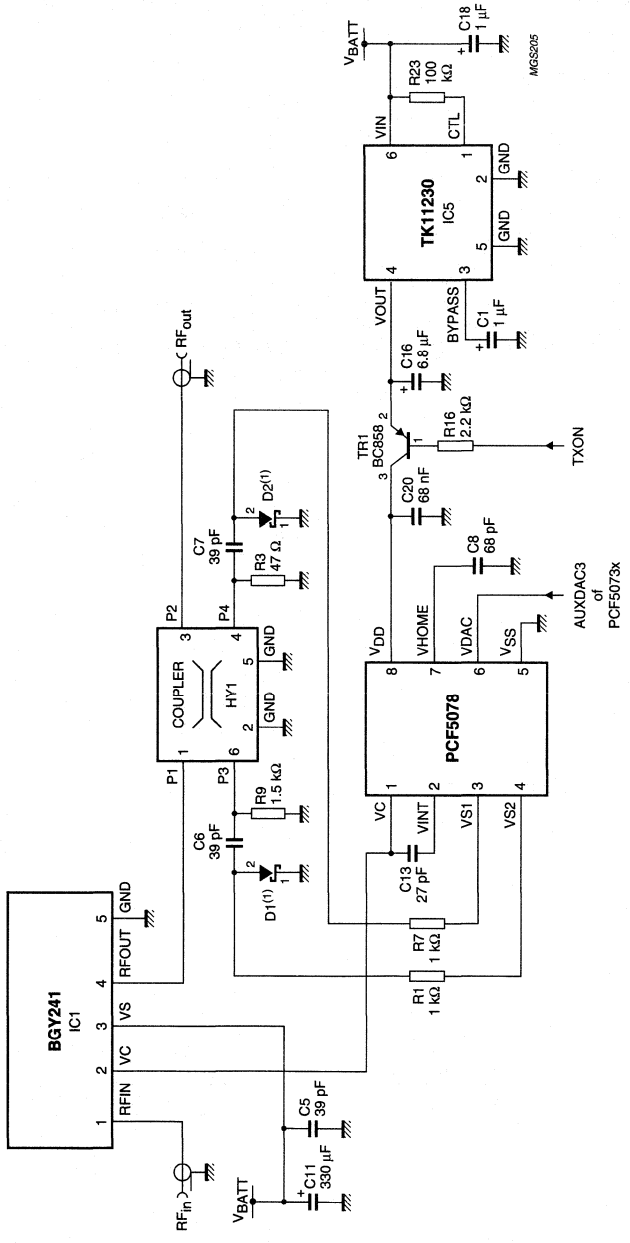


Fig.13 Application example of PCF5078.

(1) D1 and D2: type BAT62_03W

34 × 128 pixel matrix driver PCF8531

FEATURES

- Single chip LCD controller/driver
- 34 row, 128 column outputs
- Display data RAM 34 × 128 bits
- 128 icons (last row is used for icons)
- Fast mode I²C-bus interface (400 kbits/s)
- Software selectable multiplex rates: 1 : 17, 1 : 26 and 1 : 34
- Icon mode with mux rate 1 : 2
  - Featuring reduced current consumption while displaying icons only.
- On-chip:
  - Generation of V_{LCD} (external supply also possible)
  - Selectable linear temperature compensation
  - Oscillator requires no external components (external clock also possible)
  - Generation of intermediate LCD bias voltages
  - Power-on reset.
- No external components
- Software selectable bias configuration
- Logic supply voltage range $V_{DD1} - V_{SS1}$: 1.8 to 5.5 V
- Supply voltage range for on-chip voltage generator $V_{DD2,3} - V_{SS1,2}$: 2.5 to 4.5 V
- Display supply voltage range $V_{LCD} - V_{SS}$:
  - Normal mode: 4 to 9 V
  - Icon mode: 3 to 9 V.
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process.

APPLICATIONS

- Telecommunication systems
- Automotive information systems
- Point-of-sale-terminals
- Instrumentation.

GENERAL DESCRIPTION

The PCF8531 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex-rates of 1 : 17, 1 : 26 and 1 : 34. Furthermore, it can drive up to 128 icons. All necessary functions for the display are provided in a single chip, including on-chip generation of V_{LCD} and the LCD bias voltages, resulting in a minimum of external components and low power consumption. The PCF8531 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). All inputs are CMOS compatible.

Note: Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

Packages

The PCF8531 is available as chip with bumps in tray.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8531U/2/F1	–	chip with bumps in tray	–

BLOCK DIAGRAM

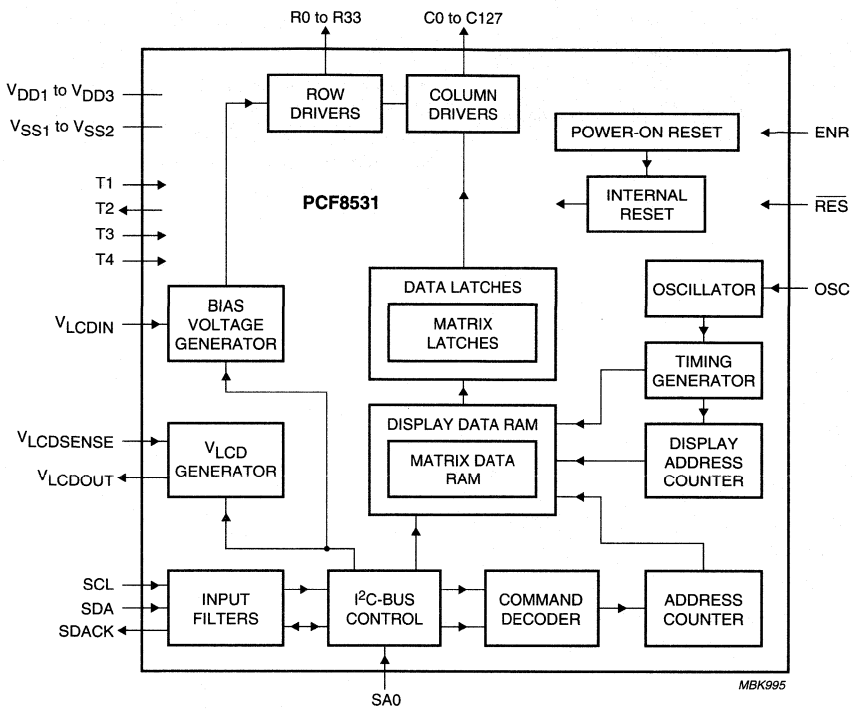


Fig.1 Block diagram.

Universal LCD driver for low multiplex rates

PCF8533

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives: up to forty 8-segment numeric characters; up to twentyone15-segment alphanumeric characters; or any graphics of up to 320 elements
- 80 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 1.8 to 5.5 V
- Wide LCD supply range: from 2.5 V for low-threshold LCDs and up to 6.5 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- 400 kHz I²C-bus interface
- TTL/CMOS compatible
- Compatible with 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 5120 segments possible)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8533 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications.

The PCF8533 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8533U	–	chip with bumps in tray	–

BLOCK DIAGRAM

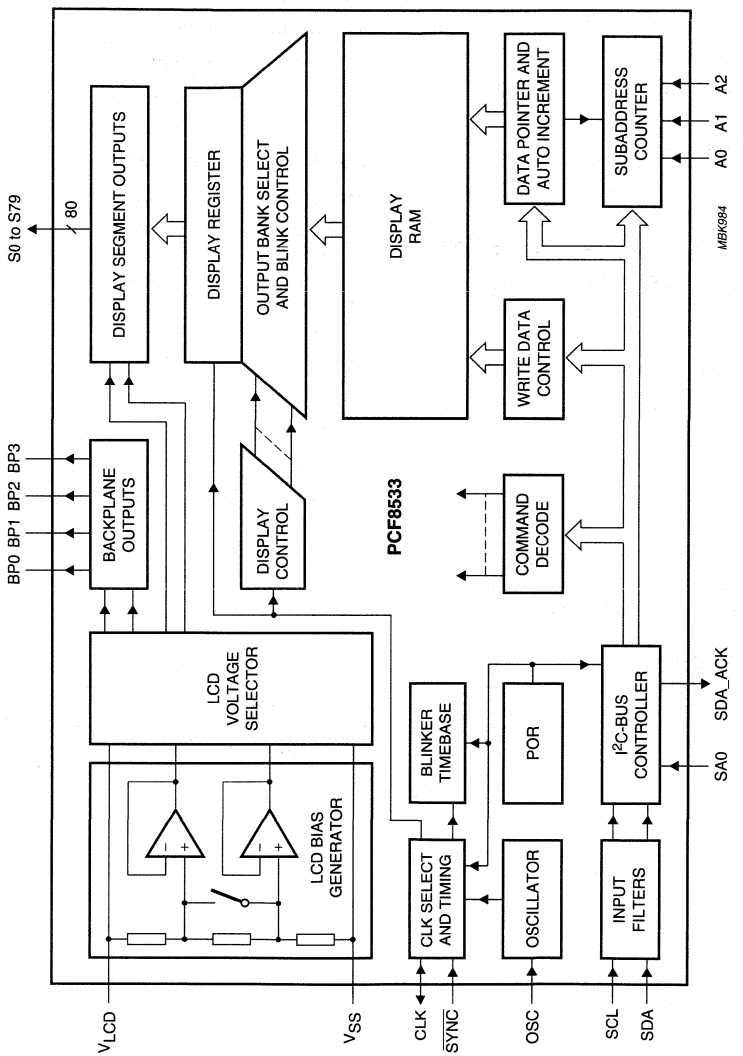


Fig.1 Block diagram.

65 × 102 pixels matrix LCD driver PCF8548

FEATURES

- Single-chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Configurable 5× (4, 3, 2) voltage multiplier generating V_{LCD} (external V_{LCD} also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- 400 kbits/s fast I²C-bus interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.9 to 5.5 V
- High voltage generator supply voltage range $V_{DD2} - V_{SS}$: 2.4 to 4.5 V with LCD voltage internally generated (voltage generator enabled)
- Display supply voltage range $V_{LCD} - V_{SS}$: 4.5 to 9.0 V.
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Slim chip layout, suited for Chip-On-Glass (COG) applications.
- programmable bottom row pads mirroring and top row pads mirroring, for compatibility with both TCP (Tape Carrier Package) and COG applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8548 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8548 interfaces to most microcontrollers via an I²C-bus interface.

Packages

The PCF8548 is available as chip with bumps in tray, Tape Carrier Package (TCP) is available on request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	
	NAME	DESCRIPTION
PCF8548U/2	–	chip with bumps in tray

BLOCK DIAGRAM

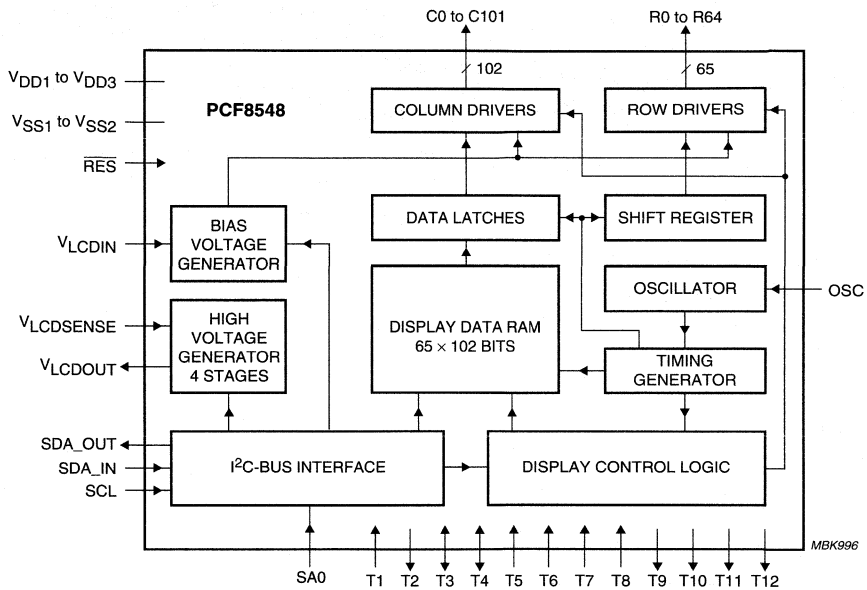


Fig.1 Block diagram.

65 × 102 pixels matrix LCD driver PCF8549

FEATURES

- Single chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Generation of LCD supply voltage
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz Fast I²C Interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.5 to 6 V
- Voltage generator voltage range $V_{DD2/2\_HV} - V_{SS}$: 2.4 to 5 V
- Display supply voltage range $V_{LCD} - V_{SS}$: 7.0 to 16 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Interlacing for better display quality
- Slim chip layout, suited for chip-on-glass applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8549 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8549 interfaces to most microcontrollers via an I²C interface.

Packages

The PCF8549U/2 is available as bumped die. Sawn wafer as chip sorted in chip tray.

Customized TCP upon request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8549U/2/F1	TRAY	chip with bumps in tray	

BLOCK DIAGRAM

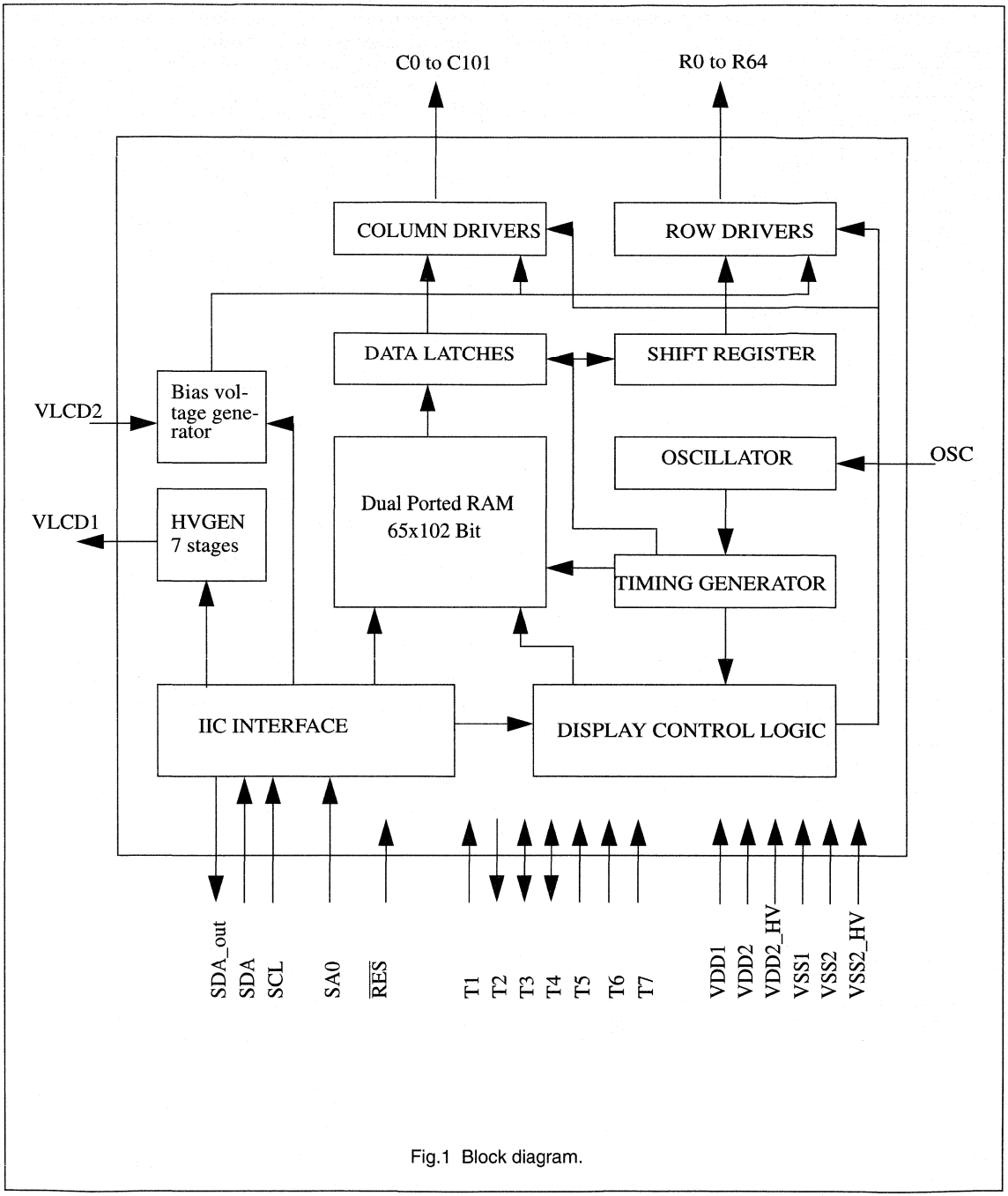


Fig.1 Block diagram.

PINNING

SYMBOL	DESCRIPTION
R0 to R64	LCD row driver outputs
C0 to C101	LCD column driver outputs
$V_{SS1,2,2\_HV}$	negative power supply
$V_{DD1,2,2\_HV}$	supply voltage
$V_{LCD1,2}$	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 I/O
T4	test 4 I/O
T5	test 5 input
T6	test 6 input
T7	test 7 input
SDA	I^2C data input
SCL	I^2C clock line
SDA_OUT	I^2C output
SA0	least significant bit of slave address
OSC	oscillator
$\overline{RES}$	external reset input, low active

Pin functions

R0 TO R64: ROW DRIVER OUTPUTS

These pads output the row signals.

C0 TO C101: COLUMN DRIVER OUTPUTS

These pads output the column signals.

$V_{SS1,2,2\_HV}$: NEGATIVE POWER SUPPLY RAILS

Negative power supplies.

$V_{DD1,2,2\_HV}$: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD2_HV} are the supply voltages for the internal voltage generator. Both have to be on the same voltage and may be connected together outside of the chip. If the internal voltage generator is not used, they should be both connected to ground. V_{DD1} is used as power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD2_HV}.

$V_{LCD1,2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCD1} and V_{LCD2} must be connected together. An external LCD supply voltage can be supplied using the V pad. In this case, V_{LCD1} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8549 is in power-down mode, the external LCD supply voltage has to be switched off.

T1, T2, T3, T4, T5, T6 AND T7: TEST PADS

T1, T3, T4, T5, T6 and T7 must be connected to V_{SS1}, T2 is to be left open. Not accessible to user.

SDA/SDA_OUT: I^2C DATA LINES

Output and input are separated. If both pads are connected together they behave like a standard I^2C pad.

SCL: I^2C CLOCK SIGNAL

Input for the I^2C-bus clock signal.

SA0: SLAVE ADDRESS

With the SA0 pin two different slave addresses can be selected. That allows to connect two PCF8549 LCD drivers to the same I^2C-bus.

OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

$\overline{RES}$: RESET

This signal will reset the device. Signal is active low.

Universal LCD driver for small graphic panels

PCF8558

FEATURES

- Single-chip LCD controller/driver
- 40 row and 101 column outputs
- Display data RAM
  40 × 101 bits = 505 bytes = 4040 bits
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz fast I²C-bus interface
- CMOS compatible
- MUX rate 1 : 40
- Logic supply voltage range $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption, suitable for battery operated systems.

GENERAL DESCRIPTION

The PCF8558 is a low power CMOS LCD controller driver, designed to drive a graphic display of 40 rows and 101 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption.

The PCF8558 interfaces to most microcontrollers via a I²C-bus interface.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals
- Alarm systems.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8558U/10	–	chip on FFC	–
PCF8558U/12	–	chip with bumps on FFC	–

BLOCK DIAGRAM

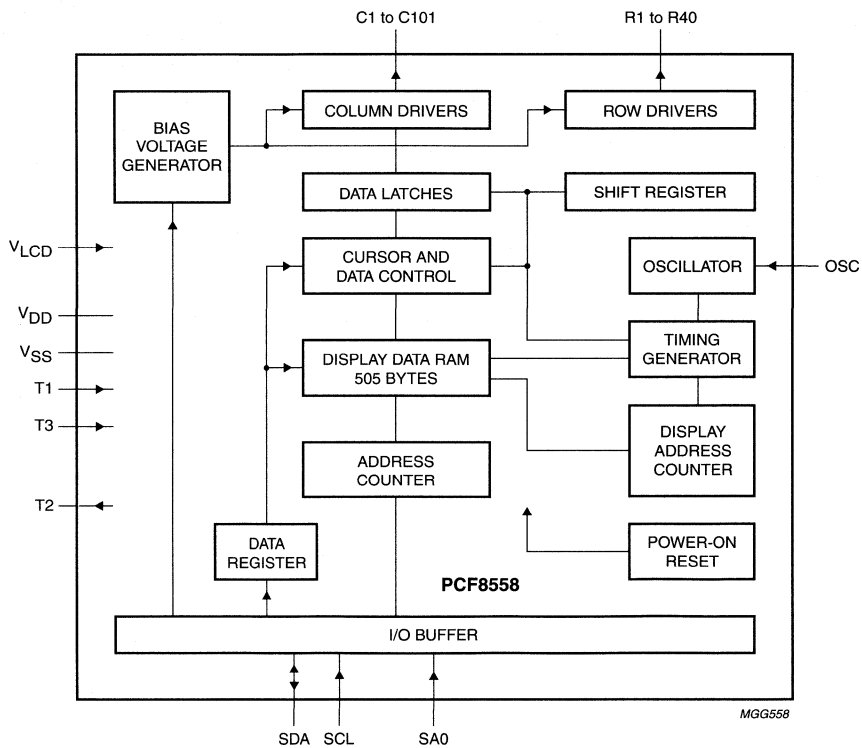


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
SCL	1	I^2C-bus serial clock input
R20 to R1	2 to 21	LCD row driver data outputs
C101 to C1	22 to 122	LCD column driver data outputs
R21 to R40	123 to 142	LCD row driver data outputs
T2	143	test pad output, must be left unconnected (not user accessible)
SDA	144	I^2C-bus serial data input/output
V_{SS}	145	ground
T1	146	test pad input, must be connected to V_{SS} (not user accessible)
V_{LCD}	147	negative supply voltage input
SA0	148	the LSB bit of the I^2C-bus slave address input is set by connecting this pin to either 0 (V_{SS}) or 1 (V_{DD})
T3	149	test pad input, must be connected to V_{DD} (not user accessible)
OSC	150	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
V_{DD}	151	positive supply voltage

Real-time clock/calendar PCF8563

FEATURES

- Provides year, month, day, weekday, hours, minutes, seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide clock operating voltage: 1.0 - 5.5 V
- Low back-up current typical 0.25 μA @ 3.0 V, 25 °C
- 400 kHz two-wire I²C interface (1.8 - 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- Alarm and timer functions
- Low-voltage detector
- Integrated oscillator capacitor
- Internal power-on reset
- I²C slave address: read A3h, write A2h
- Open drain interrupt pin.

GENERAL DESCRIPTION

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C bus. Maximum bus speed is 400 kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

APPLICATIONS

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage operating mode	I²C bus active –40 to +85 °C	1.8	5.5	V
		Clock operating, 25 °C	1.0	5.5	V
I_{DD}	Supply current (Timer and CLKOUT disabled)	f_{SCL} = 100 kHz	–	200	μA
		f_{SCL} = 400 kHz	–	800	μA
		f_{SCL} = 0 Hz: V_{DD} = 5 V, 25 °C	–	1.0	μA
		f_{SCL} = 0 Hz: V_{DD} = 2 V, 25 °C	–	0.75	μA
T_{AMB}	Operating ambient temperature		–40	+85	°C
T_{STG}	Storage temperature		–55	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

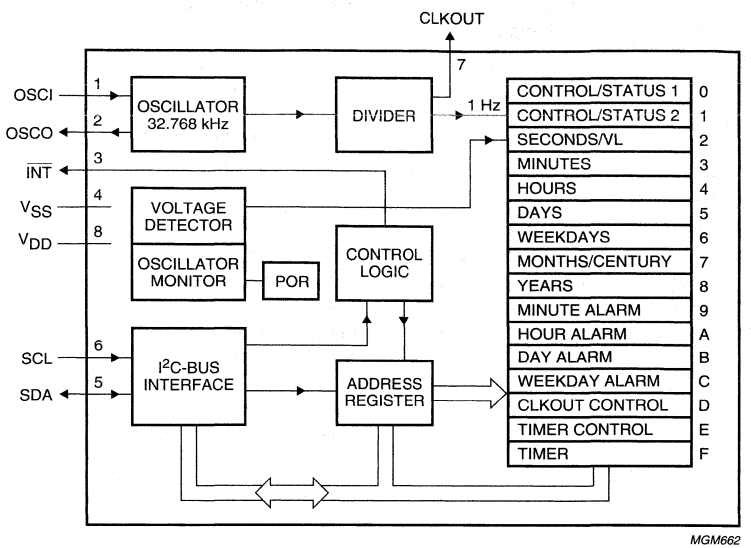


Fig.1 Block diagram PCF8563 real-time clock/calendar.

PINNING INFORMATION

Pin description

SYMBOL	PIN	DESCRIPTION
OSCI	1	Oscillator input
OSCO	2	Oscillator output
$\overline{INT}$	3	Open drain interrupt output (active LOW)
V_{SS}	4	Ground
SDA	5	Serial data I/O
SCL	6	Serial clock input
CLKOUT	7	Clock output
V_{DD}	8	Positive supply

Pinning

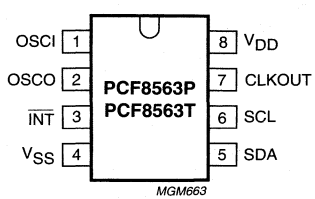


Fig.2 Pinning.

FUNCTIONAL DESCRIPTION

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the real time clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00, 01) are used as control and/or status registers. The memory addresses 02 through 08 are used as counters for the clock function (seconds up to year counters). Address locations 09 through 0C contain alarm registers which define the conditions for an alarm. Address 0D controls the CLKOUT output frequency. 0E and 0F are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Alarm function modes

By clearing the MSB of one or more of the alarm registers (AE = 'Alarm Enable'), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF may only be cleared by software.

Timer

The 8-bit countdown timer at address 0F is controlled by the timer control register at address 0E. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $1/_{60}$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT register at address 0D. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a push-pull output and enabled at power on. If disabled it becomes logic 0.

Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE bits which are set to 1.

Voltage low detector & clock monitor

The PCF8563 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW} the 'Voltage Low' (VL, bit 7 in the seconds register) is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Register organization

Bit positions labelled as 'x' are not implemented, those labelled with '0' should always be written with 0.

ADDRESS	FUNCTION	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	Control/status 1	TEST1	0	STOP	0	TESTC	0	0	0
01	Control/status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1
09	Minute alarm	AE	4	2	1	8	4	2	1
0A	Hour alarm	AE	x	2	1	8	4	2	1
0B	Day alarm	AE	x	2	1	8	4	2	1
0C	Weekday alarm	AE	x	x	x	x	4	2	1
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

Bit assignments

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Control/Status 1		**Address 00**	
3	TESTC	0	Power on reset override facility is disabled. Set to 0 for normal operation.
		1	Power on reset override may be enabled.
5	STOP	0	RTC source clock runs.
		1	All RTC divider chain flip flops are asynchronously set to 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
7	TEST1	0	Normal mode.
		1	EXT_CLK test mode.
Control/Status 2		**Address 01**	
TIE & AIE		These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set	
0	TIE	0	Timer interrupt disabled
		1	Timer interrupt enabled
1	AIE	0	Alarm interrupt disabled
		1	Alarm interrupt enabled

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
TF & AF		When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.	
2	TF	0 (READ)	Timer flag inactive.
		1 (READ)	Timer flag active.
		0 (WRITE)	Timer flag is cleared.
		1 (WRITE)	Timer flag remains unchanged.
3	AF	0 (READ)	Alarm flag inactive.
		1 (READ)	Alarm flag active.
		0 (WRITE)	Alarm flag is cleared.
		1 (WRITE)	Alarm flag remains unchanged.
4	TI/TP	0	$\overline{INT}$ is active when TF is active (subject to the status of TIE).
		1	$\overline{INT}$ pulses active according to table 1(subject to the status of TIE). Note that if AF and AIE are active then $\overline{INT}$ will be permanently active.
Seconds & VL		**Address 02**	
6..0	Seconds	00 - 59	This register holds the current seconds coded in BCD format. Example: seconds register contains 'x1011001' = 59 seconds.
7	VL	0	Clock integrity is guaranteed.
		1	Integrity of the clock information is no longer guaranteed.
Minutes		**Address 03**	
6..0	Minutes	00 - 59	This register holds the current minutes coded in BCD format.
Hours		**Address 04**	
5..0	Hours	00 - 23	This register holds the current hours coded in BCD format.
Days		**Address 05**	
5..0	Days(1)	01 - 31	This register holds the current day coded in BCD format.
Weekdays		**Address 06**	
2..0	Weekdays(2)	0 - 6	This register holds the current weekday coded in BCD format, see table 4.
Months & Century		**Address 07**	
4..0	Month	01 - 12	This register holds the current month coded in BCD format, see table 5.
7	Century(2)	0	Indicates the century is 20xx.
		1	Indicates the century is 19xx.
		This bit is toggled when the years register overflows from 99 to 00.	
Years		**Address 08**	
7..0	Years	00 - 99	This register holds the current year coded in BCD format.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Alarm registers		**Address 09 to 0C**	
		When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding 'Alarm Enable' (AE) is '0', then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the 'Alarm Flag' (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their 'Alarm Enable' bit at '1' will be ignored.	
Alarm: Minute		**Address 09**	
6..0	Alarm minutes	00 - 59	This register holds the minute alarm information coded in BCD format.
7	AE	0	Minute alarm is enabled.
		1	Minute alarm is disabled.
Alarm: Hour		**Address 0A**	
5..0	Alarm hours	00 - 23	This register holds the hour alarm information coded in BCD format.
7	AE	0	Hour alarm is enabled.
		1	Hour alarm is disabled.
Alarm: Day		**Address 0B**	
5..0	Alarm days	01 - 31	This register holds the day alarm information coded in BCD format.
7	AE	0	Day alarm is enabled.
		1	Day alarm is disabled.
Alarm: Weekday		**Address 0C**	
2..0	Alarm weekdays	00 - 00	This register holds the weekday alarm information coded in BCD format.
7	AE	0	Weekday alarm is enabled.
		1	Weekday alarm is disabled.
CLKOUT frequency		**Address 0D**	
1..0	FD1, FD0		These bits control the frequency output on the CLKOUT pin, see table 2.
7	FE	0	The CLKOUT output is inhibited and CLKOUT output is set to logic 0.
		1	The CLKOUT output is activated.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Countdown Timer		**Address 0E and 0F**	
		The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control/status 2 registers. For accurate read back of the countdown value, the I^2C clock (SDA) must be operating at a frequency of at least twice the selected timer clock.	
Timer control		**Address 0E**	
1..0	TD1, TD0		Timer source clock frequency select. These bits determine the source clock for the countdown timer, see table 3. When not in use, TD1 & TD0 should be set to 1/60 Hz for power saving.
7	TE	0	Timer is disabled.
		1	Timer is enabled.
Timer countdown value		**Address 0F**	
7..0	Timer	00..FF	Countdown value, n. $\text{CountdownPeriod} = \frac{n}{\text{SourceClockFrequency}}$

Notes

1. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.
2. These bits may be re-assigned by the user.

Table 1 $\overline{\text{INT}}$ OPERATION (TI/TP=1)

$\overline{\text{INT}}$ PERIOD		
SOURCE CLOCK	**n = 1**	**n > 1**
4096 Hz	1/8192 s	1/4096 s
64 Hz	1/128 s	1/64 s
1 Hz	1/64 s	1/64 s
1/60 Hz	1/64 s	1/64 s

Notes

1. n = Loaded countdown value.
   Timer stopped when n = 0.
2. TF and $\overline{\text{INT}}$ become active simultaneously.

Table 2 FD1, FD0: CLKOUT frequency selection.

FD1	FD0	CLKOUT FREQUENCY
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

Table 3 TD1, TD0: Timer frequency selection.

TD1	TD0	TIMER SOURCE CLOCK FREQUENCY
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

Table 4 Weekday assignments.

DAY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 5 Month assignments

MONTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

EXT_CLK test mode.

A test mode is available which allows for on board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the TEST1 bit in Control/Status1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300ns and a minimum period of 1000ns. The internal 64 Hz clock, now sourced from CLKOUT, is divide down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Note. Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

OPERATION EXAMPLE.

1. Set EXT_CLK test mode (Bit7 Control/Status1 = 1).
2. Set STOP (Bit5 Control/Status1 = 1).
3. Clear STOP (Bit5 Control/Status1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 & 8 for additional increments.

Power On Reset override.

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on board test of the device. The setting of this mode requires that the I^2C pins, SDA and SCL, be toggled in a specific order as shown in figure 3. All timings are required minimums.

Once the override mode has been entered, the chip immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C access. The override mode may be cleared by writing a 0 to TESTC. TESTC must be set to 1 before re-entry into the override mode is possible. Setting TESTC to 0 during normal operation has no effect except to prevent entry into the POR override mode.

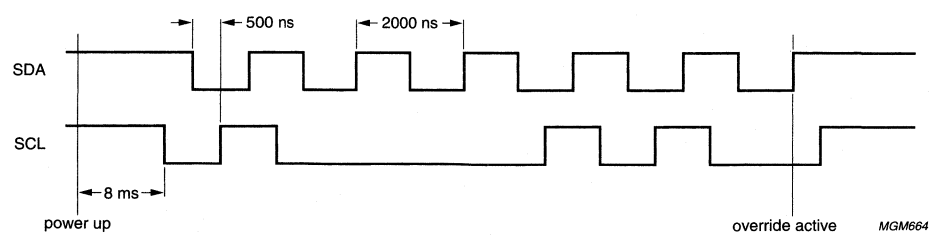


Fig.3 POR override sequence.

LIMITING VALUES.

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}	Supply current	−50	+50	mA
I_{SS}	Supply current	−50	+50	mA
P_{TOT}	total power dissipation	−	300	mW
T_{AMB}	operating ambient temperature	−40	+85	°C
T_{STG}	storage temperature	−65	+150	°C

CHARACTERISTICS OF THE I²C-BUS.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

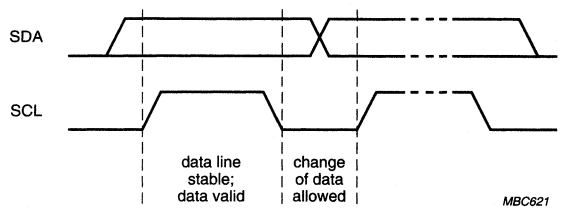


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

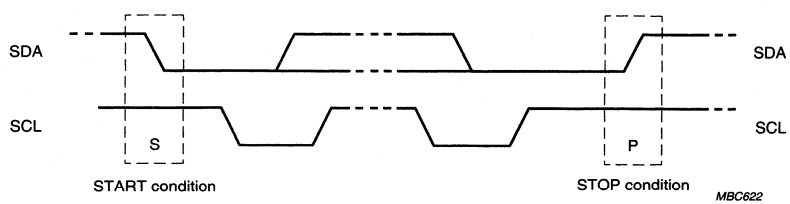


Fig.5 Definition of start and stop conditions.

System configuration (see Fig.6)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

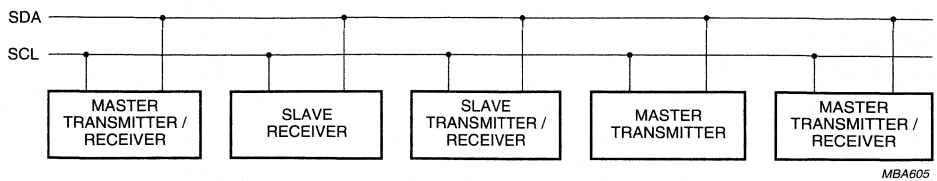


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

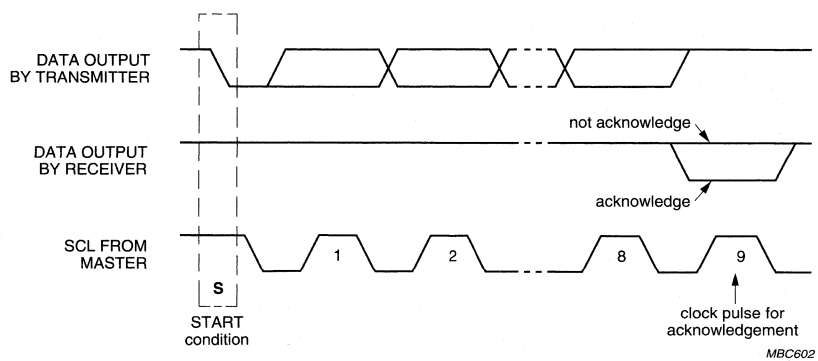


Fig.7 Acknowledgment on the I^2C-bus.

I²C-BUS PROTOCOL.

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Fig.8.

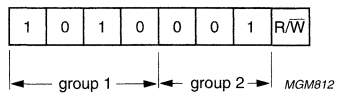


Fig.8 Slave address.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8563 READ and WRITE cycles is shown below. The word address is four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

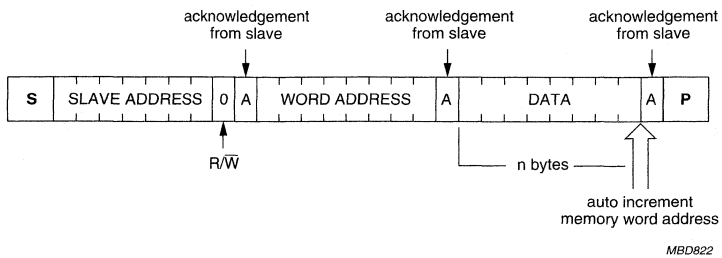


Fig.9 Master transmits to slave receiver (WRITE) mode.

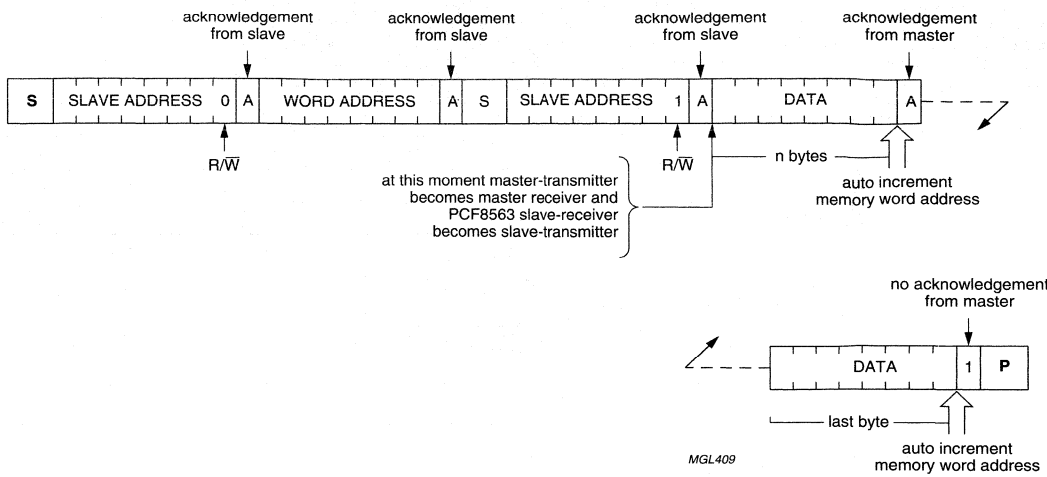


Fig.10 Master reads after setting word address (write word address; READ data).

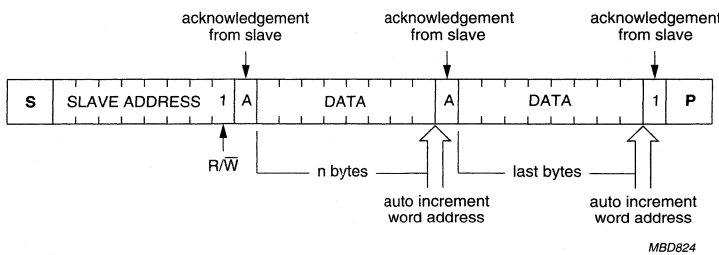


Fig.11 Master reads slave immediately after first byte (READ mode).

DC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (1)	I^2C bus inactive, 25 °C	1.0	–	5.5	V
		400 kHz I^2C bus activity	1.8	–	5.5	V
	clock data integrity	25 °C	V_{LOW}	–	5.5	V
I_{DD}	supply current (2)	f_{SCL} = 400 kHz	–	–	800	μA
		f_{SCL} = 100 kHz	–	–	200	μA
		f_{SCL} = 0 Hz V_{DD} = 5.0 V 25 °C	–	0.3	1.0	μA
		f_{SCL} = 0 Hz V_{DD} = 2.0 V 25 °C	–	0.25	0.75	μA
Inputs						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage	$V_I = V_{DD}$ or V_{SS}	−1	–	1	μA
C_I	input capacitance	(note 3)	–	–	7	pF
Outputs						
$I_{OL(SDA)}$	SDA LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−3	–	–	mA
$I_{OL(\overline{INT})}$	$\overline{INT}$ LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OL(CLKOUT)}$	CLKOUT LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OH(CLKOUT)}$	CLKOUT HIGH output current	V_{OH} = 4.6 V, V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage	$V_O = V_{DD}$ or V_{SS}	−1	–	1	μA
Voltage detector						
V_{LOW}	Low voltage detection	25 °C	–	0.9	1.0	V

Notes

1. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
2. CLKOUT disabled, (FE = 0). Timer source clock = $1/60$ Hz.
3. Tested on sample basis.

AC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_L	integrated load capacitance		19	25	31	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 200 mV; 25 °C	–	$2x10^{-7}$	–	–
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
CLKOUT output						
T_{CLKOUT}	CLKOUT duty cycle	note 1	–	50	–	%
Timing characteristics: I²C-bus; notes 5 & 6						
f_{SCL}	SCL clock frequency	note 4	–	–	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Unspecified for f_{CLKOUT} = 32.768 kHz.
2. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C bus specification, with applications, is given in brochure "The I²C bus and how to use it". This brochure may be ordered using the code 9398 393 40011.
4. I²C access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

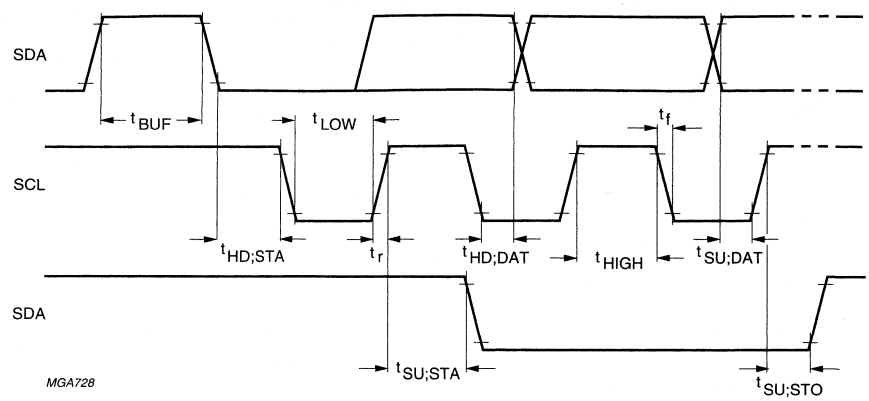


Fig.12 I²C-bus timing waveforms.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

METHOD 2: OSCI TRIMMER

Using the 32.768 kHz signal available after power-on at the CLKOUT pin fast setting of a trimmer is possible.

METHOD 3:

Direct measurement of OSCO out (accounting for test probe capacitance).

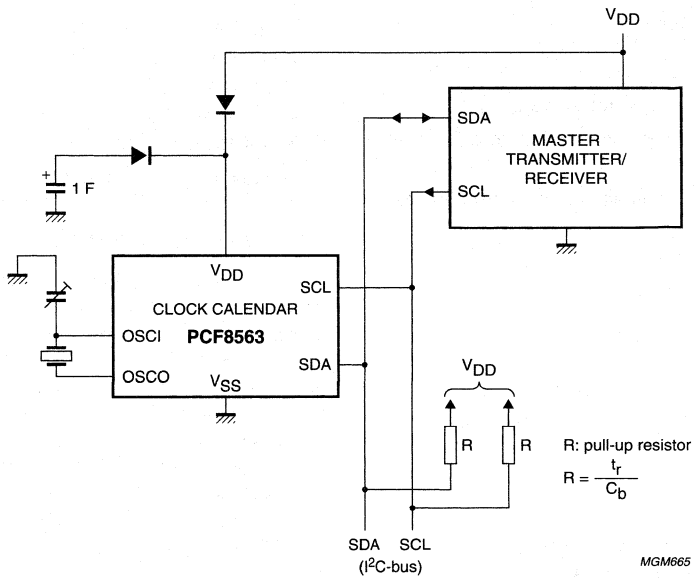


Fig.13 Application diagram.

Universal LCD driver for low multiplex rates

PCF8566

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8566P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8566T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

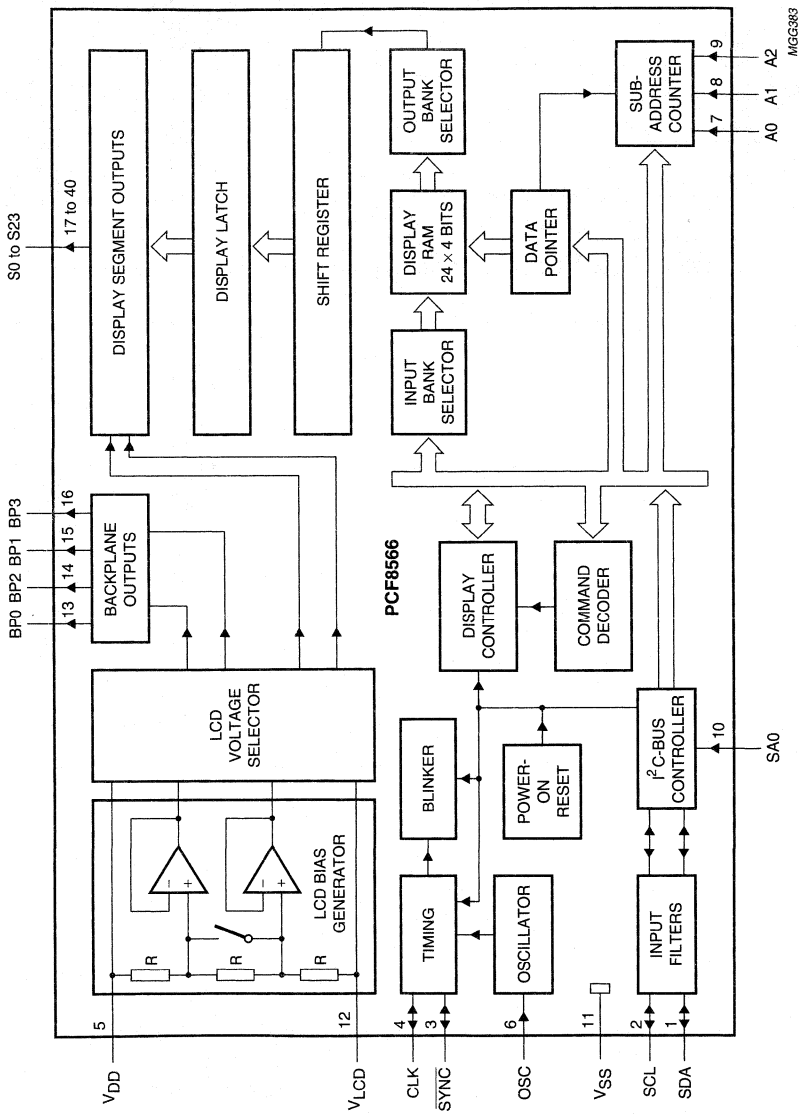


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

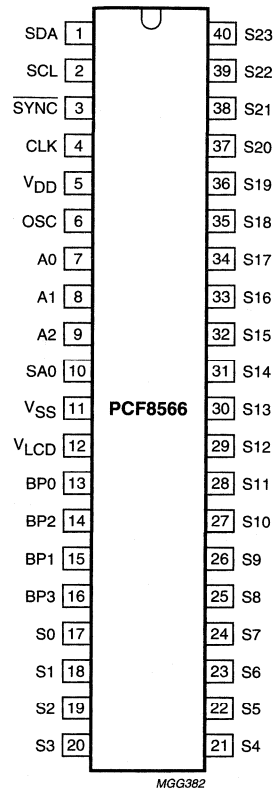


Fig.2 Pin configuration.

Universal LCD driver for low multiplex rates

PCF8576

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic very small outline package (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576U	–	chip in tray	–
PCF8576U/2	–	chip with bumps in tray	–
PCF8576U/5	–	unsawn wafer	–
PCF8576U/7	–	chip with bumps on tape	–
PCF8576U/10	FFC	chip on film frame carrier (FFC)	–
PCF8576U/12	FFC	chip with bumps on film frame carrier (FFC)	–

BLOCK DIAGRAM

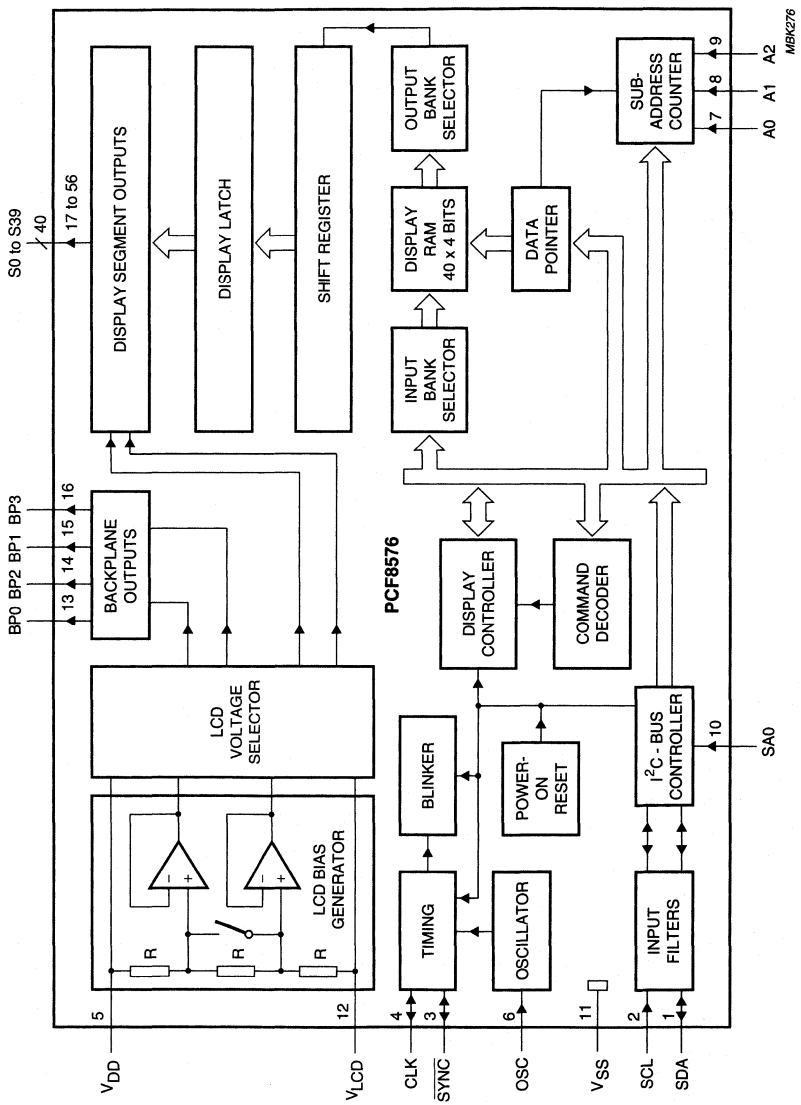


Fig.1 Block diagram (for VSO56 package; SOT190-1).

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data input/output
SCL	2	I²C-bus serial clock input
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	supply voltage
OSC	6	oscillator input
A0 to A2	7 to 9	I²C-bus subaddress inputs
SA0	10	I²C-bus slave address input; bit 0
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0, BP2, BP1 and BP3	13 to 16	LCD backplane outputs
S0 to S39	17 to 56	LCD segment outputs

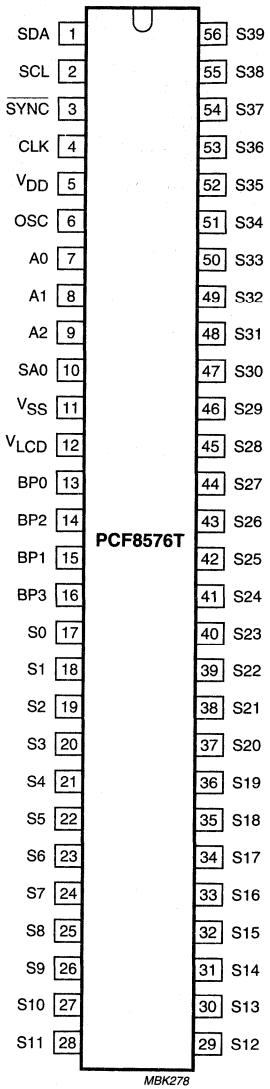


Fig.2 Pin configuration; SOT190-1.

Universal LCD driver for low multiplex rates

PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs.

  A 9 V version is also available on request.
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	chip in tray	–
PCF8576CU/2	–	chip with bumps in tray	–
PCF8576CU/5	–	unsawn wafer	–
PCF8576CU/7	–	chip with bumps on tape	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CU/12	FFC	chip with bumps on film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

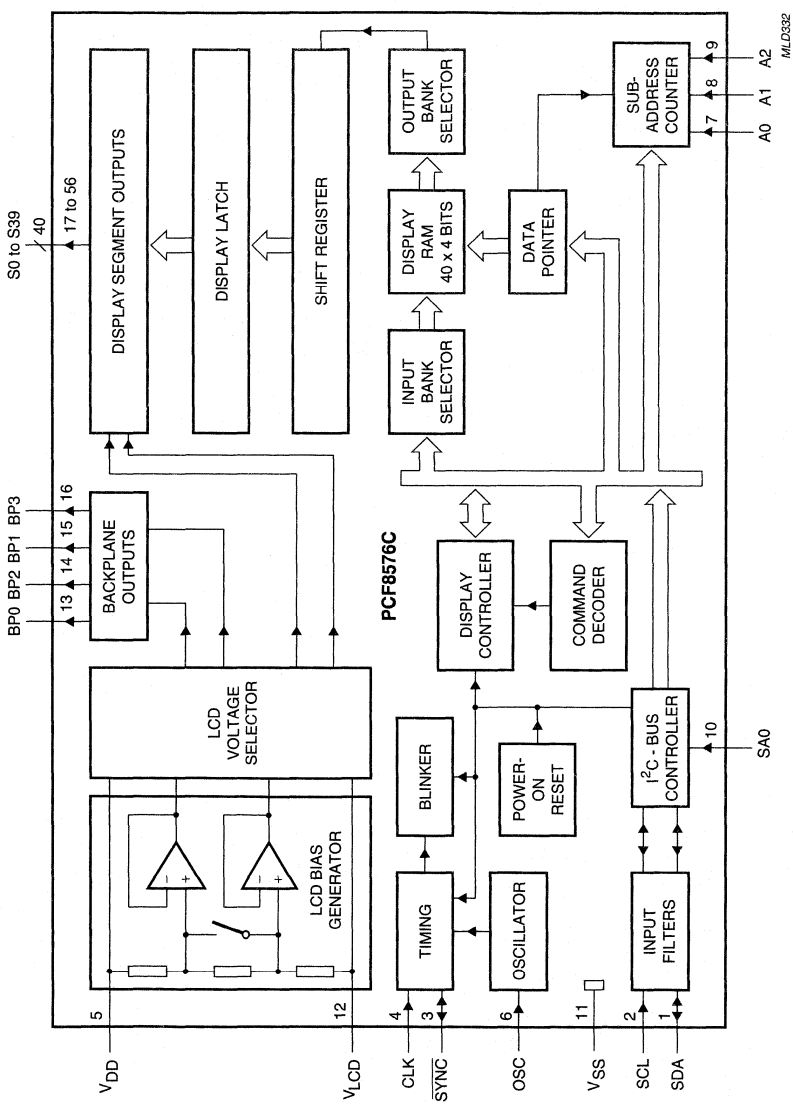


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

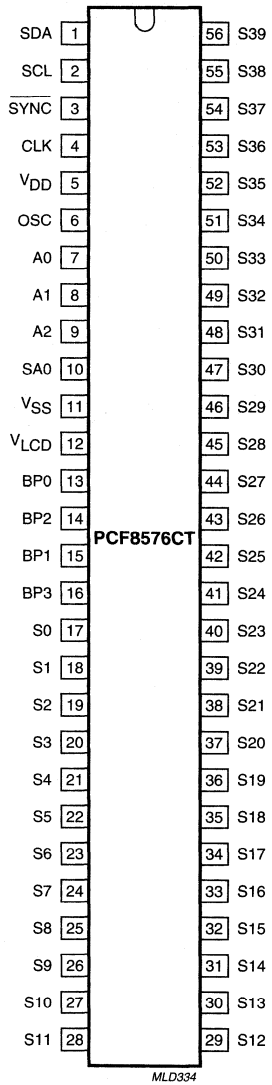


Fig.2 Pin configuration; VSO56.

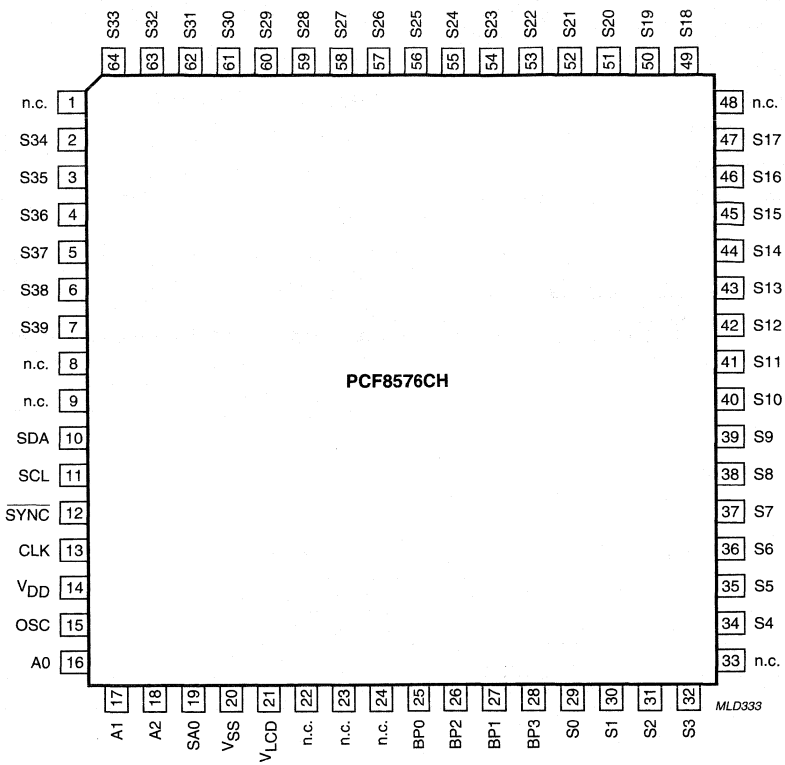


Fig.3 Pin configuration; LQFP64.

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I²C-bus address: 0111 0100.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	VS040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

BLOCK DIAGRAM

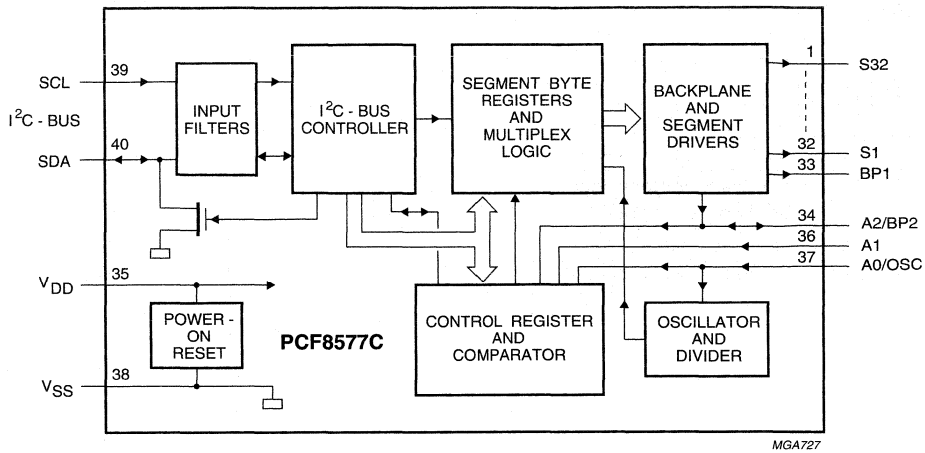


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

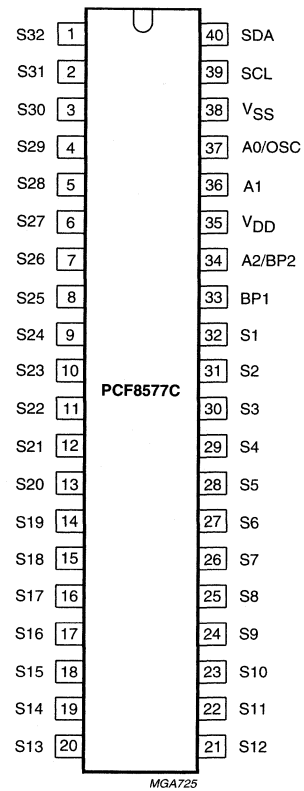


Fig.2 Pin configuration.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

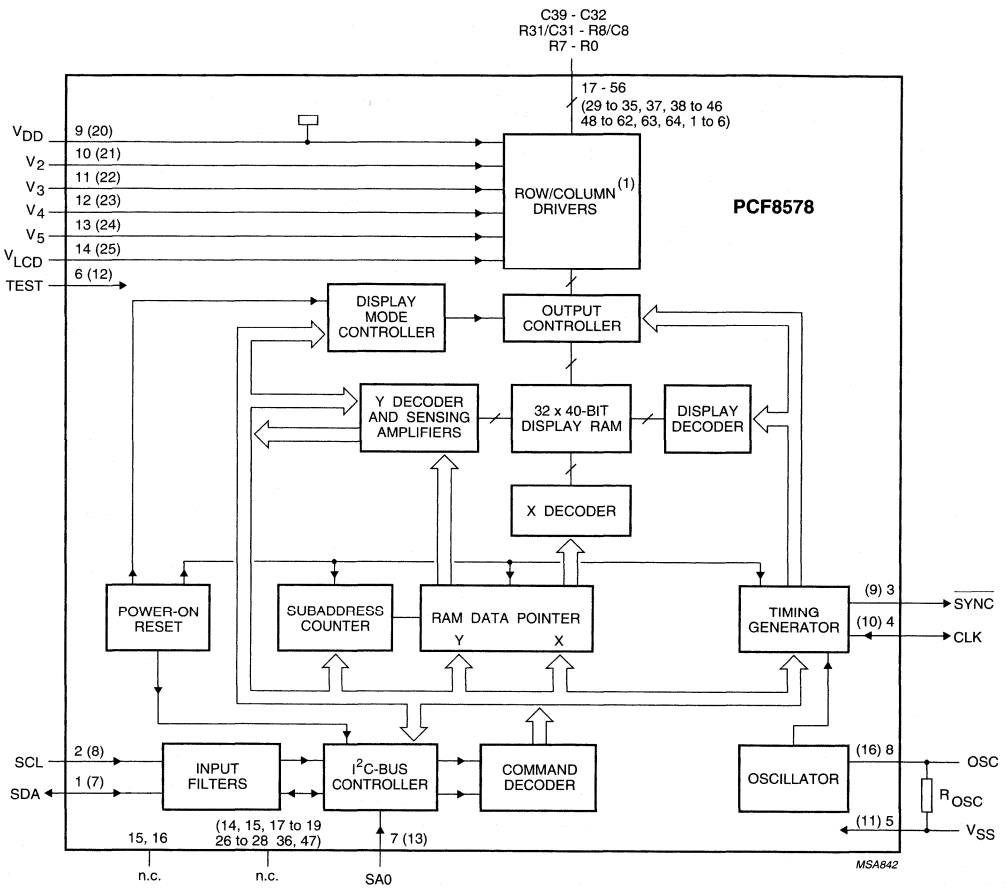
GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U/2	–	chip with bumps in tray	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

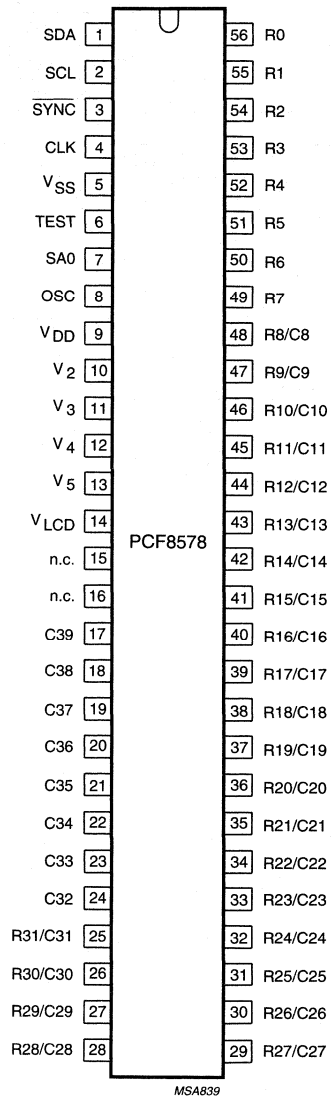


Fig.2 Pin configuration (VSO56).

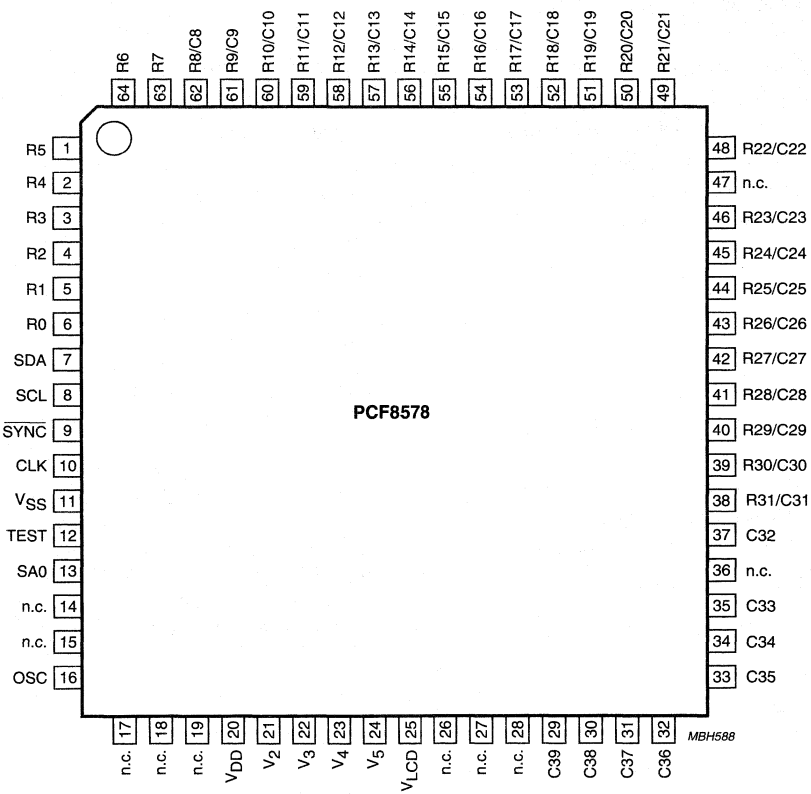


Fig.3 Pin configuration (LQFP64).

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology
- I^2C-bus address: 011110 SA0.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

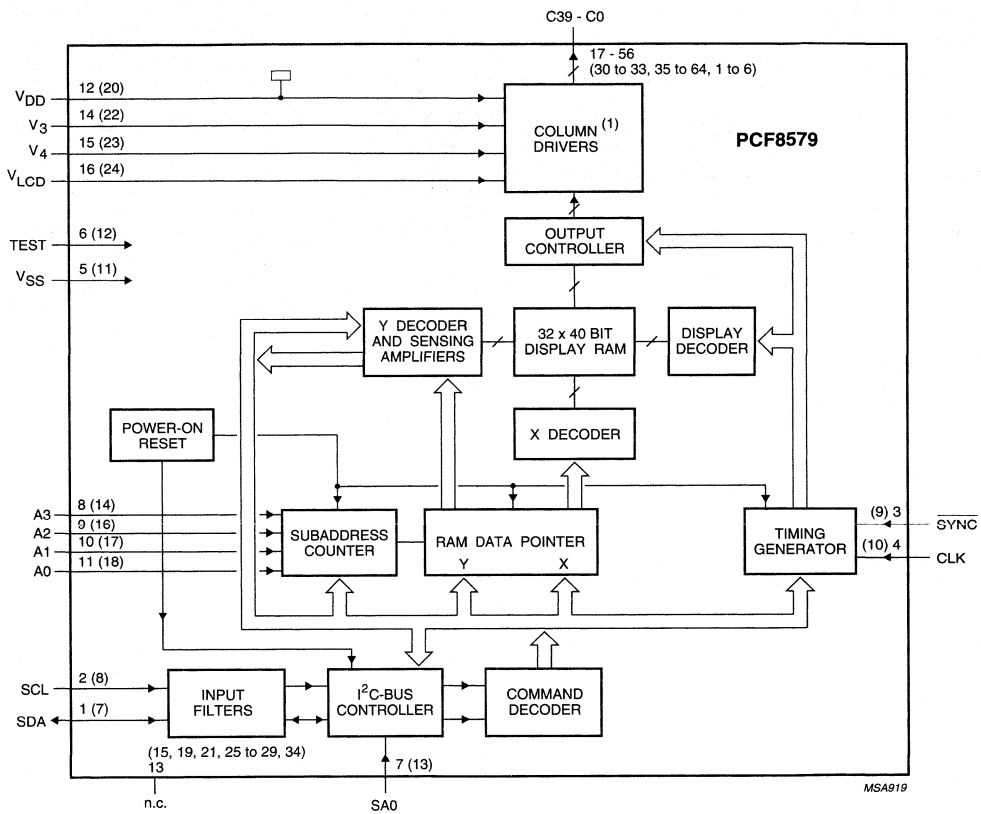
GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190
PCF8579U7	–	chip with bumps on tape	–
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I²C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13[1]	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

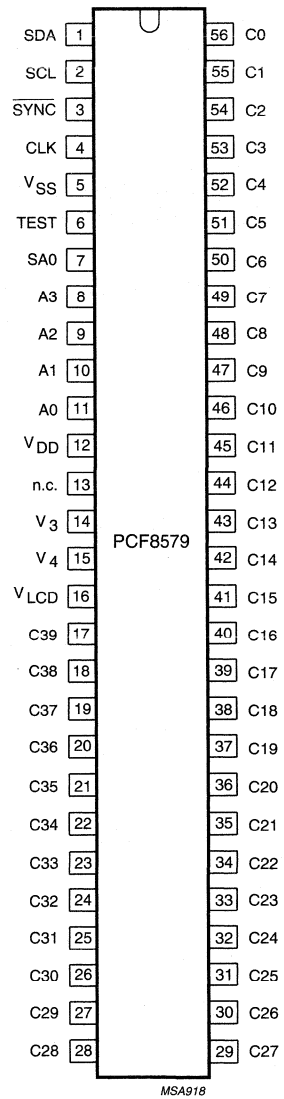


Fig.2 Pin configuration (VSO56).

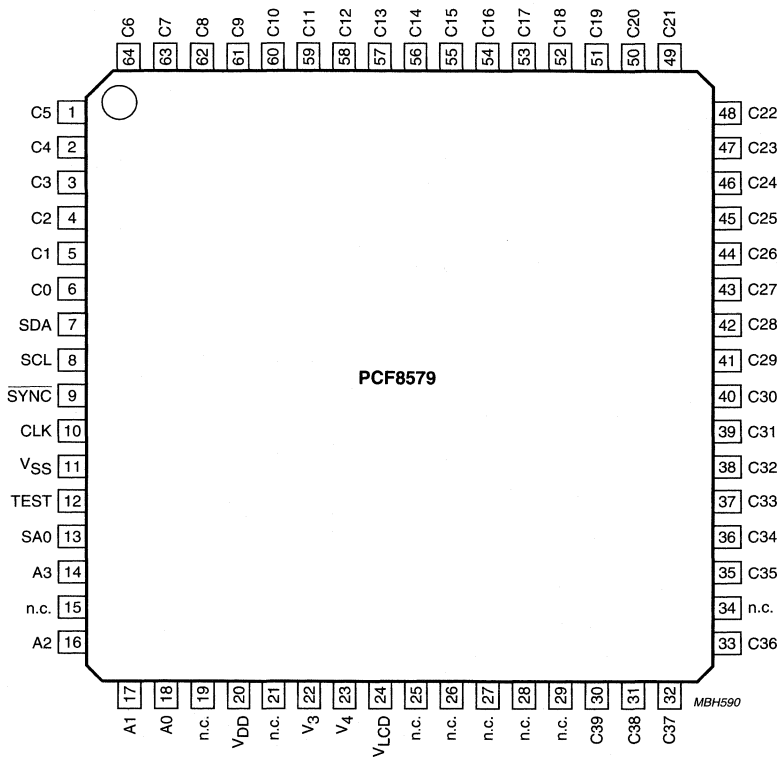


Fig.3 Pin configuration (LQFP64).

Low power clock/calendar PCF8593

CONTENTS

Low power clock/calendar PCF8593

1 FEATURES

- I^2C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{RESET}$ input resets I^2C interface (only)
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package available
- Slave address:
  - READ A3
  - WRITE A2.

2 GENERAL DESCRIPTION

The PCF8593 is a CMOS clock/calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I^2C-bus. The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I^2C-bus active	2.5	–	6.0	V
		I^2C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	–	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	–	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 BLOCK DIAGRAM

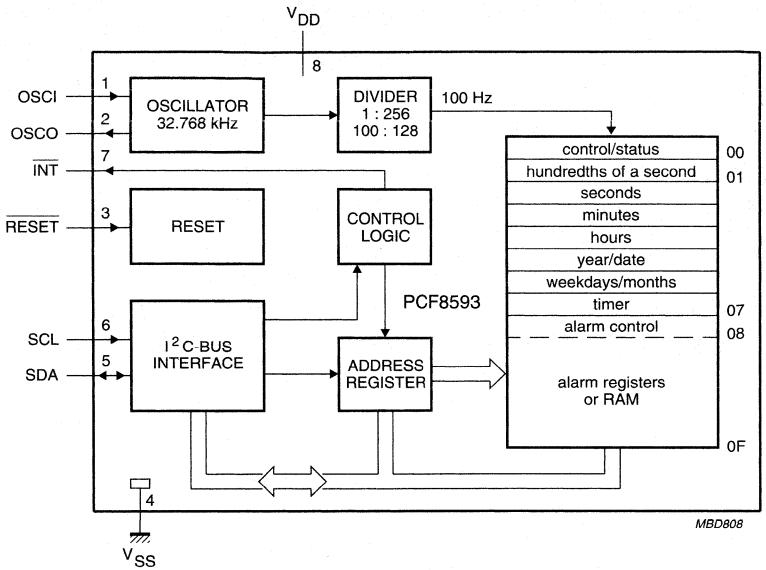


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{RESET}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

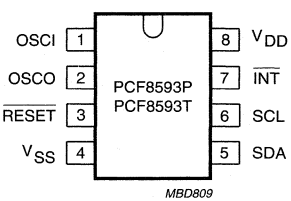


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I^2C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

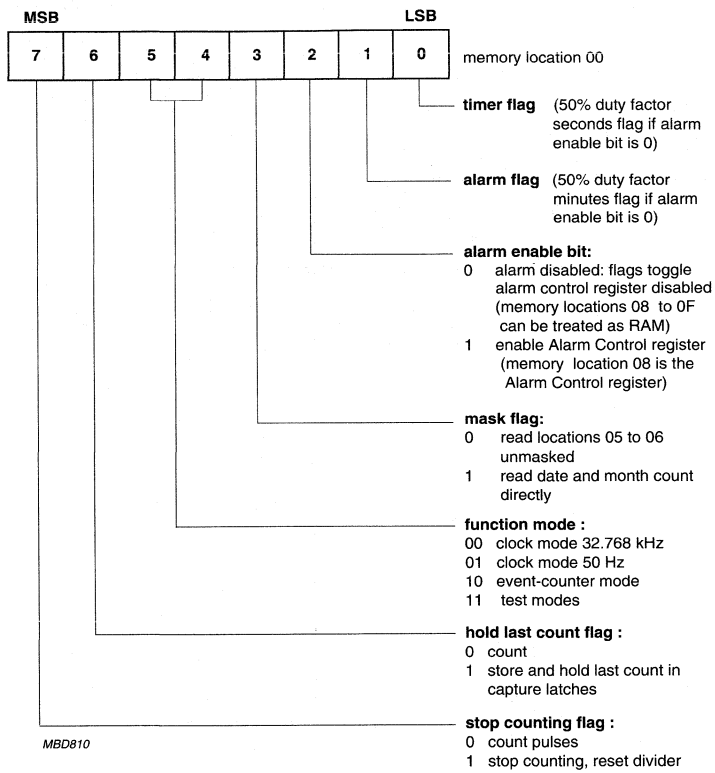


Fig.3 Control/status register.

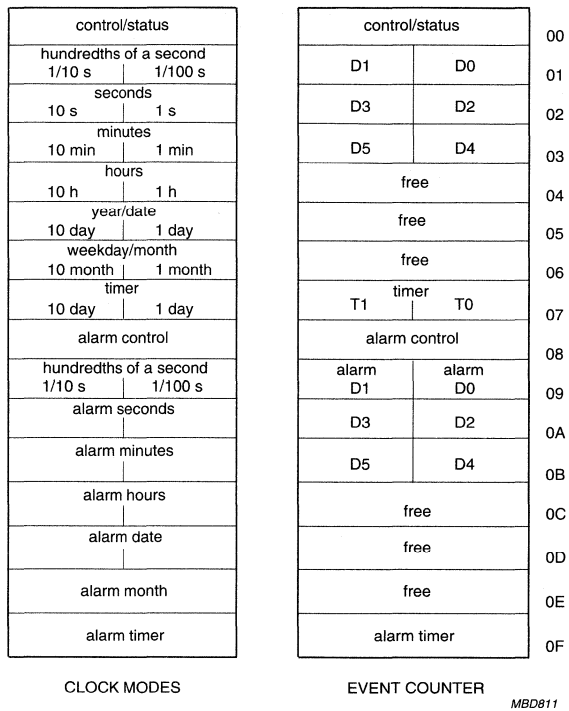


Fig.4 Register arrangement.

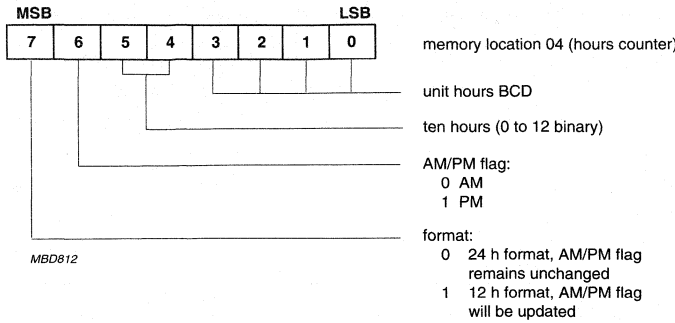


Fig.5 Format of the hours counter.

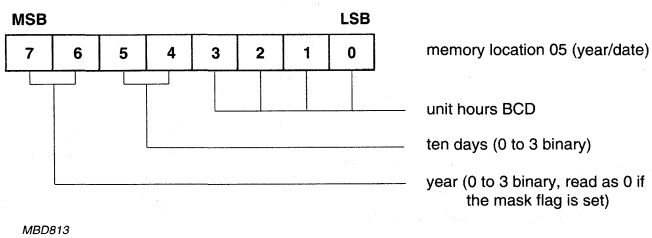


Fig.6 Format of the year/date counter.

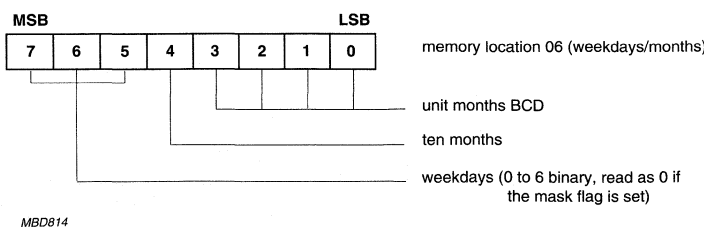


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4,Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

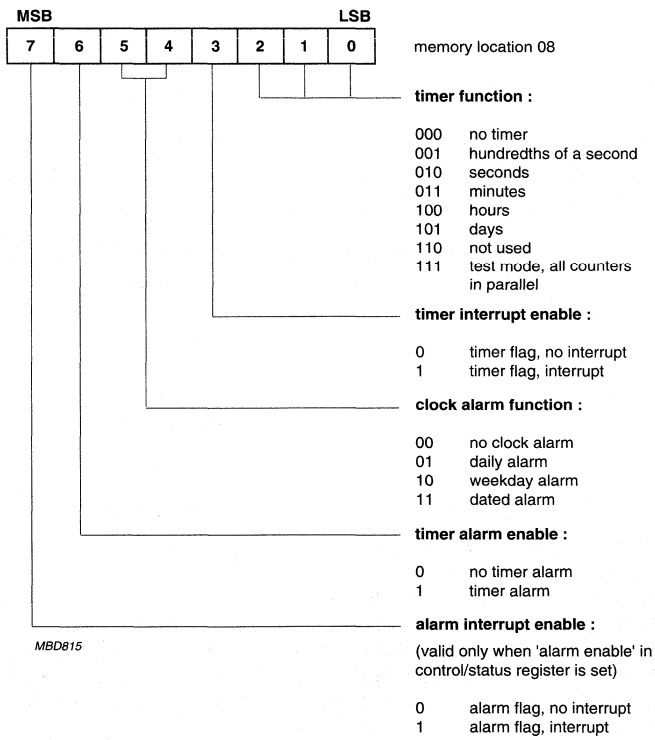


Fig.8 Alarm control register, clock mode.

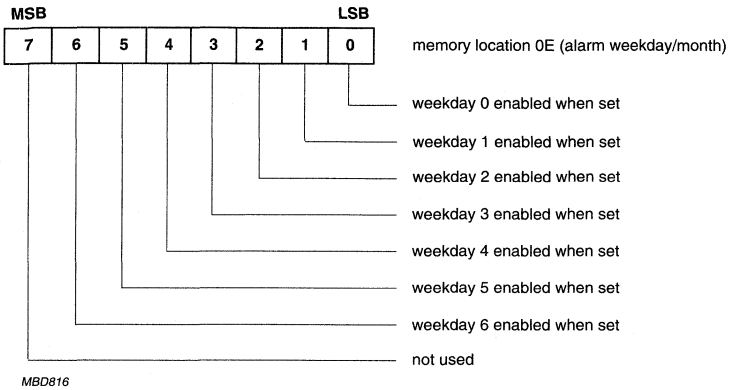


Fig.9 Selection of alarm weekdays.

7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

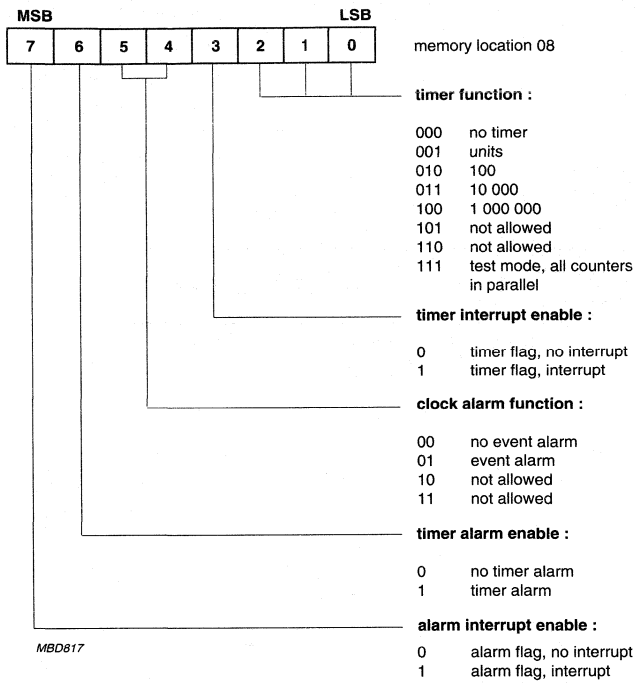
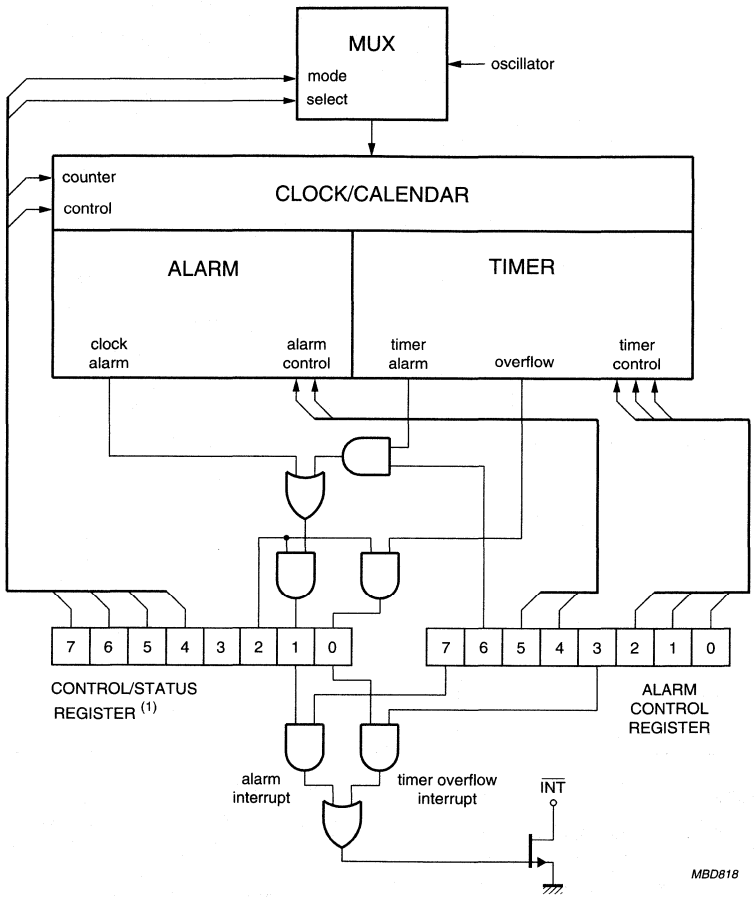


Fig.10 Alarm control register, event-counter mode.

7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter 14, Section 14.1). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

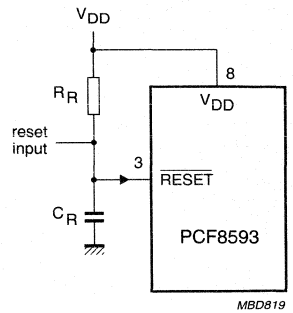
7.10.1 DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

7.11 Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs only the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2\ \mu F$. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.13)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

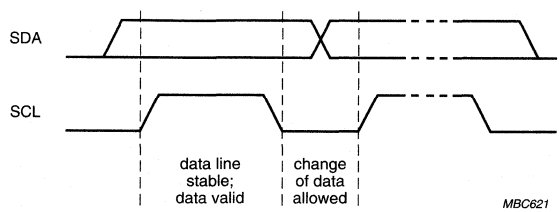


Fig.13 Bit transfer.

8.2 Start and stop conditions (see Fig.14)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

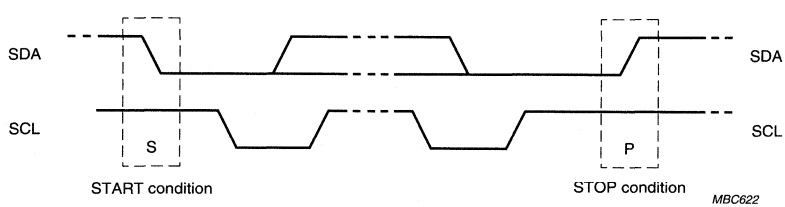


Fig.14 Definition of start and stop conditions.

8.3 System configuration (see Fig.15)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

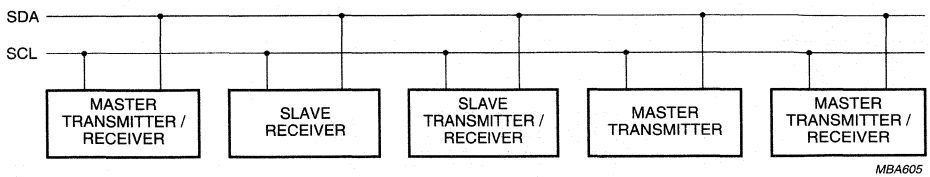


Fig.15 System configuration.

8.4 Acknowledge (see Fig.16)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

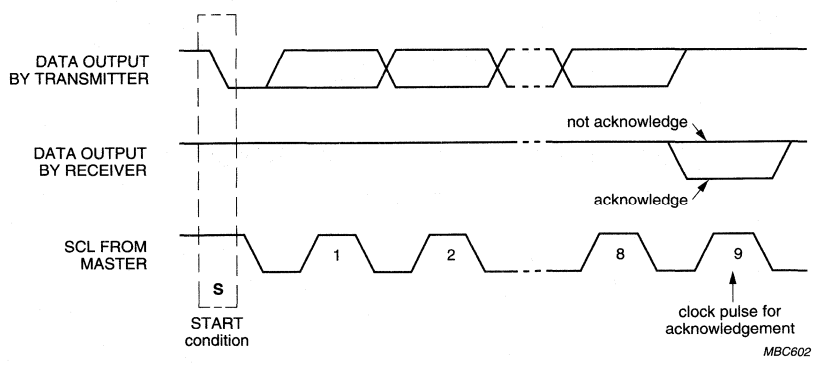


Fig.16 Acknowledgment on the I²C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock/calendar slave address is shown in Fig.17.

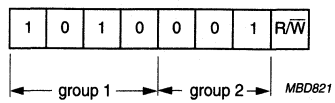


Fig.17 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 18, 19 and 20.

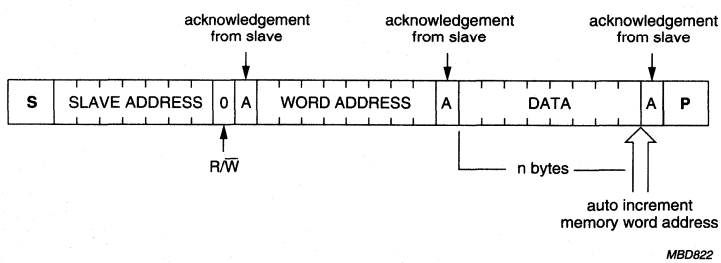


Fig.18 Master transmits to slave receiver (WRITE) mode.

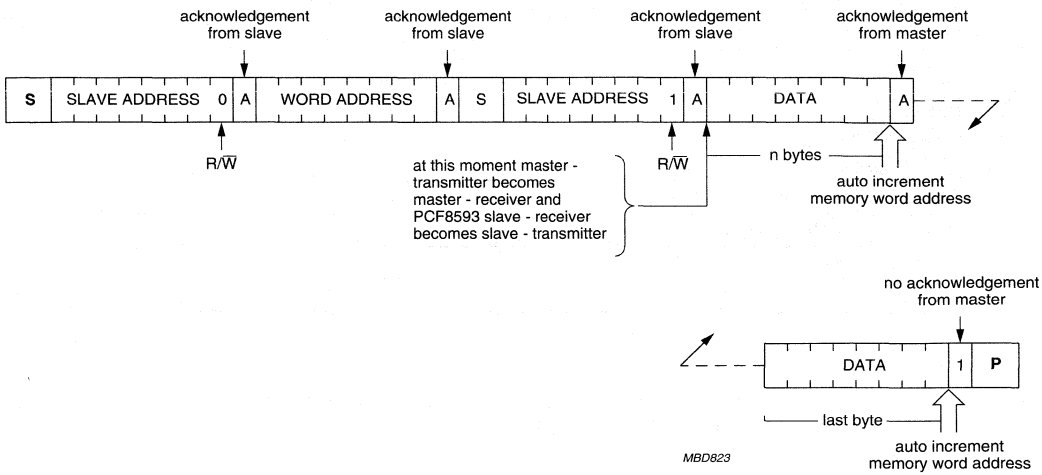


Fig.19 Master reads after setting word address (write word address, READ data).

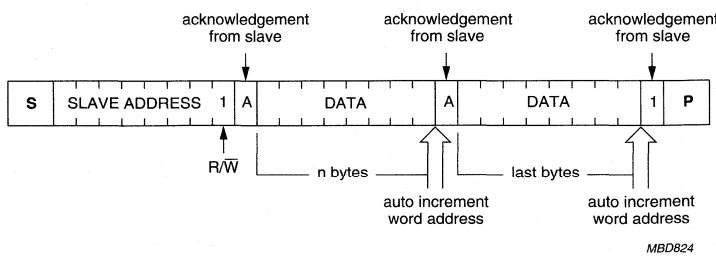


Fig.20 Master reads slave immediately after first byte (READ mode).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	−	50	mA
I_{SS}	supply current (pin 4)	−	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	input current	−	10	mA
I_O	DC output current	−	10	mA
P_{tot}	total power dissipation per package	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

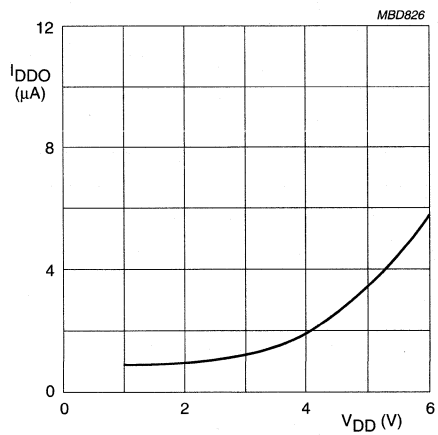
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating mode)	I²C-bus active	2.5	−	6.0	V
		I²C-bus inactive	1.0	−	6.0	V
V_{DDosc}	supply voltage (quartz oscillator)	note 2				
		T_{amb} = 0 to 70 °C	1.0	−	6.0	V
		T_{amb} = −40 to 85 °C	1.2	−	6.0	V
I_{DD}	supply current (operating mode)	f_{scl} = 100 kHz; clock mode; note 3	−	−	200	µA
I_{DDO}	supply current (clock mode with I²C-bus inactive)	f_{scl} = 0 Hz; inputs at V_{DD} or V_{SS}				
		V_{DD} = 2 V	−	1.0	8.0	µA
		V_{DD} = 5 V	−	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	−	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
C_i	input capacitance	note 4	–	–	7	pF
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_i	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at T_{amb} = 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode: supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.21 Typical supply current in clock mode as a function of supply voltage.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.22; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

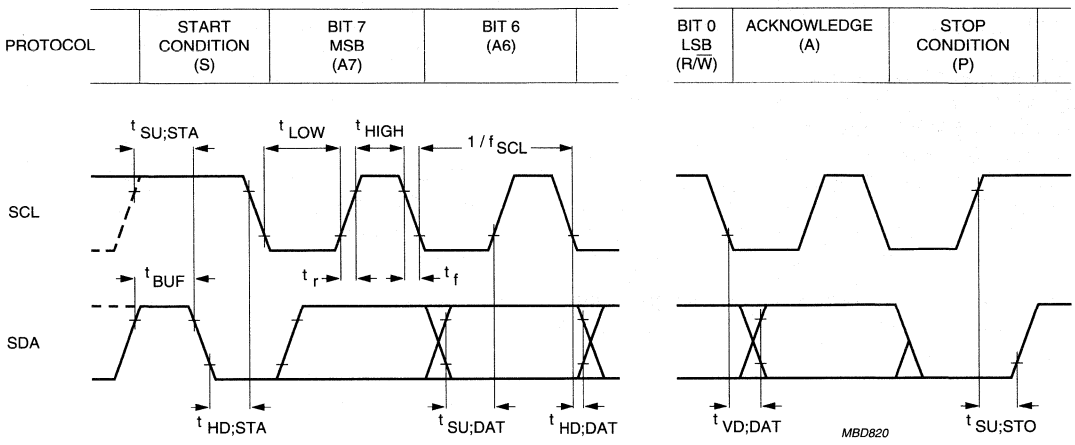


Fig.22 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

14.1 Quartz frequency adjustment

14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

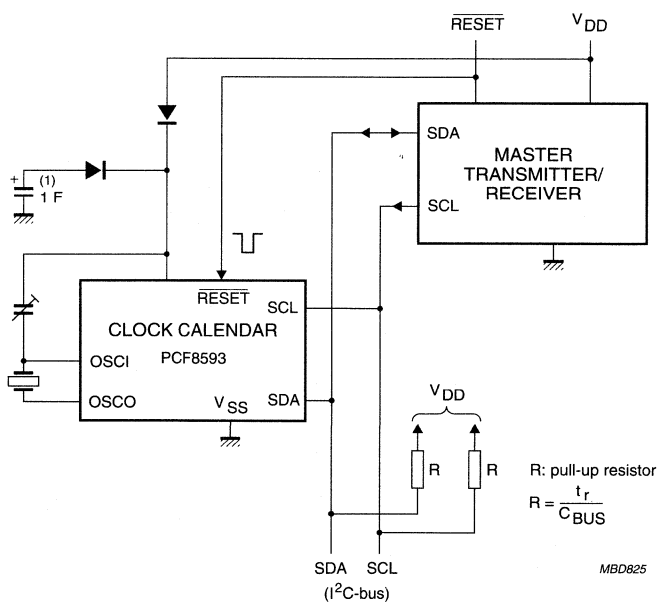
- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

14.1.3 METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).



(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

CONTENTS

1 FEATURES

- Low power and low voltage device in 0.25 micron CMOS technology; supply voltage: analog 2.7 V (typical) and digital 1.5 V (typical)
- Compatible with GSM phase 2 and DCS1800 recommendations
- Complete in-phase and quadrature component interface paths between the Digital Signal Processor (DSP) and RF circuitry
- Complete linear PCM CODEC for audio signal conversion between earphone/microphone and DSP
- Four auxiliary analog inputs for measurement purposes (e.g. battery monitoring)
- Three auxiliary analog outputs for control purposes (i.e. AFC, AGC and power ramping control)
- Separate baseband, audio and control serial interfaces
- Voice band Signal Processor (VSP) for flexible audio data processing.

2 APPLICATIONS

The CMOS integrated circuit PCF50732, Baseband and audio interface for GSM, is dedicated to wireless telephone handsets conforming to the GSM recommendations phases 1 and 2, DCS1800 and PCS1900.

3 GENERAL DESCRIPTION

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the Digital Signal Processor (DSP). It consists of three parts:

- The **receive path**, which transforms the quadrature signals from the RF (I/Q) to digital signals
- The **transmit path**, which transforms a bitstream to analog quadrature signals for the RF devices
- The digital **Baseband Serial Interface (BSI)**, which exchanges baseband data between the PCF50732 and the digital signal processor. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

The voice band CODEC is a complete analog front-end circuit. It consists of four parts:

- The **receive path**, which converts a digital signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives the analog external signal from a microphone and converts it into a digital signal
- The **Voice band Signal Processor (VSP)**, which filters the voice band data
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to an external DSP. The voice band data is coded in 16-bit linear PCM twos complement words.

The **auxiliary Analog-to-Digital Converter (ADC)** section consists of four input channels specified for battery management applications.

The **auxiliary Digital-to-Analog Converter (DAC)** section consists of three DACs for Automatic Gain Control (AGC), for Automatic Frequency Control (AFC) and for power ramping.

The **Control Serial Interface (CSI)** is used to program a set of control registers, to store the power amplifier ramping characteristics into the dedicated RAM and to transmit auxiliary ADC values to the DSP. It also controls switches, modes and power status of the different parts of the IC.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF50732H	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		1.0	1.5	2.75	V
V_{DDA}	analog supply voltage	$V_{DDA} \geq V_{DDD}$	2.5	2.7	2.75	V
I_{DDA}	analog supply current	V_{DDD} = 1.5 V; V_{DDA} = 2.7 V; RXON active	–	3.5	–	mA
P_{av}	average power consumption	V_{DDD} = 1.5 V; V_{DDA} = 2.7 V; note 1	–	15	–	mW
$I_{stb(tot)}$	total standby current		–	10	–	µA
f_{clk}	master clock frequency		–	13.0	–	MHz
T_{amb}	operating ambient temperature		–40	+27	+85	°C

Note

1. Without load on audio outputs EARP, EARN, AUXSP and BUZ.

6 BLOCK DIAGRAM

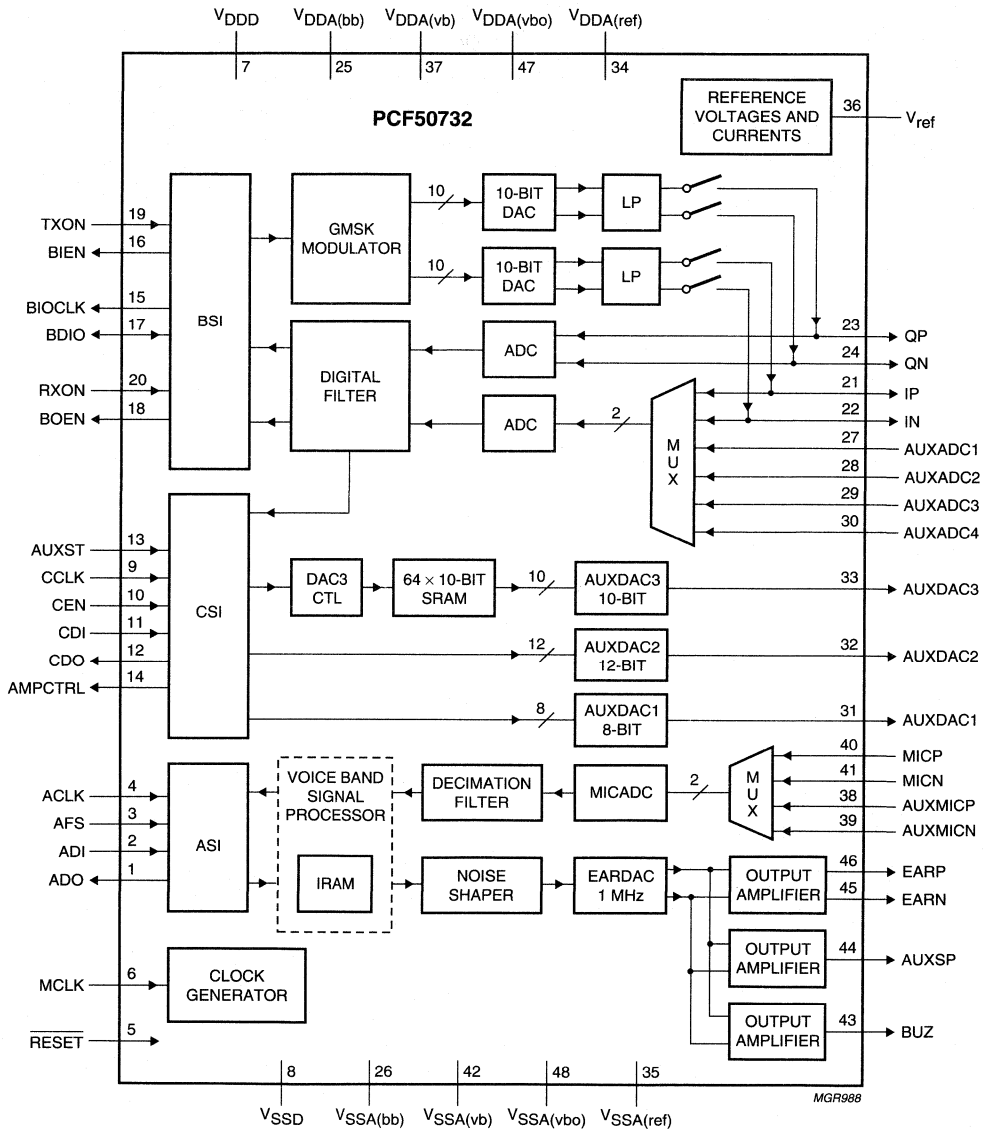


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN					DESCRIPTION
	NR.	TYPE[1]	ACTIVE LEVEL	ACTIVE EDGE	I_{DD}	
ADO	1	O/TS	–	–	1.5 mA	audio digital interface PCM data output to DSP
ADI	2	I	–	–	–	audio digital interface PCM data input from DSP
AFS	3	I	–	rising	–	audio digital interface PCM frame synchronization signal from DSP
ACLK	4	I	–	rising	–	audio digital interface PCM clock signal from DSP
$\overline{RESET}$	5	I	LOW	–	–	asynchronous reset input
MCLK	6	I	–	rising	–	low-swing master clock input; f_{clk} = 13 MHz; integrated capacitive coupling
V_{DDD}	7	P	–	–	–	digital power supply
V_{SSD}	8	G	–	–	–	digital ground
CCLK	9	I	–	falling	–	control bus clock input from DSP
CEN	10	I	LOW	–	–	control bus data enable from DSP
CDI	11	I	–	–	–	control bus data input from DSP
CDO	12	O/TS	–	–	1.5 mA	control bus data output to DSP
AUXST	13	I	HIGH	–	–	status control signal for activation of AUXDAC1, AUXDAC2 and MCLK input
AMPCTRL	14	O	–	–	1.5 mA	general purpose output pin
BIOCLK	15	O/TS	–	–	3 mA	baseband interface data clock
BIEN	16	O	LOW	–	1.5 mA	baseband transmit interface data enable signal
BDIO	17	I/O	–	–	1.5 mA	baseband interface data I/O from/to DSP
BOEN	18	O	LOW	–	1.5 mA	baseband receive interface data enable signal
TXON	19	I	HIGH	–	–	baseband transmit path activation signal
RXON	20	I	HIGH	–	–	baseband receive path activation signal
IP	21	I/O	–	–	–	(I) baseband differential positive input/output to IF circuit
IN	22	I/O	–	–	–	(I) baseband differential negative input/output to IF circuit
QP	23	I/O	–	–	–	(Q) baseband differential positive input/output to IF circuit
QN	24	I/O	–	–	–	(Q) baseband differential negative input/output to IF circuit
$V_{DDA(bb)}$	25	P	–	–	–	baseband power supply (analog)
$V_{SSA(bb)}$	26	G	–	–	–	baseband ground (analog)
AUXADC1	27	I	–	–	–	auxiliary ADC input 1 for battery voltage measurement
AUXADC2	28	I	–	–	–	auxiliary ADC input 2
AUXADC3	29	I	–	–	–	auxiliary ADC input 3
AUXADC4	30	I	–	–	–	auxiliary ADC input 4
AUXDAC1	31	O	–	–	–	auxiliary DAC output for AGC; max. load 50 pF // 2 kΩ
AUXDAC2	32	O	–	–	–	auxiliary DAC output for AFC; max. load 50 pF // 10 kΩ

SYMBOL	PIN					DESCRIPTION
	NR.	TYPE[1]	ACTIVE LEVEL	ACTIVE EDGE	I_{DD}	
AUXDAC3	33	O	–	–	–	auxiliary DAC output for power ramping; maximum load 50 pF, ±600 μA
$V_{DDA(ref)}$	34	P	–	–	–	reference voltage power supply (analog)
$V_{SSA(ref)}$	35	G	–	–	–	reference voltage ground (analog)
V_{ref}	36	I/O	–	–	–	band gap reference voltage noise decoupling
$V_{DDA(vb)}$	37	P	–	–	–	voice band voltage power supply
AUXMICP	38	I	–	–	–	auxiliary microphone differential positive input
AUXMICN	39	I	–	–	–	auxiliary microphone differential negative input
MICP	40	I	–	–	–	microphone differential positive input
MICN	41	I	–	–	–	microphone differential negative input
$V_{SSA(vb)}$	42	G	–	–	–	voice band ground
BUZ	43	O	–	–	–	buzzer output
AUXSP	44	O	–	–	–	auxiliary speaker output
EARN	45	O	–	–	–	earphone differential negative output
EARP	46	O	–	–	–	earphone differential positive output
$V_{DDA(vbo)}$	47	P	–	–	–	voice band output buffer voltage power supply (analog)
$V_{SSA(vbo)}$	48	G	–	–	–	voice band output buffer ground (analog)

Note

1. O/TS = 3-state output.

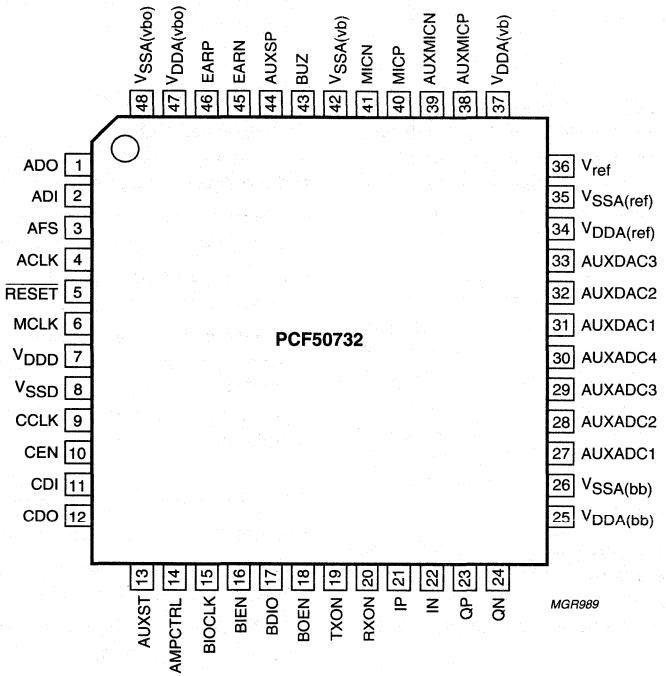


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

This chapter gives a brief overview of the device. The detailed functional description can be found in the following chapters:

Chapter 9 "Baseband CODEC"

Chapter 10 "Voice band CODEC"

Chapter 11 "Auxiliary functions"

Chapter 12 "Control Serial Interface (CSI)"

Chapter 13 "Voice band Signal Processor (VSP)".

8.1 General

As low power consumption in mobile telephones is a very important issue, all the circuit parts in the PCF50732 can be powered-on/off either by means of the external signals AUXST, TXON or RXON, or by programming the respective register bits in the Control Serial Interface (CSI).

The most important signal for the digital and analog circuit functions in the PCF50732 is the DAC enable signal AUXST, which allows to activate AUXDAC1 (AGC) and AUXDAC2 (AFC), as well as the low-swing master clock input MCLK. AUXST must be active (HIGH) and **V_{DDA} must be stable** (see also Section 18.1) to allow the master clock to access different circuit parts after a reset ($\overline{\text{RESET}}$ active). AUXDAC1 and AUXDAC2 are only activated if their related power-on bit is set. AUXDAC1 is default off, AUXDAC2 is default on.

$\overline{\text{RESET}}$ must be active during at least 3 MCLK cycles, with AUXST active, to ensure a correct initialisation of all the digital circuitry of the PCF50732. Since $\overline{\text{RESET}}$ is asynchronous even small spikes of a few nanoseconds can cause partial resets.

For power supply noise interference reduction, a pair of power supply and ground pins are provided for the:

- Baseband analog: $V_{DDA(bb)}/V_{SSA(bb)}$
- Voice band analog: $V_{DDA(vb)}/V_{SSA(vb)}$
- Voice band output drivers: $V_{DDA(vbo)}/V_{SSA(vbo)}$
- DC reference voltages and currents: $V_{DDA(ref)}/V_{SSA(ref)}$
- Digital circuitry: V_{DDD}/V_{SSD}.

All V_{SS} pins are connected internally. V_{DDD} is the digital supply. $V_{DDA(bb)}$, $V_{DDA(vb)}$, $V_{DDA(vbo)}$, and $V_{DDA(ref)}$ are analog supplies, and are referred to as V_{DDA} throughout this document. These analog supplies must be connected externally.

8.2 Baseband and voice band reference voltages

The reference voltage V_{ref} is generated on-chip by a band gap voltage reference circuit and is available at pin V_{ref}.

As V_{ref} is used as reference for most of the internal analog circuitry, noise must be kept as low as possible by connecting an external decoupling capacitor at this pin.

The voltage at V_{ref} is buffered to generate the baseband and voice band reference voltage V_{ref} as well as internal references for the different functions, such as the auxiliary and the transmit DACs.

9 BASEBAND CODEC

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the digital signal processor. It consists of three parts:

- The **transmit path**, which converts a bitstream to analog quadrature signals for the RF devices
- The **receive path**, which transforms the quadrature signals of the IF chip (I/Q) to digital signals
- The digital **baseband serial interface**, which exchanges baseband data between the PCF50732 and the DSP. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

9.1 Baseband transmit path

The baseband transmit path consists of three parts:

- **GMSK modulator:** generation of a Gaussian Minimum Shift Keying (GMSK) signal
- **10-bit DACs:** digital-to-analog converters for the I and Q components of the GMSK signal
- **Low-pass filters:** analog reconstruction low-pass filters for the output of the DACs.

The requirements of the transmit path of a GSM terminal are given by *"GSM recommendation 05.05"*:

- Phase RMS error <5°
- Phase peak error <20°
- Amplitude error < ±1 dB.

Nevertheless the performance of the PCF50732 is far better than these figures indicate; see Section 18.1.

9.1.1 GMSK MODULATOR

The input signal of the GMSK modulator is a bitstream coming from the baseband serial interface, with a sampling frequency of 270.833 kHz. Typically 148 bits are modulated during a normal burst, and 88 bits during an access burst. Using this bitstream, the GMSK modulator generates digital I and Q components as described in *"GSM recommendation 05.04"*.

This is done in three steps:

1. First the incoming bitstream is differentially encoded by an EXOR operation on the actual bit and the previous bit
2. The instantaneous phase (φ) is calculated using a gaussian filter with an impulse response of 4 taps
3. A look-up table provides the cosine (I component) and the sine values (Q component) of the phase (φ).

   The look-up table also interpolates the signal to a 16 times higher frequency (4.333 MHz).

9.1.2 10-BIT DACS

The two 10-bit DACs are working at a sampling rate of 4.3333 MHz. They convert the digital I and Q components of the GMSK modulator to differential analog I and Q signals.

9.1.3 LOW-PASS FILTER

The analog output signals of the DACs are filtered by analog reconstruction low-pass filters.

These filters remove high frequency components of the DAC output signals and attenuate components around the 4.3333 MHz sampling frequency. The low-pass filters have a cut-off frequency of approximately 300 kHz, with very linear phase behaviour in the pass band.

9.2 Baseband receive path

The baseband receive path consists of two parts:

- **Receive ADC:** $\Sigma\Delta$ analog-to-digital converters
- **Decimation filter**: digital decimation filters for I and Q.

The baseband receive section can be switched between two modes of operation:

- ZIF (zero IF) mode for radio sections, which convert the receive signal down to baseband. In this mode the ADC is sampled at 6.5 MHz, the decimation filter samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers 2×12-bit values for I and Q components at 270.833 kHz.
- NZIF (near zero IF) mode for radio sections, which converts the receive signal down to a centre frequency of 100 kHz. In this mode the ADC is sampled at 13 MHz, the decimation filter samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers 2×12-bit values for I and Q components at 541.667 kHz.

9.2.1 RECEIVE ADC

The receive ADCs are $\Sigma\Delta$ analog-to-digital converters that convert differential input signals into1-bit data streams with a sampling frequency of 6.5 or 13 MHz.

9.2.2 DIGITAL DECIMATION FILTER

Digital filtering is required for:

- Suppression of out-of-band noise produced by the $\Sigma\Delta$ ADC
- Decimation of the sampling rate (6.5 or 13 MHz) by 24
- System level filtering.

The digital filtering is performed by a digital FIR filter with a group delay for this running average filter of approximately 23 or 11.5 μs respectively. The filter uses twos complement arithmetic.

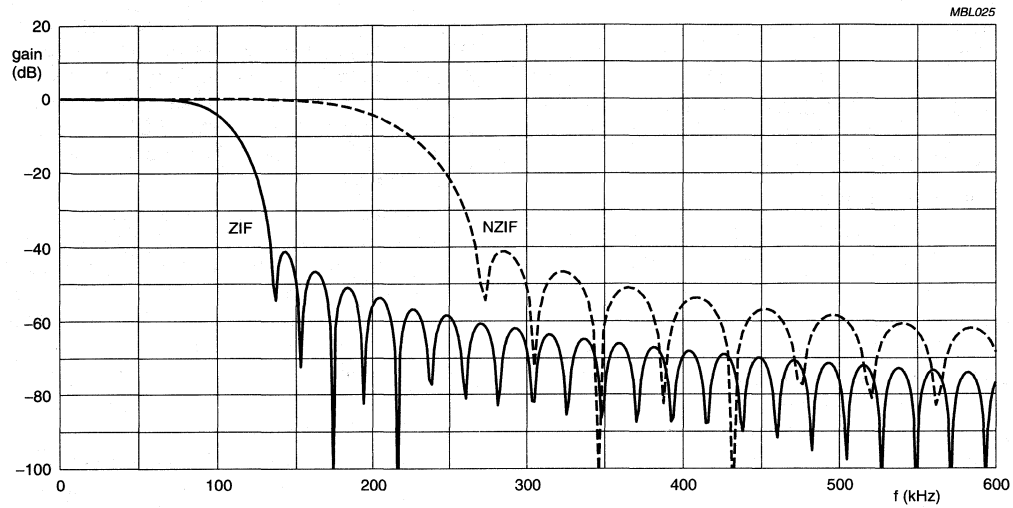


Fig.3 Transfer functions for the baseband receive filter.

9.3 Baseband Serial Interface (BSI)

9.3.1 Overview

The digital part of the baseband consists of a receive section and a transmit section. The receive section is a FIR filter that reduces the 6.5 MHz (13 MHz for NZIF mode) bitstream from the sigma-delta converters into 2 × 12-bit values at 270.833 kHz (541.667 kHz for NZIF mode).

The transmit section converts the 270.833 kHz data stream from the DSP into a GMSK signal sampled at 4.333 MHz. The 10-bit I and Q signals are then fed into two 10-bit DACs. The power ramping signal is also generated by the transmit section with the 10-bit AUXDAC3 block.

9.3.2 Transmit path block description

9.3.2.1 Transmit serial interface

The power-up of the BSI transmit path is controlled via the TXON pin. When TXON is pulled HIGH, the transmit path recovers from power-down. The MCLK/48 = 270.833 kHz output signal BIOCLK is activated. When the BIEN0 period has elapsed the output signal BIEN goes LOW and the bits to be transmitted are clocked out of the DSP.

BIEN0 must be at least 10 quarterbits long to allow settling of the analog filters. Bits are clocked out of the DSP by the falling edge and clocked into the PCF50732 by the rising edge of BIOCLK. After the BIEN1 period has elapsed, BIEN is set HIGH again and transmission from the DSP ends. Logic 1s are modulated whenever BIEN is HIGH and the baseband transmit (BBTX) block is active. Values for BIEN0 and BIEN1 can be set in the Burst control register.

Figure 5 shows the timing for the BSI data transmission. In power-down the de-asserted value of BIOCLK is high-Z and BIEN is HIGH. Typical connection to the system DSP is defined in Table 1.

Table 1 Connection of BSI transmit signals to PCF5087X

PCF50732		PCF5087X	
PIN	**I/O**	**PIN**	**I/O**
TXON	I	RFSIG[y]	O
BDIO	I/O	SIOXD	I/O
BIEN	O	SOXEN_N	I
BIOCLK	O	SIOXCLK	I

9.3.2.2 Power ramping controller

The PCF50732 fully supports all multislot modes which do not require full duplex operation or more than two consecutive transmit bursts. In this specification double burst mode is used for all supported multislot modes while single burst mode supports the normal GSM modes.

The power ramping controller drives the power amplifier output envelope.

In each transmit (TX) burst one ramp-up and one ramp-down will be carried out. In multislot mode one intermediate ramp will be carried out in addition to ramp-up and ramp-down. Each ramp consists of 16 discrete step values that are sent to the DAC3. Each step's duration is 2 quarterbits which translates into 8-bit long ramps. The DAC3 output is in 3-state whenever it is powered down. The ramping step values are stored in a 64 × 10-bit RAM as shown in Table 2.

In order to initialize AUXDAC3 it is necessary to write into the RAM all 32 (or 48 in multislot mode) DAC3 output values. Filling the RAM is normally done by writing a logic 0 to the address sub-register of the Burst control register, after which 32 or 48 values, depending on multislot mode, can be written into the data sub-register of the Burst control register. Writing to the DAC3 RAM is only possible when the DAC3 is powered off.

Total number of CSI-accesses is therefore 33 for a normal burst and 49 for a double burst.

An autoincrement feature will store these data into the correct RAM positions.

The value after power-up of DAC3 will always be equal to the value of RAM location 47.

AUXDAC3 timing is controlled by the Burst control register. This contains the following sub-registers:

- The **RU register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-up ramping; default value is 0
- The **RM register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the intermediate power ramp; default value is 0. RM is only used in case of multislot mode
- The **RD register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-down ramping; default value is 0
- DAC3 burst RAM address register
- DAC3 burst RAM data register
- Single/double burst mode register: normal mode or multislot mode selection flag.

After TXON goes HIGH and a time equal to RU quarterbit periods has elapsed, power ramp-up is done.

After a time period equal to RD quarterbits has elapsed power ramp-down is initiated.

The AUXDAC3 output is also shown in Fig.4.

Values for RU (ramp-up) and RD (ramp-down) can be set in the Burst control register of the control serial interface. RD must be greater than RU + 32. RU and RD range from 0 to 4000 QB (quarterbit). The register offers the possibility to enter codes up to 4095.

The GMSK modulator is active for a period of 2 clock cycles after the ramp-down or for the length of the TXON burst, whichever is longer.

Multislot (high speed switched data mode) can be selected by setting the appropriate bit in the Burst control register. In multislot mode an intermediate ramping step is done. This intermediate step is started after a time period equal to RM quarterbits has elapsed. A value for RM (intermediate ramp) is also set using the Burst control register. The following conditions must be true:

RU + 32 < RM and RM + 32 < RD.

Table 2 AUXDAC3 RAM contents

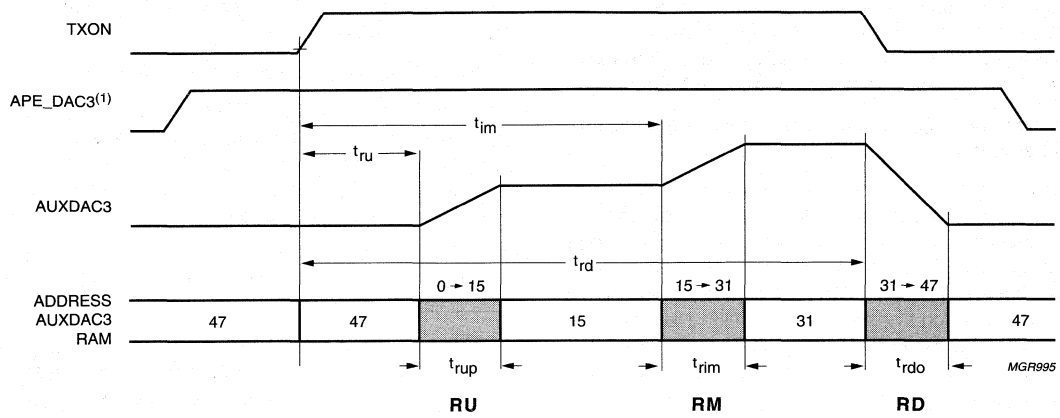
RAM ADDRESS	DATA
0 to 15	ramp-up data
16 to 31	intermediate ramp data
32 to 47	ramp-down data
48 to 64	not used

Table 3 Power ramping timing characteristics

SYMBOL	VALUE	COMMENTS(1)
t_0	$12t_1$	one quarterbit (QB)
t_{ru}	RU register	0 to 4000 QB
t_{im}	RM register	RU + 32 to 4000 QB
t_{rd}	RD register	RM + 32 to 4000 QB
t_{rup}, t_{rim}, t_{rdo}	$32t_0$	8 bits; 32 QB

Note

1. QB: Quarterbit, usually referred to the time needed for one quarter of a GSM baseband bit, i.e. a frequency of $^1/_{12} \times 13$ MHz.



(1) APE_DAC3: Analog Power Enable signal for the AUXDAC3.

Fig.4 Power ramping timing characteristics (multislot mode).

9.3.3 Receiver path block description

9.3.3.1 Receive serial interface

The baseband serial interface sends the digital signal of the receive path to a digital signal processor. It also takes the digital bitstream from the digital signal processor and transmits it via the baseband CODEC.

The baseband reception and transmission are active in bursts. A normal burst has a length of 548 µs. The frame rate of bursts is 4.615 ms. Using a normal traffic channel, one burst for each frame is transmitted and two bursts are received. To save as much power as possible, the transmit path and the receive path of the PCF50732 are in power-up mode only during the transmission or reception bursts respectively.

The power-up of the receive section is controlled via the RXON pin or RXON bit. When RXON is driven HIGH, the receive section recovers from power-down and the output clock BIOCLK is activated. After a settling delay of 52 µs (ZIF mode, analog circuitry + decimation filter settling time), BOEN goes LOW to transfer the first 12-bit I and Q words. The settling time is only 26 µs in NZIF mode.

Bits are clocked out of the PCF50732 by the falling edge, and clocked into the DSP by the rising edge of BIOCLK. In normal bursts 148 I/Q pairs are read from the PCF50732.

When RXON goes LOW, the last pair of I and Q values will be sampled and transferred to the baseband processor (both I and Q components). BIOCLK stops after additional 16 BIOCLK cycles. The receive path is powered down again. In power-down the BIOCLK output is put in 3-state and the BOEN output is HIGH.

The output format is 2 × 12-bit I/Q (twos complement). Transmission occurs MSB first, I followed by Q. The serial clock signal BIOCLK will run at 6.5 MHz, or 13 MHz in the NZIF mode. Figure 6 shows the timing of the BSI data reception.

An automatic offset compensation mechanism is provided in order to achieve the required performance. This mechanism will short the receive (RX) inputs internally and measure the resulting offset value. This offset value will be subtracted from all subsequent I/Q output words.
The offset inherent to the device can thereby be reduced to a few millivolts. Default value for both I- and Q-offset is zero.

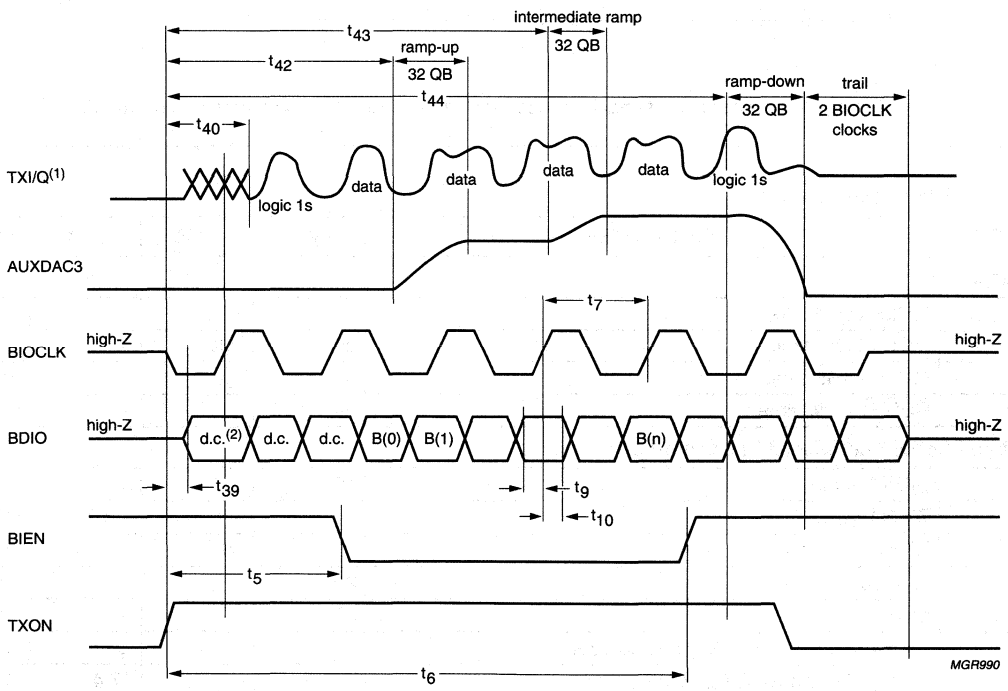
Offset compensation measurement can be done on three channels separately: baseband receive I channel, baseband receive Q channel and AUXADC channel. All AUXADC channels use the same offset compensation value. Starting an offset measurement is done by writing a logic 1 into the offset trigger register for each channel that needs calibration. If the value '7' (decimal) is written into the offset trigger register offsets will be measured for I, Q and AUXADC channels.

Offsets can also be read or written directly. Each offset measurement is implemented internally as an AUXADC measurement and takes approximately 100 µs. Offsets from –256 up to 255 can be compensated.

Table 4 Connection of BSI receive signals to the PCF5087X

PCF50732		PCF5087X	
PIN	**I/O**	**PIN**	**I/O**
RXON	I	RFSIG[z]	O
BDIO	I/O	SIOXD	I/O
BOEN	O	SIXEN_N	I
BIOCLK	O	SIOXCLK	I

9.3.4 Baseband Serial Interface (BSI) timing characteristics



(1) TXI/Q = transmit I or Q.
(2) d.c. = don't care; will be overwritten with logic 1.

Fig.5 Timing of the baseband serial interface transmit path; for the timing values see Table 5

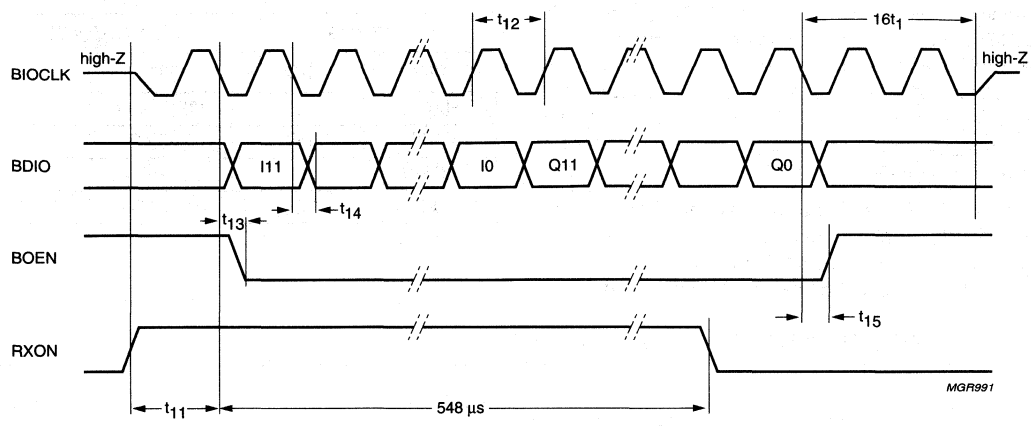


Fig.6 Timing of the baseband serial interface receive path; for the timing values see Table 5.

Table 5 BSI timing characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Master clock					
t_1	MCLK cycle time	–	76.9	–	ns
t_2	MCLK LOW time	30	$\frac{1}{2}t_1$	–	ns
t_3	MCLK HIGH time	30	$\frac{1}{2}t_1$	–	ns
t_4	$\overline{\text{RESET}}$ LOW time	$3t_1$	–	–	ns
Baseband Serial Interface (BSI) transmit path (see Fig.5)					
t_5	BIEN0 value	10	–	511	QB
t_6	BIEN1 value	t_5	–	4000	QB
t_7	BIOCLK cycle time	–	$48t_1$	–	ns
t_9	data set-up time	20	–	–	ns
t_{10}	data hold time	20	–	–	ns
t_{39}	BIOCLK active after TXON rising edge	–	–	t_1	ns
t_{40}	analog TX and GMSK power-up time	–	–	17.4	QB
t_{42}	ramp-up value	0	–	3940	QB
t_{43}	intermediate ramp value	$32 + t_{42}$	–	3980	QB
t_{44}	ramp-down value				
	normal mode	$32 + t_{42}$	–	4020	QB
	double burst mode	$32 + t_{43}$	–	4020	QB

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Baseband Serial Interface (BSI) receive path (see Fig.6)					
t_{11}	analog power-up and filter settling time				
	ZIF mode	–	52	–	µs
	NZIF mode	–	26	–	µs
t_{12}	BIOCLK cycle time				
	ZIF mode	–	$2t_1$	–	ns
	NZIF mode	–	t_1	–	ns
t_{13}	BOEN LOW after falling clock edge	–	–	15	ns
t_{14}	BIOCLK falling edge to data valid	–	–	15	ns
t_{15}	BOEN HIGH after falling clock edge	–	–	15	ns

10 VOICE BAND CODEC

The voice band CODEC is a complete analog front-end circuit. It consists of three parts:

- The **receive path**, which converts a digital linear PCM signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives an analog signal from a microphone or an auxiliary input and converts it into a digital linear PCM signal
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to a digital signal processor.

Various functions and characteristics of the voice band CODEC can be selected by programming the corresponding control registers in the Control register block (see also Tables 11, 22, 23, 24 and 25).

10.1 Voice band receive path

The voice band receive path consists of the following parts:

- The receive part of the voice band signal processor
- **NOISE SHAPER:** 3rd order digital ΣΔ modulator, generates a bit stream at 1 MHz to drive the EARDAC
- **EARDAC:** digital-to-analog converter including low-pass filter for high frequency noise content of noise shaper
- **EARAMP:** amplifier for an earpiece
- **AUXAMP:** amplifier for an auxiliary loudspeaker
- **BUZAMP:** amplifier for a buzzer output.

Linearity of receiver equipment (to earpiece) at EARPGA = 0 dB and a volume control (VOLPGA and EARAMP or AUXAMP) of –12 dB, signal-to-total harmonic distortion ratio according to *"GSM recommendation II.11.10 V.4.16.1"*.

10.1.1 RXVOL

RXVOL controls the volume of the voice band receive path. In conjunction with EARAMP, AUXAMP and BUZAMP it allows a gain variation from +6 to –30 dB in 64 steps; see Table 25. RXVOL also provides a mute selection of the three outputs EARP/EARN, AUXSP and BUZ respectively. At $\overline{\text{RESET}}$ the volume is automatically set to –12 dB.

10.1.2 RXPGA

RXPGA controls the gain of the voice band receive path within a range of –24 to +12 dB in 64 steps for calibration purposes.

10.1.3 RXFILTER

RXFILTER is a digital band-pass filter with a pass band from 300 to 3400 Hz. It is realized by a programmable structure (voice band signal processor).

10.1.4 EARDAC

EARDAC is a DAC operating at a sampling frequency of 1 MHz. It converts the bitstream input to a sampled differential analog signal and low-pass filters the output signal at the same time.

10.1.5 EARAMP

EARAMP is an amplifier, capable of driving a standard earpiece with a minimum impedance of 8 Ω in single-ended mode or 16 Ω in differential mode.

10.1.6 AUXAMP

AUXAMP is an amplifier for connection to an external loudspeaker amplifier of minimum 8 Ω (hands-free car kit).

An **'auxiliary speaker external amplifier control' output pin** (AMPCTRL) can be used to switch on/off an external amplifier (hands-free car kit). The status of AMPCTRL is programmable via the Control Serial Interface; its default value is on.

10.1.7 BUZAMP

BUZAMP is an amplifier for connection to an external buzzer of minimum 8 Ω. It has the same output characteristics as the AUXAMP and can hence be used as a second auxiliary output amplifier. It is switched on/off by a dedicated control bit in the Control register block.

10.2 Voice band transmit path

The voice band transmit path consists of the following parts:

- **MICMUX:** microphone input multiplexer
- **MICADC:** ΣΔ analog-to-digital converter
- **DECIMATOR:** decimates the incoming bit stream from 1 MHz to 40 kHz
- **TXFILTER:** band-pass filter for the digital transmit signal and down-sampling
- **TXPGA/LIM:** fine-programmable gain for calibration, limiter
- **SidePGA:** voice band sidetone programmable gain amplifier.

Linearity of transmitter equipment, signal-to-total harmonic distortion ratio according to *"GSM recommendation II.11.10 V.4.16.1"*.

10.2.1 MICMUX

MICMUX is used to select between a differential signal at pins MICP/MICN and a differential signal at pins AUXMICP/AUXMICN.

Values are specified for a standard electret microphone with a sensitivity of −64 ±3 dB for high gain or for an external microphone with an amplifier sensitivity of −26 ±3 dB (0 dB ≡ 1 V/0.1 Pa = 1 V/μbar; at 1 kHz).

10.2.2 MICADC

MICADC is a ΣΔ A/D converter which generates a 1 MHz bitstream.

10.2.3 DECIMATOR AND TXFILTER

The DECIMATOR is a digital filter, which performs a signal processing to a lower sampling rate at the output compared to the input.

The bitstream with a sampling frequency of 1 MHz is low-pass filtered and down-sampled to 40 kHz by a FIR filter.

A digital high-pass filter and a digital low-pass filter (both IIR filters) process the 14-bit input samples to achieve a band-pass with a pass band from 300 to 3400 Hz. These filters run on the on-chip voice band signal processor (see Fig.7). It's program is down-loaded into the instruction memory (IRAM) via the CSI (see Table 26).

The output of the TXFILTER is down-sampled to a sampling frequency of 8 kHz with a word length of 16 bits.

10.2.4 TXPGA

TXPGA adapts the analog signals coming from MICMUX within a range of −30 to +6 dB. It is designed for calibration purposes.

10.2.5 SIDEPGA

SidePGA loops part of the voice band transmit signal back into the receive path. There are 64 gain steps from mute to +6 dB.

10.3 Voice band digital circuitry

The voice band digital circuitry is responsible for converting a 16-bit PCM signal at 8 kHz sample rate to and from a 1-bit 1 MHz signal. It also contains a band-pass filter for 300 to 3400 Hz and a sidetone engine. Various volume settings are calculated inside this block. Figure 7 shows the block diagram of the voice band signal processor.

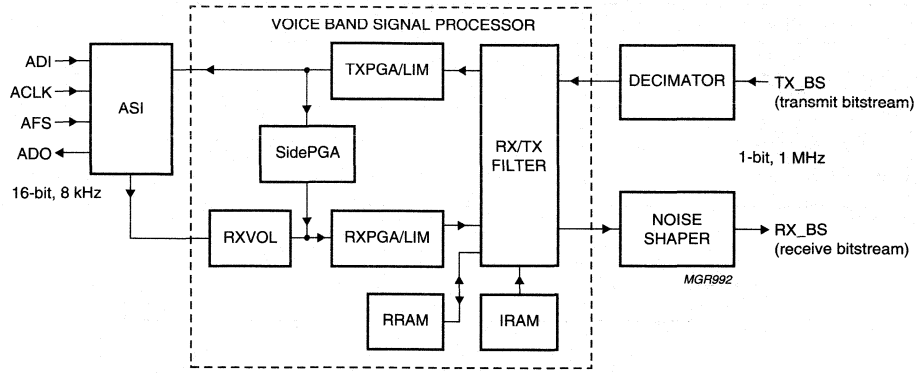


Fig.7 Block diagram of the voice band signal processor.

10.3.1 Volume control block

The volume control block contains the RXPGA, SidePGA, TXPGA and both limiter blocks. The possible settings can be found in the description of the CSI block. All digital volume control blocks, i.e. RXPGA, SidePGA, and TXPGA, will allow settings from +6 to −30 dB and mute in 64 steps. However, not all combinations of settings for these blocks will be meaningful. The limiter will always clip signals with overflow to the maximum or minimum allowable value.

10.3.2 Audio Serial Interface (ASI) block

The ASI is the voice band serial interface which provides the connection for the exchange of PCM data in both receive and transmit directions, between the baseband digital signal processor and the PCF50732. The data is coded in 16-bit linear PCM twos complement words.

A frame start is defined by the first falling edge of ACLK after a rising AFS. This first falling edge is used to clock in the first data bit on both the baseband and the DSP device.

Data on pin ADI is clocked in (MSB first) on the falling edge of the ACLK clock. Data is clocked out (MSB first) on pin ADO on the rising edge of the ACLK clock.

Pin ADO is put in 3-state after the LSB of the transmit word, independent of the length of the AFS pulse. If the channel position 0 (see Section 10.3.2.1) is selected, then the MSB must be output directly after AFS becomes a logic 1, even if no rising edge on ACLK has been given yet.

The following modes of operation are programmable: channel position and ACLK clock mode.

10.3.2.1 Channel position mode

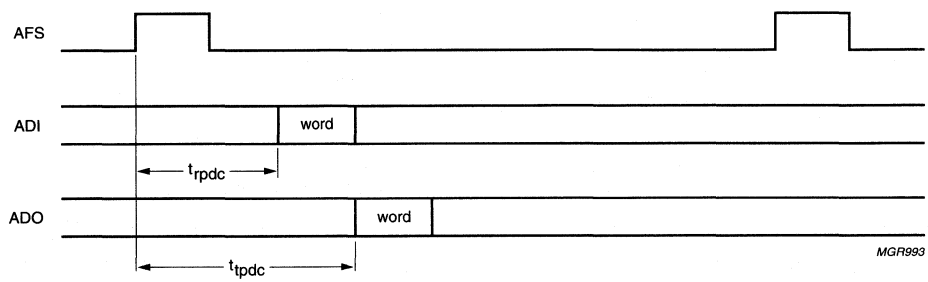
Depending on a programmable register value n (n = 0 to 15) one of 16 channels can be selected (see Table 22). The ASI can add a delay of 16 × n-bit clocks between the assertion of AFS and the start of the MSB of the PCM values. This delay is independently programmable for transmit and receive mode.

10.3.2.2 ACLK clock mode

Single or double clock mode can be selected. Double clock mode implies two clock pulses per data bit and is used for communication with IOM2 compatible devices. In double clock mode data must be output on the first rising edge and be read on the last falling edge.

Table 6 Pin connection of the audio serial interface to the PCF5087X

PCF50732		PCF5087X	
PIN	**I/O**	**PIN**	**I/O**
ADI	I	DD	O
ADO	O	DU	I
ACLK	I	DCL	O
AFS	I	FSC	O



t_{rpdc}: receive path data channel delay.
t_{tpdc}: transmit path data channel delay.

Fig.8 Frame structure of the Audio Serial Interface (ASI).

10.3.2.3 Audio Serial Interface (ASI) timing characteristics

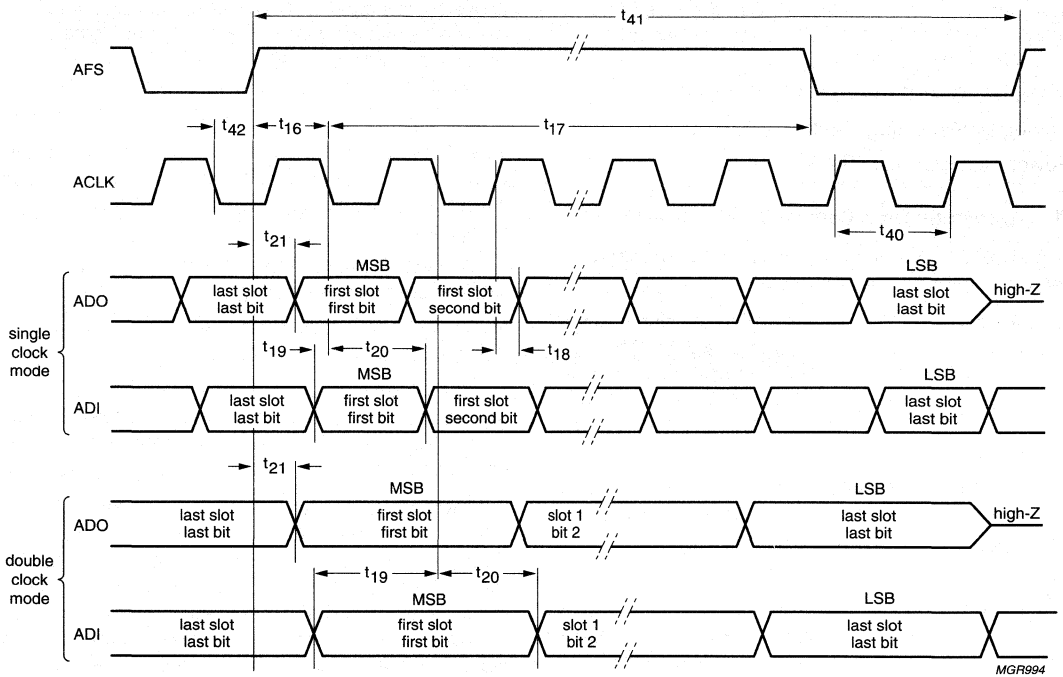


Fig.9 Timing of the Audio Serial Interface (ASI).

Table 7 ASI timing characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{16}	frame sync (AFS) set-up time to falling edge of ACLK	70	–	–	ns
t_{17}	frame sync (AFS) hold time from falling edge of ACLK	40	–	–	ns
t_{18}	ACLK rising edge to data (ADO) valid	–30	–	+30	ns
t_{19}	data (ADI) set-up time to falling edge of ACLK	50	–	–	ns
t_{20}	data (ADI) hold time from falling edge of ACLK	80	–	–	ns
t_{21}	first data valid (ADO) after AFS rising edge	0	–	60	ns
t_{40}	ACLK period				
	single clock mode	0.5	–	7.8	µs
	double clock mode	0.5	–	3.9	µs
t_{41}	AFS period	–	125	–	µs
t_{42}	ACLK LOW before AFS rising edge	40	–	–	ns

11 AUXILIARY FUNCTIONS

The auxiliary functions part consists of three digital-to-analog converters (DACs) and a 4 input analog-to-digital converter (ADC) with a 12-bit range. The DACs are for:

- Automatic Gain Control (AGC): AUXDAC1
- Automatic Frequency Control (AFC): AUXDAC2
- Power ramping: AUXDAC3.

11.1 Automatic Gain Control (AGC): AUXDAC1

The AUXDAC1 is an 8-bit binary coded, guaranteed monotonic digital-to-analog converter.

The status of AUXDAC1 is controlled by the signal AUXST and a power-up bit in the Power control register. The signal that switches the external VCXO can also be used to control the AUXST pin of the PCF50732. The AUXDAC1 output is floating in Power-down mode (AUXST = LOW). The input MCLK is then deactivated.

When AUXST goes HIGH, AUXDAC1 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC1 output pin.

If a write access to the AUXDAC1 register occurs, the DAC is activated with the new content of the DAC register (see Table 14 and 15). The AUXDAC1 must be powered-up by setting the correct bit in the Power control register. At reset AUXDAC1 is powered-down.

11.2 Automatic Frequency Control (AFC): AUXDAC2

The AUXDAC2 is a 12-bit binary coded, guaranteed monotonic digital-to-analog converter. This DAC is used to control the frequency of an external master clock VCXO.

The status of AUXDAC2 is controlled by the signal AUXST and a power-up bit in the Power control register. The signal that switches the external VCXO can also be used to control the AUXST pin of the PCF50732. The AUXDAC2 output is floating in Power-down mode (AUXST = LOW). When AUXST goes HIGH, AUXDAC2 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC2 output pin.

The default value for AUXDAC2 is 1.1 V which corresponds to a 800H code in the AUXDAC2 register. At reset AUXDAC2 is powered on.

11.3 Power ramping: AUXDAC3

AUXDAC3 is a 10-bit binary coded digital-to-analog converter designed for power ramping purposes. AUXDAC3 is default off. The power ramping behaviour is described in Section 9.3.2.2.

11.4 Auxiliary analog-to-digital converter (AUXADC)

The AUXADC is specified for voltage and temperature measurements. It contains 4 input channels required for ΔT and ΔV measurements, as well as battery type recognition:

- ΔT: battery temperature, ambient temperature (measured across sensor)
- ΔV: peak battery voltage, battery voltage during transmit burst.

Five 12-bit registers are available in which results of auxiliary analog-to-digital conversions can be stored. Two registers are dedicated to the input AUXADC1 and one to each of AUXADC2, AUXADC3 and AUXADC4.

The AUXADC1 input can be used for battery voltage measurement. In the AUXADC1A register the voltage during a transmit time slot can be stored. The AUXADC1B register can store the voltage during other time slots. If a read request to one of these registers is executed by loading its address into the Read request register, the actual contents of the addressed register are given to the control interface and a new measurement is performed in the next appropriate time slot.

A multiplexer connects each of the AUXADC inputs to a channel of the receive ADC depending on read access to the corresponding register.

Thus an auxiliary analog-to-digital conversion is only possible, if the baseband receive section is not in use (RXON is LOW). At each read request to one of the AUXADC registers, a flag is set in the AUXADC flag register indicating that an analog-to-digital conversion is to be performed. When one of the registers AUXADC1B, AUXADC2, AUXADC3, or AUXADC4 is being read, the baseband interface verifies that RXON is LOW, indicating that no receive burst is currently active. The baseband receive path is then powered up. After the ADC settling time has elapsed (see $POST_{AUXADC}$ in Chapter 18), valid data is available and stored in the corresponding register.

After conversion the corresponding bit in the AUXADC flag register is reset (see Table 18). If RXON is activated during an auxiliary analog-to-digital conversion cycle, the auxiliary conversion is interrupted and restarted when RXON returns LOW, indicating no receive burst activity.

When register AUXADC1A is read, a battery voltage measurement during a transmission burst is executed.

The PCF50732 waits for a rising edge of TXON, and powers up the receive path. After the settling time of the ADC added to the programmed AUXADC conversion delay (in 48 MCLK cycles) has elapsed, valid data is available and stored in the AUXADC1A register.

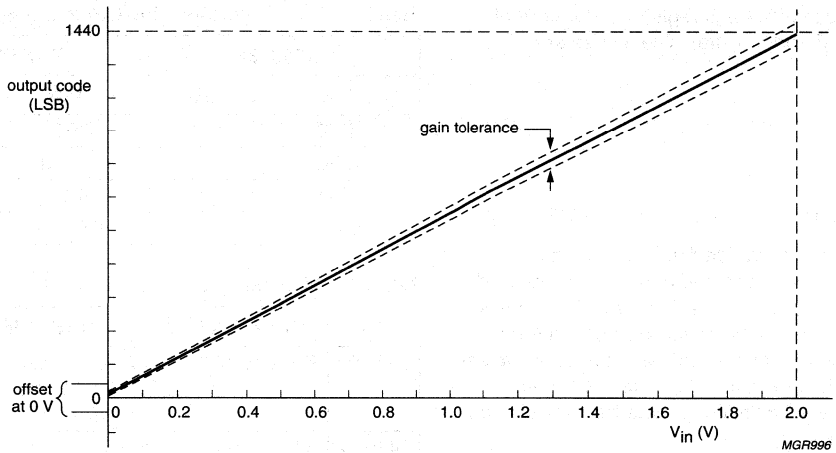


Fig.10 Typical transfer characteristics of AUXADC (output code as function of differential input voltage).

12 CONTROL SERIAL INTERFACE (CSI)

The Control Serial Interface block is used to set and read the status bits inside the PCF50732. It is also used to read data from the auxiliary ADCs and to write data into the auxiliary DACs. Finally, the block is used to write the power ramping curve into a 64 × 10-bit static RAM. It should be noted that only 48 of the 64 addresses can be accessed; see Table 2.

12.1 The serial interface

A 4-line bidirectional serial interface is used to control the circuit. It allows access to each register of the control register block (read and/or write). The 4 lines are:

- Data in (CDI)
- Data out (CDO)
- Clock (CCLK)
- Enable (CEN).

Table 8 lists the normal connections to the PCF5087X.

The data sent to or from the device is loaded in bursts framed by CEN. Clock edges and data bits are ignored until CEN goes active (LOW). Each data word consists of 21 bits that comprises a 4-bit device address, a 4-bit register address, a 12-bit data word and a dummy bit; see Table 9. The 21 bits are transmitted with MSB first. Figure 5 shows the valid timing for data transmission on the control interface.

Data is read in from the CDI pin on the rising edge of the CCLK clock and output on CDO on the falling edge of the CCLK clock. Data is written into the registers on the rising edge of CEN.

If the device address is equal to the chip address, the programmed information on CDI (DB11 to DB00) is loaded into the addressed register (RA3 to RA0) when CEN returns inactive HIGH.

The dummy bit in front is needed for compatibility with older baseband devices.

Reading a register is accomplished by writing the address of the required register into the read request register. The next time CEN goes LOW, the requested data will be shifted out, together with the register and device address.

Table 8 Pin connection of the CSI to the PCF5087X

PCF50732		PCF5087X	
PIN	**I/O**	**PIN**	**I/O**
CDI	I	RFDO	O
CDO	O	RFDI	I
CCLK	I	RFCLK	O
CEN	I	RFE_N2	O

Table 9 Bit mapping of the 21-bit words

BIT	CONTENT	DESCRIPTION
00 to 03	ADD0 to ADD3	device address; for the PCF50732 this is '1001' (= 9 decimal)
04 to 07	RA0 to RA3	register address
08 to 19	DB00 to DB11	data value
20	dummy	don't care

12.2 Control Serial Interface (CSI) timing characteristics

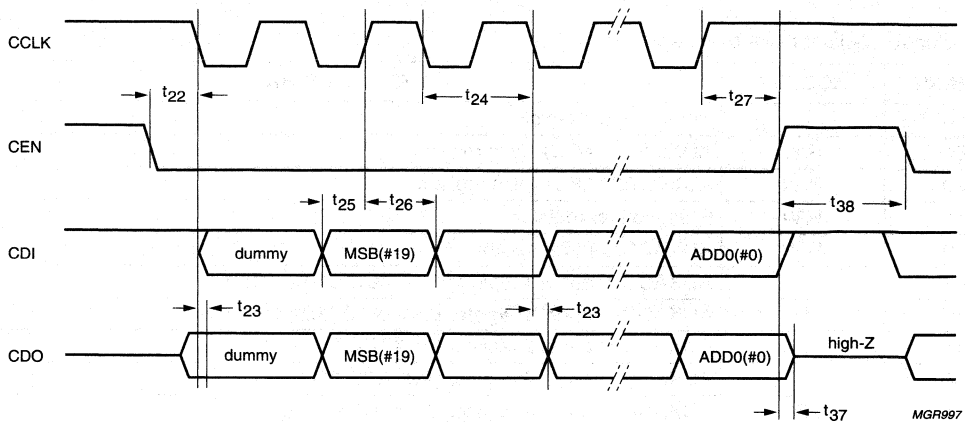


Fig.11 Timing diagram of the Control Serial Interface (CSI).

Table 10 CSI timing characteristics

For the timing diagram see Fig.11.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{22}	CEN set-up time	20	–	ns
t_{23}	CDO data valid after falling clock edge	–	50	ns
t_{24}	CCLK cycle time	100	–	ns
t_{25}	data set-up time to rising edge of CCLK	20	–	ns
t_{26}	data hold time from rising edge of CCLK	30	–	ns
t_{27}	CEN hold time	30	–	ns
t_{37}	CDO 3-state after CEN HIGH	–	30	ns
t_{38}	CEN HIGH time	50	–	ns

12.3 Control register block

This section describes the different registers that are implemented in the PCF50732. An overview is given in Table 11. Tables 12 to 29 describe all the registers of the PCF50732.

Table 11 Control register block overview

ADDRESS	ACCESS	REGISTER NAME
0000	W	Read request register
0001	R/W	AUXDAC1 (AGC) value register
0010	R/W	AUXDAC2 (AFC) value register
0011	R/W	Burst control register
0100	R/W	AUXADC control register
0101	R	AUXADC channel 1 register A (AUXADC1A); note 1
0110	R	AUXADC channel 1 register B (AUXADC1B); note 1
0111	R	AUXADC channel 2 register (AUXADC2); note 1
1000	R	AUXADC channel 3 register (AUXADC3); note 1
1001	R	AUXADC channel 4 register (AUXADC4); note 1
1010	R/W	Voice band control register
1011	R/W	Voice band volume register
1100	R/W	Power control register
1101	R/W	RAM interface register
1110	R/W	Baseband receive control register
1111	R/W	Test mode register; note 2

Notes

1. See description in Section 11.4.
2. Do not use this register.

12.3.1 READ REQUEST REGISTER

Table 12 Read request register

X = don't care during a read/or write access.

ADDRESS	REGISTER NAME	VALUE											
		11	10	9	8	7	6	5	4	3	2	1	0
0000	Read request register	X	X	X	X	r3	r2	r1	r0	s3	s2	s1	s0

Table 13 Read request registers value description

VALUE OF	SYMBOL	DESCRIPTION
Read request register	r3 to r0	Address of the register to be read.
	s3 to s0	Subaddress that might be needed. The subaddress bits are right aligned, meaning that the subaddress always starts with bit 's0' (LSB); e.g. in case of two subaddress bits, 's1' and 's0' are used.

12.3.2 AUXDAC1 (AGC) VALUE AND AUXDAC2 (AFC) VALUE REGISTERS

Table 14 Registers overview

X = don't care during a read/or write access.

ADDR.	REGISTER NAME	VALUE											
		11	10	9	8	7	6	5	4	3	2	1	0
0001	AUXDAC1 (AGC) value register	X	X	X	X	b7	b6	b5	b4	b3	b2	b1	b0
0010	AUXDAC2 (AFC) value register	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 15 AUXDAC1 (AGC) value and AUXDAC2 (AFC) value registers value description

VALUE OF	SYMBOL	DESCRIPTION
AUXDAC1 (AGC) value register	b7 to b0	input value to the 8-bit AUXDAC1 (fed directly into the DAC); the default value is 85H
AUXDAC2 (AFC) value register	b11 to b0	input value to the 8-bit AUXDAC2 (fed directly into the DAC); the default value is 800H

12.3.3 BURST CONTROL REGISTER

The Burst control register controls the timing of the transmit burst (TX-burst). The 'lo'-registers contain the lower 8 bits, the 'hi'-registers the upper 4 bits of a 12-bit delay value. Therefore, each register has a programmable range from 0 to 4095. Not all combinations of values might make sense e.g. ramp-down before ramp-up.

Table 16 Burst control register (address 001 and subaddresses)

X = don't care during a read/or write access.

FUNCTION	SUBADDRESS				VALUE							
	11 (s3)	10 (s2)	9 (s1)	8 (s0)	7	6	5	4	3	2	1	0
RU-lo	0	0	0	0	b7	b6	b5	b4	b3	b2	b1	b0
RU-hi	0	0	0	1	X	X	X	X	b11	b10	b9	b8
RM-lo	0	0	1	0	b7	b6	b5	b4	b3	b2	b1	b0
RM-hi	0	0	1	1	X	X	X	X	b11	b10	b9	b8
RD-lo	0	1	0	0	b7	b6	b5	b4	b3	b2	b1	b0
RD-hi	0	1	0	1	X	X	X	X	b11	b10	b9	b8
BIEN0-lo	0	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0
BIEN0-hi	0	1	1	1	X	X	X	X	b11	b10	b9	b8
BIEN1-lo	1	0	0	0	b7	b6	b5	b4	b3	b2	b1	b0
BIEN1-hi	1	0	0	1	X	X	X	X	b11	b10	b9	b8
Single/double burst mode[1]	1	0	1	0	X	X	X	X	X	X	X	b0
DAC3 burst RAM address[1]	1	0	1	1	X	X	a5	a4	a3	a2	a1	a0
DAC3 burst RAM data[1]	1	1	d9[2]	d8[2]	d7	d6	d5	d4	d3	d2	d1	d0

Notes

1. The programming is described in Section 9.3.2.2.
2. The subaddress positions bit 9 (s1) and bit 8 (s0) do not apply to the DAC3 burst RAM data register.

Table 17 Burst control registers value description

VALUE OF	DESCRIPTION
RU	Value RU, consisting of RU-lo (least significant byte) and RU-hi (most significant byte), is the delay measured in quarterbits ($^1/_{12}$MCLK) between the rising edge of TXON and the start of the ramp-up on AUXDAC3. After this delay, the first 16 values of the AUXDAC3 RAM are sent to AUXDAC3. Shifting out is done at $^1/_{24}$MCLK.
RM	Value RM, consisting of RM-lo (least significant byte) and RM-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the intermediate ramp in a double burst ramp. The RM value is only used in multislot mode. RM must be greater than RU + 32.
RD	Value RD, consisting of RD-lo (least significant byte) and RD-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the ramp-down on AUXDAC3. RD must be greater than RU + 32, or in case of multislot mode, greater than RM + 32.
BIEN0	Value BIEN0, consisting of BIEN0-lo (least significant byte) and BIEN0-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the falling edge of BIEN.
BIEN1	Value BIEN1, consisting of BIEN1-lo (least significant byte) and BIEN1-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the rising edge of BIEN. BIEN1 must be greater than BIEN0.

12.3.4 AUXADC CONTROL REGISTER

Table 18 AUXADC control register (address 0100 and subaddresses)

X = don't care during a read/or write access.

FUNCTION	SUBADDRESS			VALUE								
	11 (s2)	10 (s1)	9 (s0)	8	7	6	5	4	3	2	1	0
AUXADC conversion delay value register	0	0	0	X	X	b6	b5	b4	b3	b2	b1	b0
AUXADC flag register	0	0	1	X	Qoff	Ioff	auxoff	flag 4	flag 3	flag 2	flag 1B	flag 1A
AUXADC offset value register	1	0	0	9-bit signed offset compensation value								
I channel offset value register	1	0	1	9-bit signed offset compensation value								
Q channel offset value register	1	1	0	9-bit signed offset compensation value								
Offset trigger register	1	1	1	X	X	X	X	X	X	Q-off	I-off	Aux

Table 19 AUXADC control registers value description

VALUE OF	DESCRIPTION
AUXADC conversion delay value register	The 7-bit value (b6 to b0) denotes the delay measured in 48MCLK units between the rising edge of TXON and the conversion on AUXADC1A. The normal power-on settling time is added to this delay. Default value is 0.
AUXADC flag register	The AUXADC flag register returns the status of the AUXADC converters. If an auxiliary A/D conversion is pending, the flag of the corresponding AUXADC will be set. The flag register is read only.
AUXADC offset value register I channel offset value register Q channel offset value register Offset trigger register	The offset value registers contain signed 9-bit offset compensation values. These values are subtracted automatically from all baseband receive (BBRX) and AUXADC measurements to compensate for offset errors. The compensation values can be read and written and have a default value of 0. It can also be measured by the device itself. A write to the Offset trigger register will trigger an offset measurement for each of the channels (Q-off, I-off or AUXADC) selected. Offset measurements are special cases of AUXADC measurements and are done sequentially. Each calibration measurement takes approximately 100 µs. The Offset trigger register is write only.

12.3.5 AUXADC REGISTERS

Table 20 AUXADC registers overview

ADDR.	REGISTER NAME	VALUE											
		11	10	9	8	7	6	5	4	3	2	1	0
0101	AUXADC channel 1 register A (AUXADC1A)	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0110	AUXADC channel 1 register B (AUXADC1B)												
0111	AUXADC channel 2 register (AUXADC2)												
1000	AUXADC channel 3 register (AUXADC3)												
1001	AUXADC channel 4 register (AUXADC4)												

Table 21 AUXADC registers value description

VALUE OF	DESCRIPTION
AUXADC1A	12-bit result of the A/D conversion on AUXADC channel 1, measured during a transmission burst
AUXADC1B	12-bit result of the A/D conversion on AUXADC channel 1, measured outside a transmission burst
AUXADC2	12-bit result of the A/D conversion on AUXADC channel 2
AUXADC3	12-bit result of the A/D conversion on AUXADC channel 3
AUXADC4	12-bit result of the A/D conversion on AUXADC channel 4

12.3.6 VOICE BAND CONTROL REGISTER

The Voice band control register is used to control the following functionality of the voice band CODEC:

- Analog input source: microphone (MICAMP) or auxiliary (AUXMIC) input
- Analog output device: earphone (EARAMP), auxiliary (AUXAMP) or buzzer (BUZAMP) output; this register allows individual control of all three output amplifiers
- EARAMP output mode: single-ended (EARP) or differential (EARN/EARP). This selects the input source for the EARAMP-N amplifier. In single-ended mode EARAMP-N will be at V_{ref}, in differential mode it will carry the output signal
- General purpose output pin: AMPCTRL
- Receive and transmit path delay values
- ASI clock mode
- TX gain boost (MICHI).

Table 22 Voice band control register (address 1010 and subaddresses)
X = don't care during a read/or write access.

FUNCTION	SUBADDRESS			VALUE									FUNCTION SETTING
	11 (s2)	10 (s1)	9 (s0)	8	7	6	5	4	3	2	1	0	
Select input source	0	0	0	don't care								0	MICAMP (default)
												1	AUXMIC
Select output amplifier	0	0	1	don't care					X	X	X	0	EARAMP-P off
									X	X	X	1	EARAMP-P on (default)
									X	X	0	X	EARAMP-N off
									X	X	1	X	EARAMP-N on (default)
									X	0	X	X	AUXAMP off (default)
									X	1	X	X	AUXAMP on
									0	X	X	X	BUZAMP off (default)
									1	X	X	X	BUZAMP on
EARAMP output mode	0	1	0	don't care								0	single-ended
												1	differential (default)
AMPCTRL pin polarity	0	1	1	don't care								0	active LOW
												1	active HIGH (default)
Receive path data channel	1	0	0	don't care					d	c	b	a	4-bit delay value (default = 0)
Transmit path data channel	1	0	1						d	c	b	a	
ASI clock mode	1	1	0	don't care								0	single clock (default)
												1	double clock
TX gain boost (MICHI)	1	1	1	don't care								0	7 dB
												1	35 dB (default)

12.3.7 VOICE BAND VOLUME REGISTER

Voice band gain settings can be independently programmed for: TXPGA, RXPGA, RXVOL and SidePGA.

Table 23 Voice band volume register (address 1011 and subaddresses)
X = don't care during a read/or write access.

FUNCTION	SUBADDRESS			VALUE									SELECTED RANGE	DEFAULT SETTING
	11 (s2)	10 (s1)	9 (s0)	8	7	6	5	4	3	2	1	0		
TXPGA gain	0	0	0	X	X	X	a	b	c	d	e	f	−24 to +12 dB	0 dB
RXPGA gain	0	0	1	X	X	X	a	b	c	d	e	f		
RXVOL gain	0	1	0	X	X	X	a	b	c	d	e	f	−30 to +6 dB	−12 dB
SidePGA gain	0	1	1	X	X	X	a	b	c	d	e	f		mute
Band gap setting level	1	0	0	X	X	X	a	b	c	X	X	X	−100 to +75 mV	0 mV offset
Experimental bits	1	0	1	X	X	X	dir	pll	dc	vbch	hclk	bgb	–	pll on, all others off

Table 24 Voice band volume registers value description

VALUE	REMARKS	DESCRIPTION
TXPGA gain	microphone calibration	TXPGA and RXPGA settings use the 6-bit binary fixed point value 'ab.cdef' as a multiplier for each PCM-sample. This results in a control range of +12 to −24 dB. See note 1a.
RXPGA gain	earphone calibration	
RXVOL gain	customer volume control	RXVOL and SidePGA settings use the 6-bit binary fixed point value 'a.bcdef' as a multiplier for each PCM-sample. This results in a control range of +6 to −30 dB (and mute). See note 1b.
SidePGA gain	–	
Experimental bits	–	• dir: bypass clock buffer • pll: clock optimizer • dc: bypass clock capacitor • vbch: voice band chopping • hclk: 26 MHz master clock input • bgb: band gap boost
Band gap setting level	**do not use**	

Note

1. Possible gain settings are listed in Table 25 or can be calculated using the following formulae ('n' is an integer that represents the value that is written into the register; n = 0 to 63):

   a) RXPGA and TXPGA: gain $= 20 \times \log\frac{n}{16}$; add 6.02 dB to each gain for RXPGA and TXPGA settings.

   b) RXVOL and SidePGA: gain $= 20 \times \log\frac{n}{32}$

12.3.7.1 Possible gain selections for voice band blocks: RXPGA, TXPGA, RXVOL and SidePGA

Table 25 shows the possible gain selections for the voice band blocks RXPGA, TXPG, RXVOL and SidePGA. It should be noted that not all possible combinations of these volume settings are meaningful; setting RXPGA, SidePGA and RXVOL to maximum will result in clipping of the output signal.

Table 25 Gain selections

BINARY CODE	GAIN (dB)	
	RXPGA/TXPGA	RXVOL/SidePGA
111111	11.88	5.88
111110	11.74	5.74
111101	11.60	5.60
111100	11.46	5.46
111011	11.31	5.31
111010	11.17	5.17
111001	11.01	5.01
111000	10.86	4.86
110111	10.70	4.70
110110	10.54	4.54
110101	10.38	4.38
110100	10.22	4.22
110011	10.05	4.05
110010	9.88	3.88
110001	9.70	3.70
110000	9.52	3.52
101111	9.34	3.34
101110	9.15	3.15
101101	8.96	2.96
101100	8.77	2.77
101011	8.57	2.57
101010	8.36	2.36
101001	8.15	2.15
101000	7.94	1.94
100111	7.72	1.72
100110	7.49	1.49
100101	7.26	1.26
100100	7.02	1.02
100011	6.78	0.78
100010	6.53	0.53
100001	6.27	0.27
100000	6.00	0.00

BINARY CODE	GAIN (dB)	
	RXPGA/TXPGA	RXVOL/SidePGA
011111	5.72	−0.28
011110	5.44	−0.56
011101	5.14	−0.86
011100	4.84	−1.16
011011	4.52	−1.48
011010	4.20	−1.80
011001	3.86	−2.14
011000	3.50	−2.50
010111	3.13	−2.87
010110	2.75	−3.25
010101	2.34	−3.66
010100	1.92	−4.08
010011	1.47	−4.53
010010	1.00	−5.00
010001	0.51	−5.49
010000	0.00	−6.02
001111	−0.58	−6.58
001110	−1.18	−7.18
001101	−1.82	−7.82
001100	−2.52	−8.52
001011	−3.28	−9.28
001010	−4.10	−10.10
001001	−5.02	−11.02
001000	−6.04	−12.04
000111	−7.20	−13.20
000110	−8.54	−14.54
000101	−10.12	−16.12
000100	−12.06	−18.06
000011	−14.56	−20.56
000010	−18.08	−24.08
000001	−24.10	−30.10
000000	off	off

12.3.8 POWER CONTROL REGISTER

The Power control register is used to control power-up and power-down of the different sections of the device. Changing the power status is accomplished by addressing the device as shown in Table 26 and setting bit 0 (= a) according to the required state:

a = 0 → power-down

a = 1 → power-up.

Setting the baseband RX or TX flag is functionally equivalent to setting RXON or TXON respectively (logical OR function). The CSI is also accessible when the band gap is powered down. Therefore no reset is required to power-up after total power-down.

Table 26 Power control register (address 1100 and subaddresses)

FUNCTION	SUBADDRESS				VALUE								DEFAULT	
	11 (s3)	10 (s2)	9 (s1)	8 (s0)	7	6	5	4	3	2	1	0	VALUE	STATUS
AUXDAC1	0	0	0	1	don't care							a	0	off
AUXDAC2	0	0	1	0								a	1	on
AUXDAC3	0	0	1	1								a	0	off
Voice band transmit	0	1	0	0								a	0	off
Voice band receive	0	1	0	1								a	0	off
V_{ref}	0	1	1	0								a	1	on
Baseband receive	1	0	0	0								a	0	off
Baseband transmit	1	0	0	1								a	0	off
Complete device	1	1	1	1								a	1	on

12.3.9 RAM INTERFACE REGISTER

The RAM interface register is a general purpose communication channel between the serial interface CSI and the voice band signal processor. None of the processor registers have default values.

The Voice band control register is used to communicate with the voice band signal processor. Register functions with subaddress '00' to '11' can be used to program the Instruction RAM (IRAM) when the voice band processor is not running, i.e. when voice band receive and transmit sections are both powered down.

The IRAM registers are used to write into the voice band instruction RAM.

Normal operation is to write an address into the VSP instruction RAM program counter and write low and high bytes of the 16-bit instructions into their respective locations. No auto-increment is foreseen, i.e. the address register must be updated by the user. Writing to the IRAM is only possible when voice band transmit and receive sections are both powered off. If this is not the case write actions are ignored.

Reading back from the IRAM is not straightforward due to the need for an extra clock pulse when accessing RAMs; when reading back the contents of RAM locations 1, 2, 3 and 4 actual output is 'undefined' as 1, 2, 3, etc.

Table 27 RAM interface register (address 1101 and subaddresses)
X = don't care during a read/or write access.

FUNCTION	SUBADDRESS		VALUE									
	11 (s1)	10 (s0)	9	8	7	6	5	4	3	2	1	0
VSP instruction RAM data low-byte	0	0	X	X	d7	d6	d5	d4	d3	d2	d1	d0
VSP instruction RAM data high-byte	0	1	X	X	d7	d6	d5	d4	d3	d2	d1	d0
VSP instruction RAM program counter	1	0	X	a8	a7	a6	a5	a4	a3	a2	a1	a0
VSP interface register	1	1	x9	x8	x7	x6	x5	x4	x3	x2	x1	x0

12.3.10 BASEBAND RECEIVE CONTROL REGISTER

Normal bandwidth refers to an input signal bandwidth of 100 kHz used for ZIF operation, double bandwidth is 200 kHz used for NZIF operation. Normal sampling refers to a sampling rate of $\frac{1}{2}$MCLK, double sampling refers to sampling at MCLK.

Table 28 Baseband receive control register (address 1110)

FUNCTION	VALUE												OUTPUT RATE
	11	10	9	8	7	6	5	4	3	2	1	0	
Normal bandwidth;													
normal sampling (ZIF)	0	0									0	0	271 kHz[1]
double sampling; note 2	0	0				don't care					0	1	135 kHz
Double bandwidth;													
normal sampling (NZIF)	0	0									1	0	542 kHz
double sampling	0	0				don't care					1	1	271 kHz

Notes

1. Default value.
2. Do not use this function.

12.3.11 TEST MODE REGISTER

Only test mode 8 (TM8) is available to the end user. It is used to mark baseband-I (BB-I) samples with a logic 0 and baseband-Q (BB-Q) samples with a logic 1 on the LSB of the 12-bit value.

Table 29 Test mode register (address 1111)

TEST MODE	FUNCTION	VALUE											
		11	10	9	8	7	6	5	4	3	2	1	0
NM	normal mode (default)	don't care								0	0	0	0
TM1	baseband transmit (BBTX) I digital									0	0	0	1
TM2	baseband receive (BBRX) digital									0	0	1	0
TM3	voice band (VB) loop digital									0	0	1	1
TM4	voice band transmit/receive (VBTX/RX) digital									0	1	0	0
TM5	CSI									0	1	0	1
TM6	baseband (BB) DACs									0	1	1	0
TM7	voice band receive (VBRX) DAC current sources									0	1	1	1
TM8	I/Q marking test									1	0	0	0
TM9	voice band signal processor test mode									1	0	0	1
TM10	VSP signature output mode									1	0	1	0
TM11	MCLK input reflected on BDIO									1	0	1	1
TM12	baseband bitstream output									1	1	0	0

13 VOICE BAND SIGNAL PROCESSOR (VSP)

13.1 Hardware description

The VSP used in the PCF50732 is a 30-bit fixed point VSP with separate data and instruction areas. The data path consists of two guard bits, 16 data bits before and 12 data bits behind the binary point for a total of 30 bits. Twos complement notation is used inside the data path. Intermediate results from calculations are stored in a 64 × 30-bit wide data RAM. Data and Programmable Gain Amplifier (PGA) settings are read in via 7 input ports and written back into 3 output ports.

The instruction path uses a 16-bit format with the 4 MSBs designating the opcode and the trailing 12 bits used to describe the operand. The VSP has 12 major instructions; some instructions use two opcodes (operation codes). The addressing range is 9 bits wide, allowing for a total of 512 instructions, which is more than adequate for the filter types it is intended to calculate. Some room is available for Built-In Self Test (BIST). The ALU consists of a 30-bit subtractor, a 30-bit adder and a 30 × 16-bit 'modified booth'-type parallel multiplier.

The VSP's accumulator has built-in overrange checking and will limit values to their minimum (in case of underflow) or maximum (in case of overflow) value.

The VSP engine is designed to operate at 4 MIPS on a 8 kHz PCM signal.

All instructions take one clock-cycle to complete. It should be noted that since the noise shaper operates at a sample rate of 32 kHz and the voice band filter operates at a sample rate of 40 kHz it is necessary to transfer 4 samples to the receive output and to read 5 samples from transmit input for each frame.

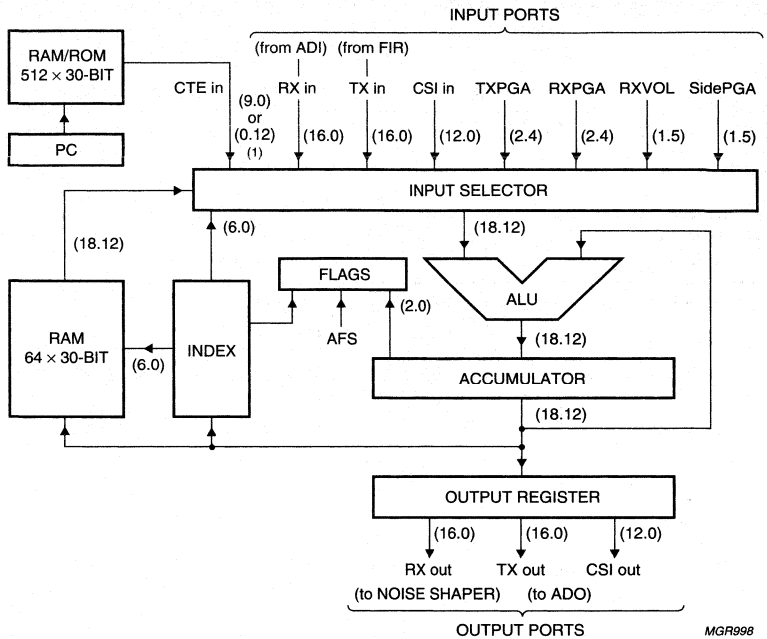
No buffering is foreseen for these samples, which means that the VSP program is responsible for proper spacing in time of the input- and output samples. Failure to ensure proper spacing will result in heavily distorted signals.

Synchronization to the 8 kHz frame-sync signals AFS is also done under program control. The VSP program must ensure that noise shaper and FIR filter are properly reset before actual operation is started.

A VSP-emulator and a VSP-assembler have been written in order to facilitate program development. The assembler generates a stream of 16-bit words that need to be loaded into the instruction RAM. This is done by repeated writes to the VSP control register. The sequence would be as follows:

1. Write address into the VSP instruction RAM program counter register
2. Write the upper 8 bits into the VSP instruction RAM data high-byte register
3. Write the lower 8 bits into the VSP instruction RAM data low-byte register.

This sequence should be repeated until the VSP is fully programmed. Programming can only be done when the VSP is not active. The VSP program counter will be set to location 0 and operation starts after enabling voice band transmit or voice band receive. See also the CSI description in Chapter 12.



The program ROM and program counter are not shown.

(1) (x.y) designates a x + y bits wide data stream with x bits before and y bits after the binary point.

Fig.12 Voice band Signal Processor (VSP) block diagram.

13.2 VSP assembler language

The stack for return addresses is only one entry deep which means that nesting of subroutines is not possible.

Table 30 VSP instruction set

X = don't care during a read/or write access. For the description of the bit symbols see notes 1 to 8.

MNEMONIC	INSTRUCTION	I3	I2	I1	I0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LDA	Load accumulator	0	0	0	m3	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
					m3	m2	m1	m0	d8	d7	d6	d5	d4	d3	d2	d1	d0
STO	Store accumulator	0	0	1	0	m2	m1	m0	X	X	X	d5	d4	d3	d2	d1	d0
RTN	Return from subroutine	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
ADD	Add to accumulator	0	1	0	m3	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
					m3	m2	m1	m0	d8	d7	d6	d5	d4	d3	d2	d1	d0
SUB	Subtract from accumulator	0	1	1	m3	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
					m3	m2	m1	m0	d8	d7	d6	d5	d4	d3	d2	d1	d0
MUL	Multiply with accumulator	1	0	0	m3	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
					m3	m2	m1	m0	d8	d7	d6	d5	d4	d3	d2	d1	d0
JMFS	Jump if flag set	1	0	1	0	f2	f1	f0	a8	a7	a6	a5	a4	a3	a2	a1	a0
JMFC	Jump if flag clear	1	0	1	1	f2	f1	f0	a8	a7	a6	a5	a4	a3	a2	a1	a0
JSFS	Jump subroutine if flag set	1	1	0	0	f2	f1	f0	a8	a7	a6	a5	a4	a3	a2	a1	a0
JSFC	Jump subroutine if flag clear	1	1	0	1	f2	f1	f0	a8	a7	a6	a5	a4	a3	a2	a1	a0
STF	Set/clear flag	1	1	1	0	f2	f1	f0	X	X	X	X	X	X	X	X	d0
IDX	Index operations	1	1	1	1	im2	im1	im0	X	X	X	i5	i4	i3	i2	i1	i0

Notes

1. c11 to c0 denotes a 12-bit twos complement coefficient between −1 and +1.
2. m3 to m0 denotes a 4-bit instruction mode descriptor.
3. f2 to f0 denotes a 3-bit flag descriptor.
4. a8 to a0 denotes a 9-bit address.
5. i5 to i0 denotes a 6-bit index register value.
6. a8 to a0 denotes a 9-bit address.
7. X is a don't care bit.
8. im2 to im0 denotes a 3-bit instruction mode descriptor for the IDX operator.

Table 31 Mode descriptions

m3	m2	m1	m0	MODE NAME	OPERAND	RANGE	ASSEMBLER SHORT HAND
0	0	0	0	register	R(d5 to d0)	register 0 to 63	r
0	0	0	1	register indexed	R((d5 to d0) + index)	register 0 to 63	i
0	0	1	0	port	P(d2 to d0)	ports 0 to 7	p
0	0	1	1	small integer	d8 to d0	−256 to +255; note 1	s
0	1	0	0	index	index	0 to 63; note 1	i
1	bits 11 to 0 form a 12-bit twos complement coefficient between −1 and +1						c

Note

1. Value range in increments of 1.

Table 32 Index mode descriptions

im2	im1	im0	NAME	OPERAND
0	0	0	store	index = d5 to d0
0	0	1	increment	index = (d5 to d0) + index
1	0	0	accu	index = accu

Table 33 Flag descriptions

f2	f1	f0	NAME	DESCRIPTION	REMARKS	TYPE
0	0	0	ALW	always set	flag is clear in VSP test mode; used to initiate BIST	system
0	0	1	INZ	set if index not zero	used to implement loops	
0	1	0	EQ0	set if accu is all 0		
0	1	1	EQ1	set if accu is all 1		
1	0	0	SYNC	PCM sync signal	used to sync VSP to external PCM signal	
1	0	1	A	user flag A		user
1	1	0	B	user flag B		
1	1	1	C	user flag C	used to reset noise shaper and FIR filter	

Table 34 Port descriptions

P2	P1	P0	NAME	DIRECTION	RANGE
0	0	0	Receive (RX)	read/write	−32768 to +32767 (16 bits)
0	0	1	Transmit (TX)	read/write	−32768 to +32767 (16 bits)
0	1	0	CSI	read/write	−2048 to +2047 (12 bits)
0	1	1	ZERO	read	fixed 0
1	0	0	TXPGA	read	0 to 63 (−24 to +12 dB)
1	0	1	RXPGA	read	0 to 63 (−24 to +12 dB)
1	1	0	RXVOL	read	0 to 63 (−20 to +6 dB)
1	1	1	SidePGA	read	0 to 63 (−20 to +6 dB)

13.3 Descriptions of the VSP instruction set

13.3.1 Conventions

In the descriptions of the VSP instruction set:

- A = the 30-bit accumulator
- I = the 6-bit index register
- r.a. = a 6-bit register address
- p.n. = a 3-bit port number (address)
- coeff = a 12-bit coefficient
- f.l. = a 3-bit flag descriptor
- addr = a 9-bit address
- stack = a one entry deep return address stack
- PC = a 9-bit program counter
- o.a. = the 9-bit old address
- s.i. = small integer
- X = don't care during a read/or write access.

13.3.2 LDA instruction

The LDA (Load accumulator) instruction is used to load data into the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 35 LDA instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER	NAME
0	0	0	1	coefficient												coeff → A	LDA c <coeff>	load coefficient
0	0	0	0	0	0	0	X	X	X	register address						R(r.a.) → A	LDA r <r.a.>	load register
0	0	0	0	0	0	1	X	X	X	register address						R(r.a. + I) → A	LDA i <r.a.>	load register indexed
0	0	0	0	0	1	0	X	X	X	X	X	X	port number			P(p.n.) → A	LDA p <p.n.>	load port
0	0	0	0	0	1	1	small integer									s.i. → A	LDA s <s.i.>	load integer
0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	I → A	LDA x	load index

13.3.3 STO instruction

The STO (Store accumulator) instruction is used to store data into register RAM or output ports. No flags are affected.

Table 36 STO instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER	NAME
0	0	1	0	0	0	0	X	X	X	register address						A → R(r.a.)	STO r <r.a.>	store register
0	0	1	0	0	0	1	X	X	X	register address						A → R(r.a. + I)	STO i <r.a.>	store register indexed
0	0	1	0	0	1	0	X	X	X	X	X	X	port number			A → P(p.n.)	STO p <p.n.>	store port

13.3.4 ADD INSTRUCTION

The ADD (Add to accumulator) instruction is used to add data to the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 37 ADD instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER	NAME
0	1	0	1	coefficient												A + coeff → A	ADD c <coeff>	add coefficient
0	1	0	0	0	0	0	X	X	X	register address						A + R(r.a.) → A	ADD r <r.a.>	add register
0	1	0	0	0	0	1	X	X	X	register address						A + R(r.a. + I) → A	ADD i <r.a.>	add register indexed
0	1	0	0	0	1	0	X	X	X	X	X	X	port number			A + P(p.n.) → A	ADD p <p.n.>	add port
0	1	0	0	0	1	1	small integer									A + s.i. → A	ADD s <s.i.>	add integer
0	1	0	0	1	0	0	X	X	X	X	X	X	X	X	X	A + I → A	ADD x	add index

13.3.5 SUB INSTRUCTION

The SUB (Subtract from accumulator) instruction is used to subtract data from the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 38 SUB instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER	NAME
0	1	1	1	coefficient												A – coeff → A	SUB c <coeff>	subtract coefficient
0	1	1	0	0	0	0	X	X	X	register address						A – R(r.a.) → A	SUB r <r.a.>	subtract register
0	1	1	0	0	0	1	X	X	X	register address						A – R(r.a. + I) → A	SUB i <r.a.>	subtract register indexed
0	1	1	0	0	1	0	X	X	X	X	X	X	port number			A – P(p.n.) → A	SUB p <p.n.>	subtract port
0	1	1	0	0	1	1	small integer									A – s.i. → A	SUB s <s.i.>	subtract integer
0	1	1	0	1	0	0	X	X	X	X	X	X	X	X	X	A – I → A	SUB x	subtract index

13.3.6 MUL INSTRUCTION

The MUL (Multiply with accumulator) instruction is used to multiply data with the VSP's accumulator. Flags affected are EQ0 and EQ1. The second operand of the multiplication is restricted to 16-bit; e.g. R(r.a.).

Table 39 MUL instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER	NAME
1	0	0	1	coefficient												A × coeff → A	MUL c <coeff>	multiply coefficient
1	0	0	0	0	0	0	X	X	X	register address						A × R(r.a.) → A	MUL r <r.a.>	multiply register
1	0	0	0	0	0	1	X	X	X	register address						A × R(r.a. + I) → A	MUL i <r.a.>	multiply register indexed
1	0	0	0	0	1	0	X	X	X	X	X	X	port number			A × P(p.n.) → A	MUL p <p.n.>	multiply port
1	0	0	0	0	1	1	small integer									A × s.i. → A	MUL s <s.i.>	multiply integer
1	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	A × I → A	MUL x	multiply index

13.3.7 JMFS INSTRUCTION

The JMFS (Jump if flag set) is used for conditional jumps. The jump is carried out when the flag is set, otherwise the PC is simply incremented.

Table 40 JMFS instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	0	1	0	flag			address									<addr> → PC	JMFS <f.l.> <addr>

13.3.8 JMFC INSTRUCTION

The JMFC (Jump if flag clear) is used for conditional jumps. The jump is carried out when the flag is clear, otherwise the PC is incremented.

Table 41 JMFC instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	0	1	1	flag			address									<addr> → PC	JMFC <f.l.> <addr>

13.3.9 JSFS INSTRUCTION

The JSFS (Jump subroutine if flag set) is used for conditional call to a subroutine. The jump is carried out when the flag is set, otherwise the PC is incremented. Note that the return stack is just one entry deep, so nesting of subroutines is not allowed.

Table 42 JSFS instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	1	1	0	flag			address									<o.a> → stack <addr> → PC	JSFS <f.l.> <addr>

13.3.10 JSFC INSTRUCTION

The JSFC (Jump subroutine if flag clear) is used for conditional jumps to a subroutine. The jump is carried out when the flag is clear, otherwise the PC is incremented. It should be noted that the return stack is just one entry deep, so nesting of subroutines is not allowed.

Table 43 JSFC instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	1	1	1	flag			address									<o.a> → stack <addr> → PC	JSFC <f.l.> <addr>

13.3.11 RTN INSTRUCTION

The RTN (Return from subroutine) is used to return from a subroutine.

Table 44 RTN instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	stack → PC	RTN

13.3.12 STF INSTRUCTION

The STF (Set/clear flag) instruction is used to set or clear the user flags A, B or C. System flags cannot be set or reset under program control.

Table 45 STF instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	1	0	0	flag			X	X	X	X	X	X	X	X	value	<value> → <f.l.>	STF <f.l.> <value>

13.3.13 IDX INSTRUCTION

The IDX (Index operations) instruction is used to store and increment/decrement index values. It should be noted that additions to the index register is done in modulo 64. A 'decrement index register by one' could therefore be programmed as 'IDX + 63'. The 'IDX A' instruction loads the 6 bits to the left of the binary point into the index register, i.e. it stores the integer part modulo 64 into I.

Table 46 IDX instruction

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OPERATION	ASSEMBLER
1	1	0	1	0	0	0	X	X	X	value						<value> → I	IDX = <value>
1	1	0	1	0	0	1	X	X	X	value						I + <value> → I	IDX + <value>
1	1	0	1	1	0	0	X	X	X	X	X	X	X	X	X	A → I	IDX A

13.4 The assembler/emulator

A 2-pass assembler and an emulator was made to assist with the development of VSP programs. The software programs are written in 'C' and currently run under NT, HPUX and LINUX operating systems. The assembler reads assembler source files and produces a log file, sets of VHDL or Verilog stimuli and an output file containing CSI instructions that, when loaded, will load the executable into the VSP RAM.

Requirements for the assembler source code are:

- One instruction or pseudo instruction (see Table 47) per line
- No empty lines
- A maximum of 512 instructions
- Operation always starts at instruction 0.

Table 47 Assembler pseudo instructions

MNEMONIC	INSTRUCTION	DEFINITION
. label	{<.>< ><label>}	Defines a location inside the source code. Is usually used as an argument to JMF/JSF instructions.
define	{<define>< ><label> < ><value>	Defines a variable and assigns a value to it. These variables can then be referenced in the assembler instructions.
include	{<include>< ><file name>}	Reads in another source code file and then continues with the current file.
--	{<-->< ><comment>	Defines a comment; the rest of the line is skipped.

14 LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+3.3	V
I_{DD}	supply current	–	30	mA
I_{I1}	DC current into any pin; except EARP/EARN, AUXSP and BUZ	−10	+10	mA
I_{I2}	DC current into pins EARP/EARN, AUXSP and BUZ	−100	+100	mA
V_I	input voltages on all inputs	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

15 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

16 DC CHARACTERISTICS

T_{amb} = −40 to +85 °C; V_{SS} = 0 V (ground pins must be interconnected externally); $V_{DDA} \geq V_{DDD}$; $V_{DDA(bb)} = V_{DDA(vb)} = V_{DDA(vbo)} = V_{DDA(ref)} = V_{DDA}$ = 2.5 to 2.75 V (supply pins must be interconnected externally); all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{stb(tot)}$	total standby current		–	10	–	µA
P_{av}	average power consumption	V_{DDD} = 1.5 V; V_{DDA} = 2.7 V; without load on audio outputs EARP, EARN, AUXSP and BUZ	–	15	–	mW
Digital power supply: V_{DDD}						
V_{DDD}	digital supply voltage		1.0	1.5	2.75	V
Digital inputs: CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		0.0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	V_{DDD}	V
I_{LI}	input leakage current		–	±1	–	µA
Digital outputs: BIEN, BOEN, ADO and AMPCTRL						
V_{OL}	LOW-level output voltage	I_{sink} = 1.5 mA	–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH-level output voltage	I_{source} = 1.5 mA	$0.7V_{DDD}$	–	–	V
Digital output: BIOCLK						
V_{OL}	LOW-level output voltage	I_{sink} = 1.5 mA	–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH-level output voltage	I_{source} = 1.5 mA	$0.7V_{DDD}$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital bidirectional pins: CDO and BDIO						
V_{IL}	LOW-level input voltage		0.0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	V_{DDD}	V
I_{LI}	input leakage current		–	±1	–	µA
V_{OL}	LOW-level output voltage	I_{sink} = 1.5 mA	–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH-level output voltage	I_{source} = 1.5 mA	$0.7V_{DDD}$	–	–	V
Low-swing clock input: MCLK						
I_{LI}	input leakage current		–	±1	–	µA
Analog power supplies: $V_{DDA(bb)}$, $V_{DDA(vb)}$, $V_{DDA(vbo)}$ and $V_{DDA(ref)}$						
V_{DDA}	analog supply voltage		2.5	2.7	2.75	V
I_{DDA}	analog supply current	V_{DDD} = 1.5 V; V_{DDA} = 2.7 V; RXON active	–	3.5	–	mA
Analog reference pin: V_{ref}						
V_{ref}	DC reference level	no external load	–	1.25	–	V
$I_{I(ref)}$	input source/sink current		–	0.1	–	µA
Analog output pins: IP, IN, QP and QN						
$V_{bias(TXIQ)}$	DC bias level		1.175	1.25	1.325	V
Analog input pins: MICP and MICN						
$V_{ref(MIC)}$	DC input reference level		–	$0.5V_{ref}$	–	V
Analog input pins: AUXMICP and AUXMICN						
$V_{ref(AUXMIC)}$	DC input reference level		–	$0.5V_{ref}$	–	V
Analog output pins: EARP and EARN						
$V_{bias(EAR)}$	DC bias level		–	V_{ref}	–	V
Analog output pin: AUXSP						
$V_{bias(AUX)}$	DC bias level		–	V_{ref}	–	V
Analog output pin: BUZ						
$V_{bias(BUZ)}$	DC bias level		–	V_{ref}	–	V

17 AC CHARACTERISTICS

V_{DDD} = 1.0 to 2.75 V; V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	master clock frequency		–	13.0	–	MHz
Digital input pins: CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and $\overline{\text{RESET}}$						
C_i	input capacitance		–	5.0	–	pF
Digital output pins: BIOCLK, BIEN, BOEN, ADO and AMPCTRL						
t_{dLHO}	output rise time	output load = 10 pF	–	10	–	ns
t_{dHLO}	output fall delay	output load = 10 pF	–	10	–	ns
Digital bidirectional pins: CDO and BDIO						
C_i	input capacitance		–	5.0	–	pF
t_{dLHO}	output rise time	output load = 20 pF	–	10	–	ns
t_{dHLO}	output fall delay	output load = 20 pF	–	10	–	ns
Low-swing clock input: MCLK						
V_{MCLK}	input amplitude	note 1	0.1	–	$0.5V_{DDD}$	V
δ_{MCLK}	duty cycle		40	–	60	%
Analog output pins: IP, IN, QP and QN						
$t_{st(TXIQ)}$	output settling time	output load = 10 pF // 10 kΩ, to 1 LSB, for 0.8 to 2.2 V	–	9.6	–	µs
$R_{o(TXIQ)}$	output resistance	f < 100 kHz	–	105	–	Ω
Analog input pins: IP, IN, QP and QN						
$R_{i(RXIQ)}$	input resistance	differential	200	–	–	kΩ
$C_{i(RXIQ)}$	input capacitance		–	5	–	pF
Analog input pins: AUXADC1, AUXADC2, AUXADC3 and AUXADC4						
$R_{i(AUXADC)}$	input resistance		–	1	–	MΩ
Analog input pins: MICP and MICN						
$R_{i(eq)(MIC)}$	equivalent input resistance	differential	200	220	320	kΩ
Analog input pin: AUXMICP and AUXMICN						
$R_{i(eq)(AUXMIC)}$	equivalent input resistance		200	220	–	kΩ
Analog output pins: EARP and EARN						
$R_{o(EARAMP)}$	output resistance	f = 1 kHz	0	–	1	Ω
Analog output pin: AUXSP						
$R_{o(AUXAMP)}$	output resistance	f = 1 kHz	0	–	1	Ω
Analog output pin: BUZ						
$R_{o(BUZ)}$	output resistance	f = 1 kHz	0	–	1	Ω

Note

1. Input MCLK is internally AC coupled; the signal must not go below V_{SS} or above V_{DDD}.

18 FUNCTIONAL CHARACTERISTICS

18.1 Baseband transmit (BSI to TXI/Q)

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES_{TXIQ}	resolution of TX DACs		–	10	–	bit
S/N_{TXIQ}	signal-to-noise TX DACs		–	55	–	dB
$FSIN_{TXIQ}$	input sampling frequency		–	270.833	–	kHz
$V_{O(TXIQ)(p-p)}$	output signal amplitude (peak-to-peak value)	note 1	0.9	1.0	1.1	V
$V_{DC(TXIQ)}$	output DC level		1.15	1.25	1.35	V
$AMAT_{TXIQ}$	output amplitude matching between I and Q TX paths	note 1	−1.75	–	+1.75	%
			−0.15	–	+0.15	dB
$VOFS_{TXIQ}$	differential DC offset voltage between IP/IN or QP/QN	note 1	−4.5	–	+4.5	mV
$FRESP_{TXIQ}$	frequency response of random output signal	f = 0 to 100 kHz	−3	–	–	dB
		f = 200 kHz	–	–	−30	dB
		f = 250 kHz	–	–	−33	dB
		f = 400 kHz	–	–	−60	dB
		f = 600 kHz	–	–	−70	dB
		f = 1200 kHz	–	–	−70	dB
		f > 1800 kHz	–	–	−70	dB
$MPEI_{TXIQ}$	maximum phase effect instance	note 2	–	22	–	µs
AGD_{TXIQ}	absolute group delay	note 1	–	10	–	µs
GDL_{TXIQ}	group delay linearity	measured at full-scale; 10 kHz < f < 100 kHz; load: 10 pF // 10 kΩ	–	100	–	ns
$GDMAT_{TXIQ}$	group delay matching of I and Q TX paths		–	–	40	ns
$PMAT_{TXIQ}$	phase matching of I and Q TX paths	note 1	–	0.5	–	deg
$PTERMS_{TXIQ}$	RMS phase trajectory error	random input pattern; notes 1 and 3	–	0.5	0.8	deg
$PTEPEAK_{TXIQ}$	peak phase trajectory error		–	1.5	3.0	deg

Notes

1. Measured at full-scale; load: 10 pF // 10 kΩ; f = 67 kHz.
2. Not tested. Defined between the rising edge of BIOCLK which latches a data bit at BDIO to its corresponding maximum phase change on the analog outputs ITX and QTX.
3. Not tested.

18.2 Baseband receive (RXI/Q to BSI)

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C; all values valid for ZIF and NZIF modes.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES_{RXIQ}	resolution	I and Q word length at BSI	–	12	–	bit
S/N_{RXIQ}	signal to noise ratio		–	66	–	dB
$V_{ICM(RXIQ)}$	input common mode voltage	(IP + IN)/2; (QP + QN)/2; referred to V_{SS}	1.0	1.25	1.5	V
$V_{IDM(RXIQ)}$	input differential voltage	(IP − IN); (QP − QN)	−1.5	–	1.5	V
$FSIN_{RXIQ}$	input sampling frequency	Baseband receive control register = 0X	–	6.5	–	MHz
		Baseband receive control register = 1X	–	13	–	MHz
$FSOUT_{RXIQ}$	output sample rate	Baseband receive control register = 00 or 11	–	270.833	–	kHz
		Baseband receive control register = 10	–	541.667	–	kHz
$FRESP_{RXIQ}$	frequency response	Baseband receive control register = 0X; note 1				
		f = 0 to 70 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	−0.8	0	+0.3	dB
		f = 90 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	−3.5	–	dB
		f = 100 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	−5.5	–	dB
		f = 200 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	–	−35	dB
		f > 220 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	–	−45	dB
		Baseband receive control register = 1X; note 1 and 2				
		f = 0 to 140 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	−0.8	0	+0.3	dB
		f = 180 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	−3.5	–	dB
		f = 200 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	−5.5	–	dB
		f = 400 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	–	−35	dB
		f > 440 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	–	−45	dB
DYN_{RXIQ}	dynamic signal range					
	ZIF mode	f = 20 Hz to 135 kHz	60	68	–	dB
	NZIF mode	f = 20 Hz to 270 kHz	60	68	–	dB
$SINAD_{RXIQ}$	signal to noise and distortion ratio	f = 20.0 kHz; $V_{IDM(RXIQ)}$ = 2 V (p-p)	40	–	–	dB
		f = 67.7 kHz; $V_{IDM(RXIQ)}$ = 2 V (p-p)	–	65	–	dB
		f = 20 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	40	–	dB
		f = 67.7 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p)	–	40	–	dB
OPC	output code in BDIO	for maximum input amplitude	–	±1440	–	LSB
$PSRR_{RXIQ}$	power supply ripple rejection	applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply	–	70	–	dB
$GERR_{RXIQ}$	gain error	referenced to maximum amplitude	−6	–	+6	%
			−0.5	–	+0.5	dB
$GMAT_{RXIQ}$	gain matching error	at maximum input level	−3	–	+3	%
			−0.25	–	+0.25	dB
$GDMAT_{RXIQ}$	group delay matching of I and Q RX paths	measured at full-scale; 10 kHz < f < 100 kHz; output load = 10 pF // 10 kΩ	–	–	5	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$OFFS_{RXIQ}$	offset error	before compensation	–40	–	+40	mV
		after compensation	–5	–	+5	mV
$POST_{RXIQ}$	power-on settling time	including decimation filter				
	ZIF mode		–	52	–	µs
	NZIF mode		–	26	–	µs
FGD_{RXIQ}	filter group delay					
	ZIF mode		–	23	–	µs
	NZIF mode		–	11.5	–	µs

Notes

1. Reference level is full-scale input at 67 kHz.
2. This will not be tested.

18.3 Voice band transmit (microphone to ASI)

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES_{MICADC}	resolution of ADC		–	13	–	bit
$FSIN_{MICADC}$	internal sampling frequency		–	1000	–	kHz
$GRAN_{TXPGA}$	calibration gain range		−24	0	+12	dB
$GSTP_{TXPGA}$	calibration gain step size	see Table 25	–	64	–	steps
$GTOL_{VBTX}$	gain tolerance of coder	at TXPGA = 0 dB	−1.5	–	+1.0	dB
$FRESP_{VBTX}$	digital filter frequency response of implemented standard VSP software (version: vb5_all)	f < 100 Hz	–	–	−20	dB
		100 Hz < f < 200 Hz	–	–	−10	dB
		f = 300 Hz to 3.3 kHz	−1	–	+1	dB
		f = 3.3 to 3.4 kHz	−1.5	–	0	dB
		f ≥ 4 kHz	–	–	−20	dB
$FREJ_{VBTX}$	out-of-band rejection	f = 4.6 kHz	40	45	–	dB
		f = 6 to 30 kHz	45	50	–	dB
Microphone/auxiliary signal path						
$V_{IN(rms)}$	nominal input level (RMS value)	TXPGA = 0 dB, MICHI = 1	–	−35	–	dBm
		TXPGA = 0 dB, MICHI = 0	–	−7	–	dBm
N_{IDLE}	idle noise level (pin ADO)	psophometrically weighted[1]; T_{amb} = 25 °C	–	–	−75	dBm0p[2]
THD	total harmonic distortion	f = 1 kHz; PGA = −4 dB; ADO = +2 dBm0	–	–	1	%
SINAD	signal-to-noise and distortion	ADO = 3 dBm0	30	–	–	dB
		ADO = 0 dBm0	40	–	–	dB
		ADO = −10 dBm0	45	–	–	dB
		ADO = −20 dBm0	45	–	–	dB
		ADO = −30 dBm0	40	–	–	dB
		ADO = −40 dBm0	30	–	–	dB
		ADO = −45 dBm0	25	–	–	dB
$PSCT_{VBTX}$	power supply crosstalk	applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply	–	–	2	LSB
Audio Serial Interface (ASI)						
FASOUT	PCM output bit rate		128	–	2048	kbits/s
$FSYNC_{AFS}$	PCM frame synchronization frequency at pin AFS		–	8	–	kHz

Notes

1. Psophometrical weighting: a frequency weighting curve described in *"ITU recommendation O.41"*.
2. The unit dBm0p: 0 dBm0p is generally defined as −3.14 dBFS, where dBFS denotes dB full scale, i.e. a signal with an amplitude covering the complete range of digital values. The suffix 'p' refers to psophometrical weighting.

18.4 Voice band receive (ASI to earphone)

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES_{EARDAC}	resolution of DAC		–	13	–	bit
$FSIN_{EARDAC}$	internal sampling frequency		–	1000	–	kHz
$GRAN_{VOL}$	gain step range		−30	−12	+6	dB
$GSTP_{VOL}$	gain step size	digital steps; see Table 25	–	64	–	steps
$GRAN_{PGA}$	calibration PGA range		−24	–	+12	dB
$GSTP_{PGA}$	gain step size	digital steps; see Table 25	–	64	–	steps
$GTOL_{VBRX}$	gain tolerance of decoder		−1	–	+1	dB
$GMUTE_{VBRX}$	mute attenuation of decoder		40	–	–	dB
$FRESP_{VBRX}$	digital filter frequency response of implemented standard VSP software (version: vb5_all)	f = 0 to 100 Hz	–	–	−20	dB
		f = 300 to 3300 Hz	−1.0	–	+1.0	dB
		f = 3300 to 3400 Hz	−2.0	–	+1.0	dB
		f = 4000 Hz	–	–	−18	dB
$FREJ_{VBRX}$	out-of-band rejection	f = 4600 Hz	38	–	–	dB
		f = 28.6 kHz	40	–	–	dB
Audio Serial Interface (ASI)						
FASIN	PCM input bit rate		128	–	2048	kbits/s
$FSYNC_{AFS}$	PCM frame synchronization frequency at pin AFS		–	8	–	kHz
Earphone output: EARP and EARN						
$V_{ref(EAR)}$	DC reference level		–	V_{ref}	–	V
$V_{o(EAR)(p-p)}$	output voltage (peak-to-peak value)	load: 16 Ω differential	–	2	–	V
		load: 8 Ω single-ended	–	1.5	–	V
$I_{o(EAR)peak}$	output source/sink current	load: 8 Ω single-ended	–	100	–	mA
$GAIN_{EARVOL}$	nominal gain from ASI to EARP/EARN	$GRAN_{VOL}$ = −12 dB; load 32 Ω				
		differential	−13	−12	−11	dB
		single-ended	−19	−18	−17	dB
$GRAN_{SIDVOL}$	total sidetone gain (from MICP/MICN to EARP/EARN)		+5	–	+41	dB
THD_{EAR}	total harmonic distortion	$GRAN_{EARVOL}$ = −12 dB	–	–	1	%
$IDLN_{EAR}$	idle noise at EARP/EARN	psophometrically weighted[1]; $GRAN_{EARPGA}$ = 0 dB	–	–	−72	dBmp[2]

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$SINAD_{EAR}$	signal-to-noise and distortion ratio from ASI to earphone	psophometrically weighted[1]				
		at 3 dBm0 input signal level	30	–	–	dB
		at 0 dBm0 input signal level	35	–	–	dB
		at –10 dBm output signal level	45	–	–	dB
		at –20 dBm output signal level	42	–	–	dB
		at –30 dBm output signal level	40	–	–	dB
		at –40 dBm output signal level	30	–	–	dB
		at –45 dBm output signal level	25	–	–	dB
$PSRR_{EAR}$	power supply ripple rejection at EARP/EARN	applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply	70	–	–	dB
Auxiliary output: AUXSP						
$V_{ref(AUXSP)}$	DC reference level		–	V_{ref}	–	V
$V_{o(AUXSP)}$	output voltage	load: 16 Ω with 47 µF in series to ground	–	V_{ref} ±1	–	V
		load: 8 Ω with 100 µF in series to ground	–	V_{ref} ±0.77	–	V
$I_{o(AUXSP)peak}$	output source/sink current	load: 16 Ω with 47 µF in series to ground	–	62.5	–	mA
$GAIN_{AUXSP}$	nominal gain from ASI to AUXSP	load: 16 Ω with 47 µF in series to ground; $GRAN_{VOL}$ = –12 dB	–19	–18	–17	dB
Buzzer output: BUZ						
$V_{ref(BUZ)}$	DC reference level		–	V_{ref}	–	V
$V_{o(BUZ)}$	output voltage	load: 8 Ω with 100 µF in series to ground	–	V_{ref} – 0.77	–	V
$I_{o(BUZ)peak}$	output source/sink current		–	100	–	mA
$GAIN_{BUZ}$	nominal gain from ASI to BUZ	load: 8 Ω with 100 µF in series to ground; $GRAN_{VOL}$ = –12 dB	–19	–18	–17	dB

Notes

1. Psophometrical weighting: a frequency weighting curve described in *"ITU recommendation O.41"*.
2. The unit dBmp: 0 dBmp refers to a voltage of a signal of 1 mW across a 600 Ω load. The suffix 'p' refers to psophometrical weighting.

18.5 Auxiliary digital-to-analog converters

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUXDAC1						
RES_{DAC1}	resolution		–	8	–	bit
$VOMIN_{DAC1}$	minimum output voltage	register value: 000H	0	–	0.15	V
$VOMAX_{DAC1}$	maximum output voltage	register value: 0FFH	2.1	2.2	2.3	V
$VDEF_{DAC1}$	output voltage after reset	register value: 085H	–	1.147	–	V
MON_{DAC1}	monotonicity range		–	8	–	bit
INL_{DAC1}	integral non-linearity(1)		−5.0	–	+5.0	LSB
DNL_{DAC1}	differential non-linearity(2)		−1.0	–	+1.0	LSB
$OFFS_{DAC1}$	offset error		−80	–	+80	mV
$FSST_{DAC1}$	full-scale settling time	load: 50 pF // 2 kΩ, to V_{SS}; see Fig.13a	–	40	–	µs
$LSBST_{DAC1}$	one LSB settling time		–	8	–	µs
AUXDAC2						
RES_{DAC2}	resolution		–	12	–	bit
$VOMIN_{DAC2}$	minimum output voltage	register value: 000H	0	–	0.15	V
$VOMAX_{DAC2}$	maximum output voltage	register value: FFFH	2.1	2.2	2.32	V
$VDEF_{DAC2}$	output voltage after reset	register value: 800H	–	1.1	–	V
MON_{DAC2}	monotonicity range		–	12	–	bit
INL_{DAC2}	integral non-linearity(1)		–	±10	–	LSB
DNL_{DAC2}	differential non-linearity(2)		−1.0	–	+2.0	LSB
$OFFS_{DAC2}$	offset error		−25	–	+25	mV
$FSST_{DAC2}$	full-scale settling time	load: 50 pF // 10 kΩ, to V_{SS}; see Fig.13b	–	40	–	µs
$LSBST_{DAC2}$	one LSB settling time		–	8	–	µs
$POST_{DAC2}$	power-on settling time	see Section 18.1	–	–	4	ms
AUXDAC3						
RES_{DAC3}	resolution		–	10	–	bit
$VOMIN_{DAC3}$	minimum output voltage	register value: 000H	0	–	0.15	V
$VOMAX_{DAC3}$	maximum output voltage	register value: 3FFH	2.1	2.2	2.3	V
MON_{DAC3}	monotonicity range		–	10	–	bit
INL_{DAC3}	integral non-linearity(1)		−5.0	–	+5.0	LSB
DNL_{DAC3}	differential non-linearity(2)		−1.0	–	+1.0	LSB
$OFFS_{DAC3}$	offset error		−40	–	+40	mV
$FSST_{DAC3}$	full-scale settling time	load: 50 pF // 1 kΩ, to V_{SS}; see Fig.13c	1	10	15	µs
$LSBST_{DAC3}$	one LSB settling time		–	2.5	–	µs
SSC_{DAC3}	output source/sink current		–	–	2.5	mA

Notes

1. INL: the difference of the output to the best fit line. $INL_{(i)} = [V_{(i)} - (a + i \times b)]/1$ LSB; $INL = (INL_{(i)(max)} - INL_{(i)(min)})/2$.
2. DNL is the difference between individual code width and average code width (1 LSB); maximum and minimum specified. $DNL_{(i)} = [(V_{(i+1)} - V_{(i)} - 1\ LSB)/1\ LSB]$; $DNL_{(min)} > -1$ is equivalent to monotonicity $V_{(i+1)} > V_{(i)}$.

18.6 Auxiliary analog-to-digital converters: AUXADC1, AUXADC2, AUXADC3 and AUXADC4

V_{DDA} = 2.5 to 2.75 V; T_{amb} = −40 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES_{AUXADC}	resolution	coded in 12 bits	–	1440	–	LSB
VIN_{AUXADC}	input voltage		0.0	–	2.0	V
$VIN_{AUXADCMIN}$	V_{in} for output code 0		−20	–	20	mV
$VIN_{AUXADCMAX}$	V_{in} for output code +1820	after offset compensation	–	2.0	–	V
$R_{i(AUXADC)}$	input resistance		–	1.0	–	MΩ
INL_{AUXADC}	integral non-linearity		–	2.5	–	mV
DNL_{AUXADC}	differential non-linearity		–	2.5	–	mV
$GERR_{AUXADC}$	gain error	$V_i = V_{ref}$	−0.5	–	+ 0.5	dB
$OFFS_{AUXADC}$	offset error after compensation		−3	–	3	LSB
$POST_{AUXADC}$	power-on settling time		–	170	–	µs

18.7 Typical total current consumption

The typical total current consumption values for the chip in different modes; T_{amb} = 25 °C.

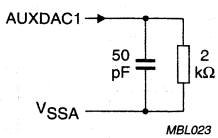
ACTIVITY	TOTAL CURRENT (mA)		REMARKS
	NOTE 1	NOTE 2	
Baseband			
transmit	3.96	4.04	baseband transmit + references + MCLK + BSI
receive	5.14	5.41	baseband receive + references + MCLK + BSI
Voice band transmit and receive	4.79	4.94	voice band transmit and receive + references + 13 MHz + auxiliary DAC2; note 3
Voice band transmit and receive			
baseband transmit	7.32	7.51	voice band transmit and receive + baseband transmit + references + 13 MHz + CSI + auxiliary DACs 2 and 3
baseband receive	8.52	8.91	voice band transmit and receive + baseband receive + references + 13 MHz + auxiliary DAC 2
Auxiliary ADC function	2.75	2.86	auxiliary ADC + CSI + references + 13 MHz + auxiliary DAC2
Auxiliary DAC1	2.35	2.49	auxiliary DACs 1 and 2 + references + 13 MHz
Auxiliary DAC2	1.55	1.59	auxiliary DAC2 + references + 13 MHz
Auxiliary DAC3	4.35	4.56	auxiliary DACs 3 and 2 + CSI + baseband transmit + references + 13 MHz
Idle with MCLK running	0.23	0.24	references + 13 MHz clock
Idle no MCLK; references on	0.18	0.19	references; see Section 19.1.1 “Possibility 1”
Idle	0.01	0.01	all blocks in power-down, no 13 MHz clock

Notes

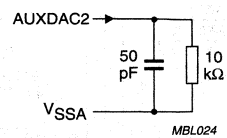
1. V_{DDD} = 2.3 V; V_{DDA} = 2.65 V; external interface current is not included.
2. V_{DDD} = 2.6 V; V_{DDA} = 2.65 V; external interface current is not included.
3. For a signal at the earpiece differential output of amplitude ‘A’ across a load resistance of ‘R’, the current ‘I’ must be added, where: $I = \frac{4}{\pi} \cdot \frac{A}{R}$.

18.8 Typical output loads

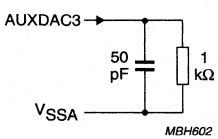
Figure 13 illustrates the typical loads for the outputs: AUXDAC1, AUXDAC2, AUXDAC3, EARP, EARN, AUXSP and BUZ.



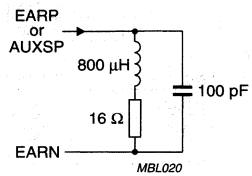
a. AUXDAC1.



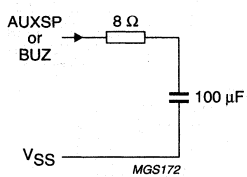
b. AUXDAC2.



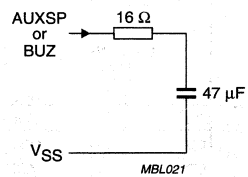
c. AUXDAC3.



d. EARP/EARN or AUXSP.



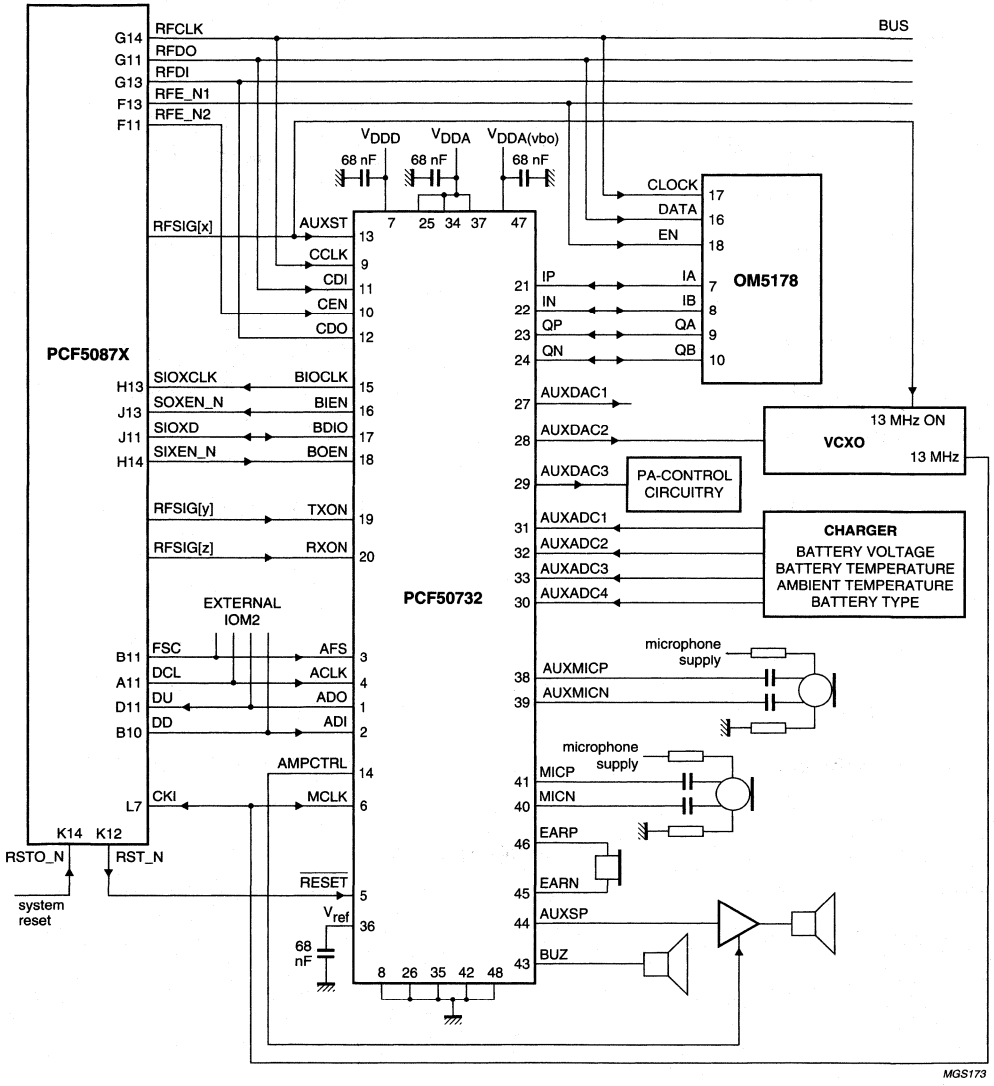
e. AUXSP or BUZ; R = 8 Ω.



f. AUXSP or BUZ; R = 16 Ω.

Fig.13 Typical output loads.

19 APPLICATION INFORMATION



(1) 10 nF can be used instead of 100 nF for high-pass filtering.

Fig.14 Application diagram.

19.1 Wake-up procedure from Sleep mode

Apart from being the status control signal of AUXDAC1, AUXDAC2 and the MCLK input, AUXST also starts a down-counter at each rising edge which controls the output drive capability of pin V_{ref}. This is important for the following considerations. For current consumption reduction during Sleep mode there are **two** possibilities as shown in Section 19.1.1 and 19.1.2.

19.1.1 Possibility 1

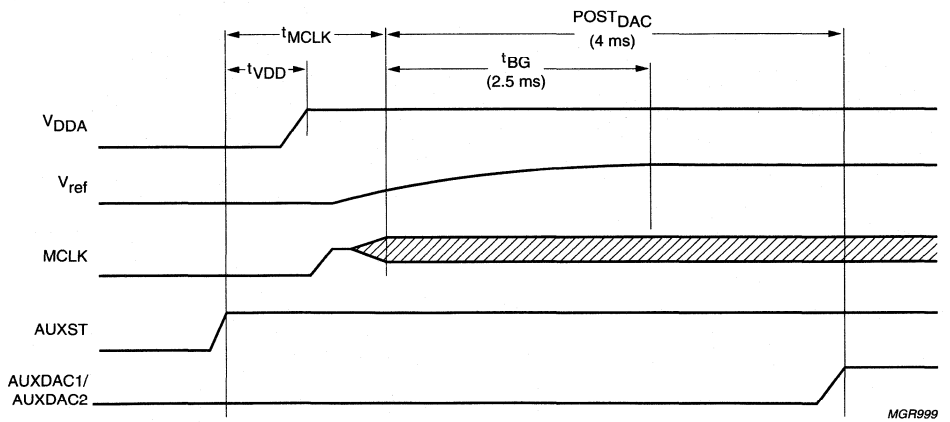
Program every block into power-down via CSI except for the band gap, then pull AUXST LOW to switch off the clock internally. This results in a $I_{DD(total)}$ = 60 µA (typical). Since the band gap hasn't been programmed into power-down, the only active reference is V_{ref}. After a rising edge of AUXST, $POST_{DAC}$ is in the order of 1.5 ms.

19.1.2 Possibility 2

If AUXST is also used to switch off the analog power supply, all references are shut down. The power-up time in this case is measured from the point where the MCLK clock input has valid levels or V_{DDA} has settled to its final value (the latter of the two signals sets the reference point).

A down-counter increases the band gap output drive capability for 32768 MCLK cycles which equals approximately 2.5 ms. After that time the voltage at V_{ref} has reached ±0.5 mV of its final value. The timing diagram illustrates the situation (see Fig.15). Other points to note for this possibility:

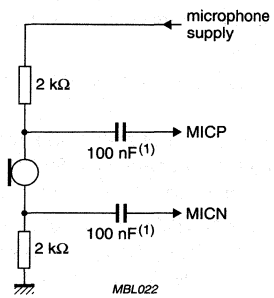
- As long as V_{DDD} is not switched off, all registers keep their values.
- As long as $V_{DDA(bb)}$ is not stable, the internal master clock is not running, because the first stage of the clock generator is supplied by V_{DDA}.
- All digital signals **MUST** remain stable for t_{MCLK} after AUXST has gone HIGH. This is necessary to avoid any timing violations in the digital part of the PCF50732 caused by an unstable MCLK clock input.
- The previously mentioned 2.5 ms for t_{BG} are only valid for C_{Vref} **= 68 nF ±10%** or less. The maximum of value 68 nF is highly recommended for good noise and power supply rejection figures.

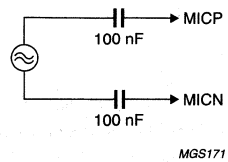


t_{VDD}: settling time until $V_{DDA(bb)}$ has reached 95% of its final value. It is assumed that $t_{MCLK} > t_{VDD}$; otherwise t_{BG} and $POST_{DAC}$ are related to t_{VDD}.
t_{MCLK}: settling time until MCLK clock has reached at least 100 mV (peak-to-peak) level and a frequency of 13 MHz ±10 kHz.
t_{BG}: settling time until voltage at V_{ref} has reached ±0.5 mV of its final value for C_{Vref} **= 68 nF ±10%.**
$POST_{DAC}$: settling time until AUXDAC1 and AUXDAC2 has reached the previously programmed value ±2 LSBs.

Fig.15 Possible timing of wake-up sequence.

19.2 Microphone input connection and test set-up





(1) 10 nF can be used instead of 100 nF for high-pass filtering.

a. Microphone input connection.

b. Microphone input test set-up.

Fig.16 Microphone input connection and test set-up.

Dual N-channel enhancement mode TrenchMOS transistor

PHN210

FEATURES

- Dual device
- Low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package.

APPLICATIONS

- Motor and delay drivers
- D.c. to d.c. converters
- Logic level translator.

The PHN210 is supplied in the SOT96-1 (SO8) surface mounting package.

GENERAL DESCRIPTION

Dual N-channel enhancement mode field-effect transistor in a plastic envelope using 'trench' technology.

PINNING

PIN	DESCRIPTION
1	source 1
2	gate 1
3	source 2
4	gate 2
5 and 6	drain 2
7 and 8	drain 1

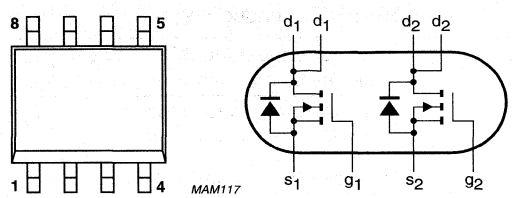


Fig.1 Simplified outline (SOT96-1) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
I_D	drain current (DC)		–	3.4	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V	–	100	mΩ
		V_{GS} = 4.5 V	–	200	mΩ

Dual N-channel enhancement mode TrenchMOS transistor

PHN210

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	repetitive peak drain-source voltage	T_j = 25 to 150 °C	–	30	V
	continuous drain-source voltage		–	30	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	–	30	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current per MOSFET; note 1	T_a = 25 °C	–	3.4	A
		T_a = 70 °C	–	2.8	A
	drain current per MOSFET (both MOSFETs conducting); note 1	T_a = 25 °C	–	2.4	A
		T_a = 70 °C	–	1.9	A
I_{DM}	drain current per MOSFET (pulse peak value)	T_a = 25 °C	–	14	A
P_{tot}	total power dissipation (either or both MOSFETs conducting); note 1	T_a = 25 °C	–	2	W
		T_a = 70 °C	–	1.3	W
T_{stg}, T_j	storage and operating temperature		–65	+150	°C

Note

1. Surface mounted on FR4 board, t ≤ 10 s.

7 N-channel 30/80 mΩ FET array PHN70308

FEATURES

- 30 mΩ pass/isolation FET
- 80 mΩ spindle FETs
- TrenchMOS (low in switching losses).

APPLICATIONS

- Driving high performance three phase brushless DC motors.

DESCRIPTION

Seven enhancement mode MOS transistors in a 28-pin plastic SOT341-1 (SSOP28) package.

FETs 1, 2, 3, 5, 6 and 7 have an R_{DSon} of 80 mΩ and can be configured in three half bridges to drive the spindle, while FET 4 is rated at 30 mΩ and is intended to pass the current through to the motor and/or isolate the motor from the driver stage in case of power loss.

CAUTION
The device is supplied in an antistatic package. The gate inputs must be protected against static discharge during transport or handling.

PINNING SOT341-1 (SSOP28)

PIN	SYMBOL	DESCRIPTION
1 and 3	d1	drain 1
2	s1	source 1
4	g1	gate 1
5 and 7	d2	drain 2
6	s2	source 2
8	g2	gate 2
9 and 11	d3	drain 3
10	s3	source 3
12	g3	gate 3
13, 14, 15, 19, 22, 25 and 28	d4	drain 4
16 and 17	s4	source 4
18	g4	gate 4
20	g5	gate 5
21	s5	source 5
23	g6	gate 6
24	s6	source 6
26	g7	gate 7
27	s7	source 7

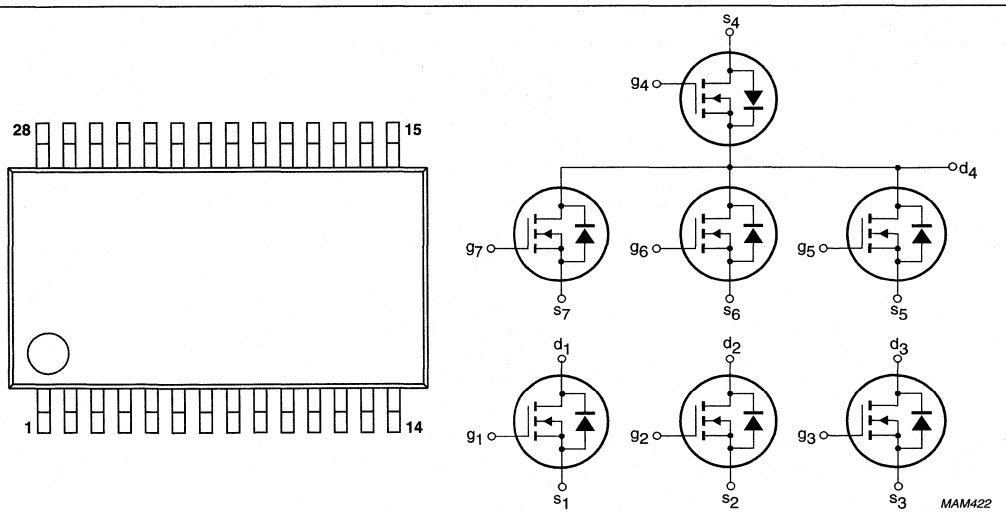


Fig.1 Simplified outline (SOT341-1) and symbol.

QUICK REFERENCE DATA

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_S = 50 °C; note 1	–	5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 2 A			
	spindle drive FETs		–	0.08	Ω
	isolation transistor		–	0.03	Ω
P_{tot}	total power dissipation	T_S = 50 °C	–	8	W

Note

1. T_S is the temperature at the soldering point of the drain leads.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_S = 50 °C			
	spindle drive FETs	duty cycle = 33.3%	–	5	A
	isolation transistor	duty cycle = 100%	–	5	A
I_{DM}	peak drain current	note 1	–	20	A
P_{tot}	total power dissipation	T_S = 50 °C; note 2	–	2.3	W
		T_S = 50 °C; note 3	–	5	W
		T_S = 50 °C; note 4	–	8	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_S = 50 °C			
	spindle drive FETs	duty cycle = 33.3%	–	5	A
	isolation transistor	duty cycle = 100%	–	5	A
I_{SM}	peak source current	note 1	–	20	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. For either one of the spindle drive FETs (FET 1, 2, 3, 5, 6 or 7).
3. For the isolation transistor (FET 4).
4. When FET 4 (duty cycle = 100%) plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 (duty cycle = 33.3%) are carrying the same current.

Compandor SA571

DESCRIPTION

The SA571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The SA571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

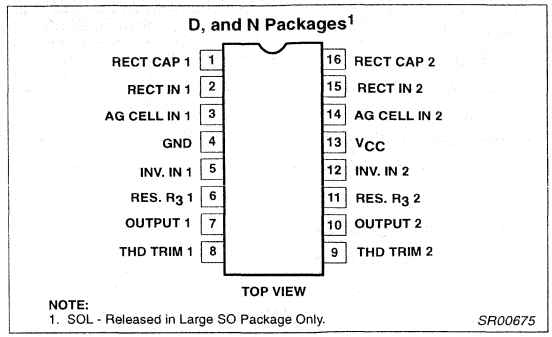


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL)	-40 to +85°C	SA571D	SOT162-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA571N	SOT38-4

BLOCK DIAGRAM

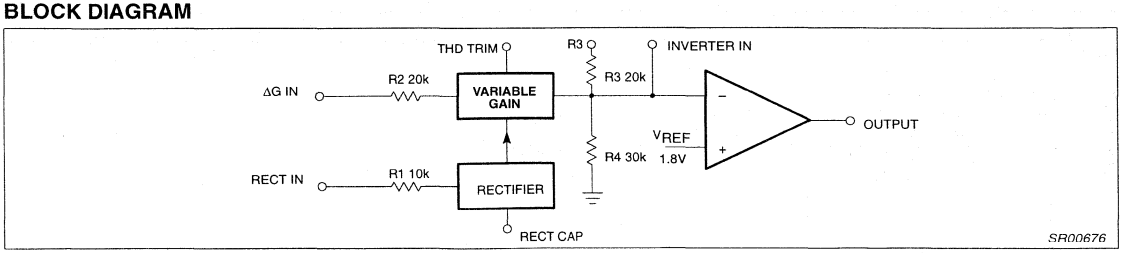


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 571	18	VDC
T_A	Operating ambient temperature range SA	-40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA571[5]			
			MIN	TYP	MAX	
V_{CC}	Supply voltage		6		18	V
I_{CC}	Supply current	No signal		3.2	4.8	mA
I_{OUT}	Output current capability		±20			mA
SR	Output slew rate			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15	%
	Internal reference voltage		1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	60	µV
	Unity gain level[6]	1kHz	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1		dB
	Reference drift[4]			+2, -25	+20, -50	mV
	Resistor drift[4]			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The SA571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})e^{-t/\tau} + G_{final} \; ; \; \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

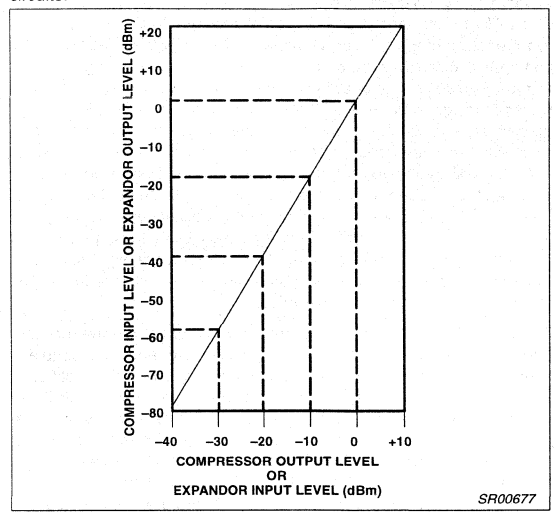


Figure 3. Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT

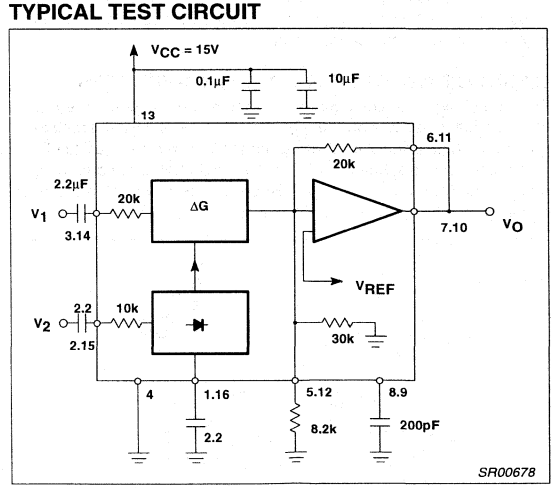


Figure 4. Typical Test Circuit

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components.

This paper describes an inexpensive integrated circuit, the SA571 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The SA571 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 5 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 6 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

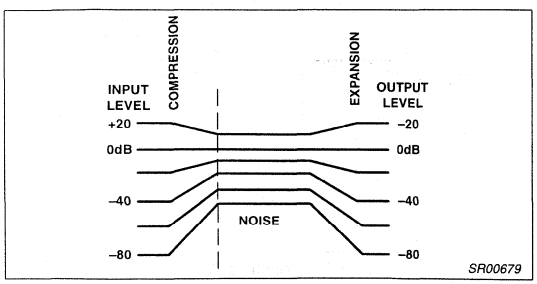


Figure 5. Restricted Dynamic Range Channel

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 7 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 8 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

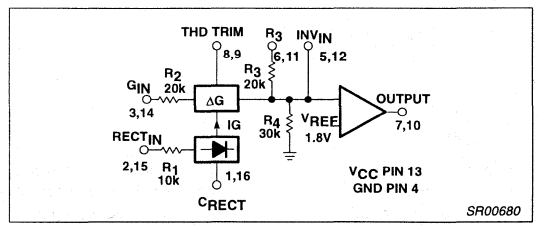


Figure 6. Chip Block Diagram (1 of 2 Channels)

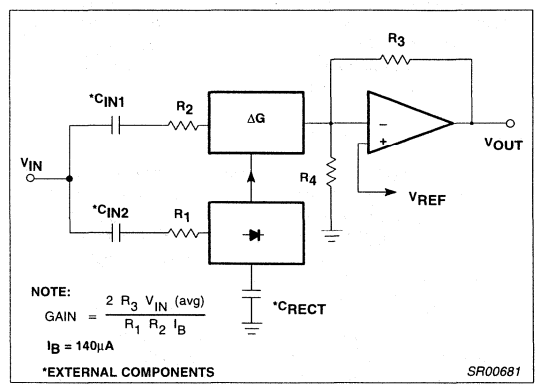


Figure 7. Basic Expander

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.

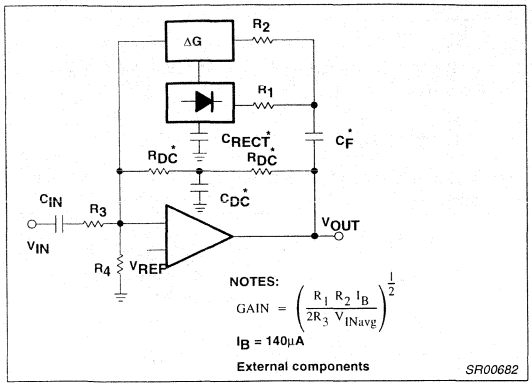


Figure 8. Basic Compressor

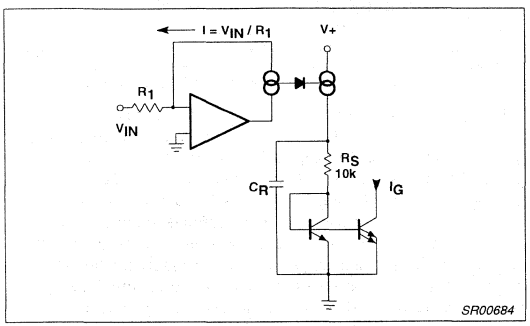


Figure 9. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 9 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

Figure 10 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 11 shows the rectifier accuracy vs input level at a frequency of 1kHz.

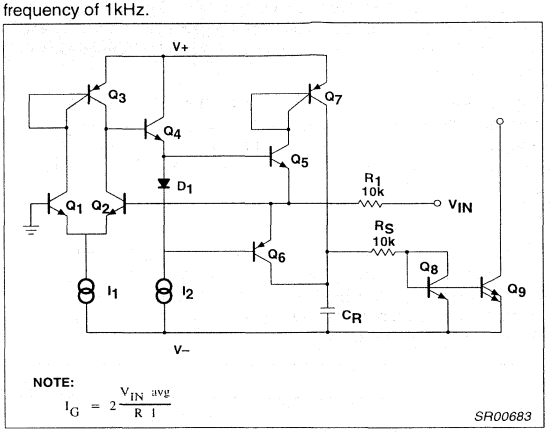


Figure 10. Simplified Rectifier Schematic

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 12. The response at all three levels is flat to well above the audio range.

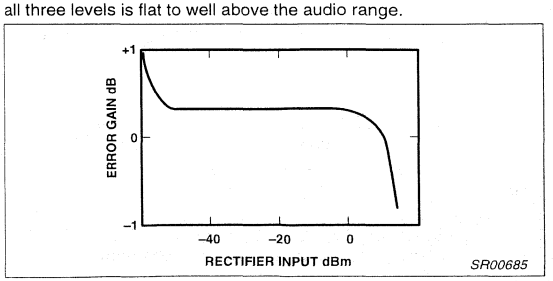


Figure 11. Rectifier Accuracy

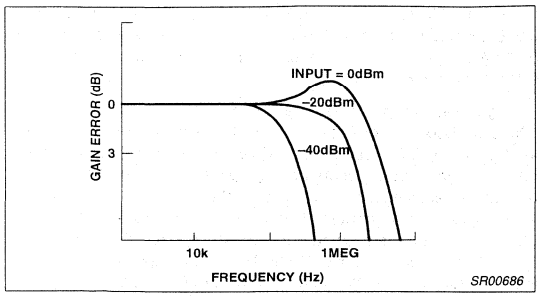


Figure 12. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 13 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($=V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

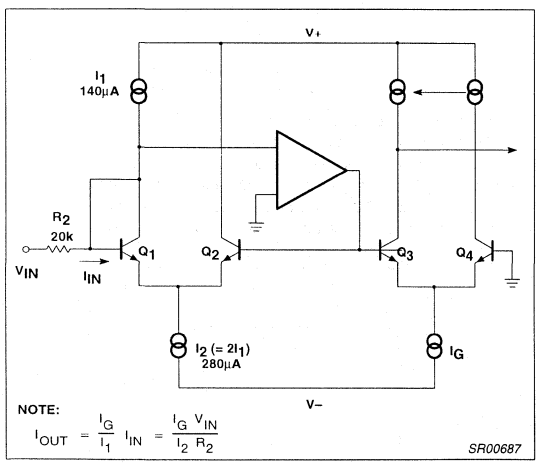


Figure 13. Simplified ΔG Cell Schematic

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN} I_G}{R_2 I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

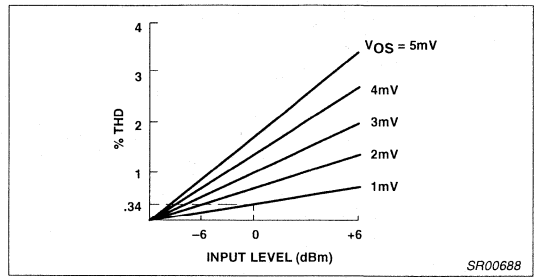


Figure 14. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 14 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated

second harmonic distortion. Figure 15 shows the simple trim network required.

Figure 16 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

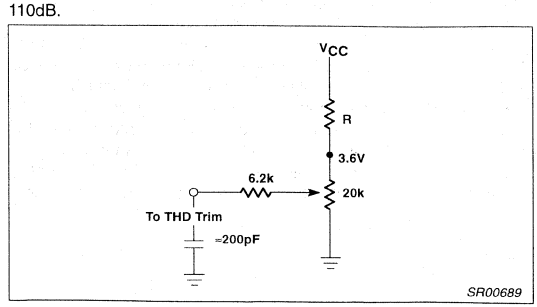


Figure 15. THD Trim Network

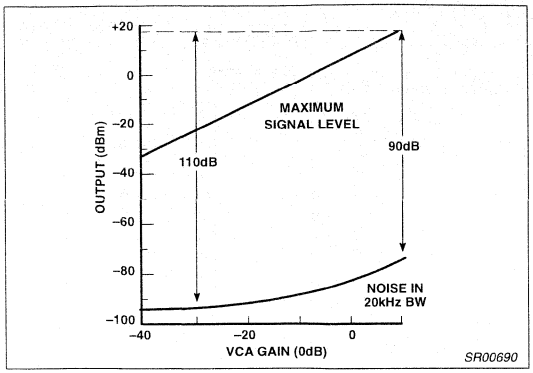


Figure 16. Dynamic Range

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 17 shows such a trim network.

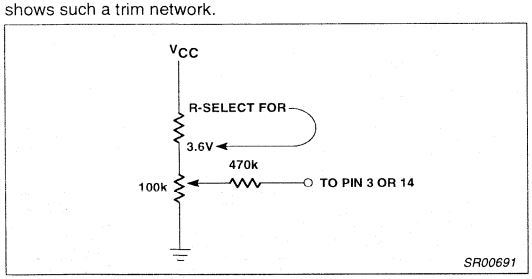


Figure 17. Control Signal Feedthrough

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 18 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

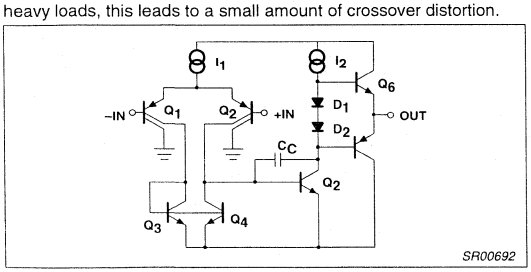


Figure 18. Operational Amplifier

RESISTORS

Inspection of the gain equations in Figures 7 and 8 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 19 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

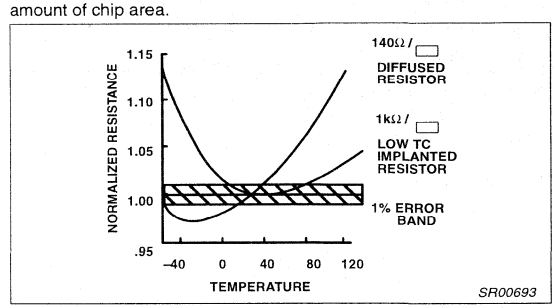


Figure 19. Resistance vs Temperature

Programmable analog compandor SA572

DESCRIPTION

The SA572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The SA572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

PIN CONFIGURATION

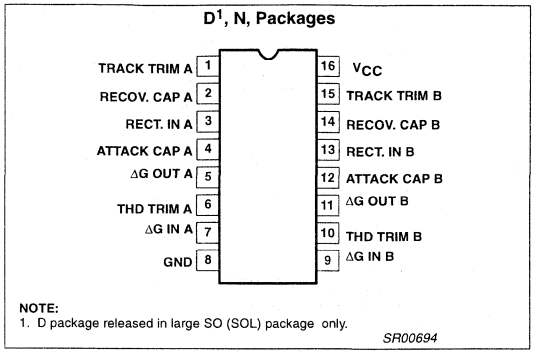


Figure 1. Pin Configuration

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SOL)	−40 to +85°C	SA572D	SOT162-1
16-Pin Plastic Dual In-Line Package (DIP)	−40 to +85°C	SA572N	SOT38-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range SA572	 −40 to +85	 °C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

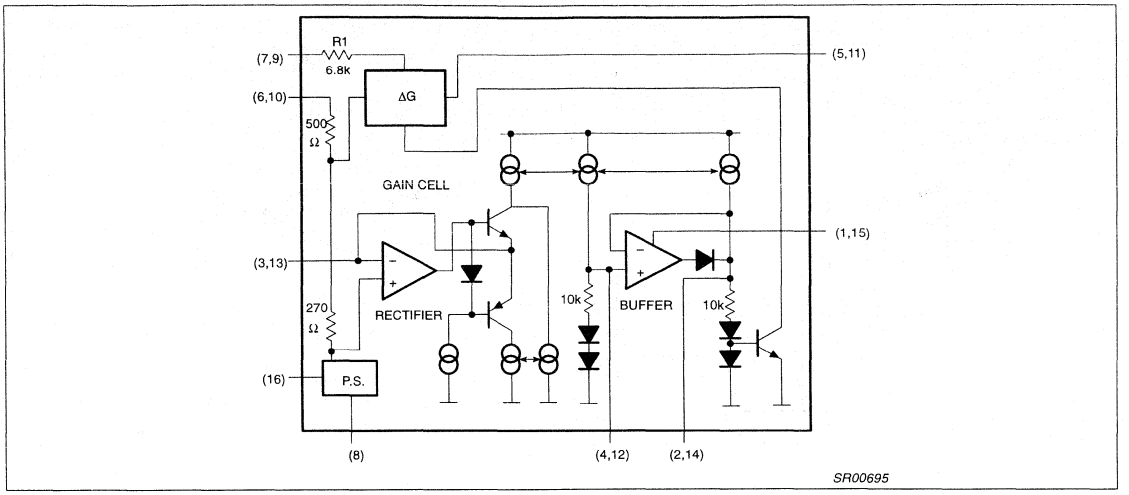


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC}=15V, T_A=25°C; Expandor mode (see Test Circuit).
Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	SA572			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No signal			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A=1.0µF		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R=10µF		0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20–20kHz)		6	25	µV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50	mV
	Unity gain level		–1.5	0	+1.5	dB
	Large-signal distortion	V_1=V_2=400mV		0.7	3	%
	Tracking error (measured relative to value at unity gain)= [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input V_2=+6dB V_1=0dB V_2=–30dB V_1=0dB		 ±0.2 ±0.5	 –2.5, +1.6	 dB dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			dB
PSRR	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT

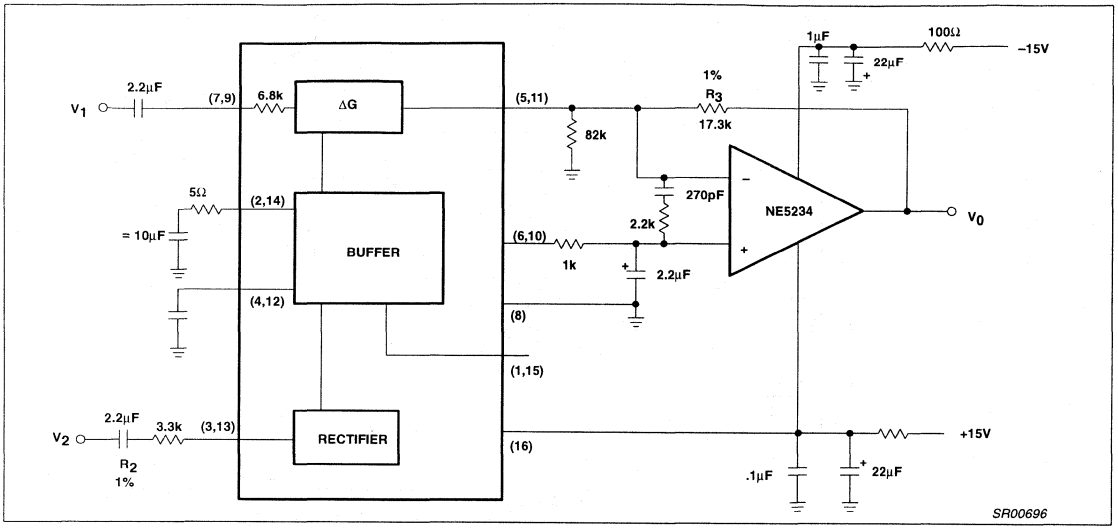


Figure 3. Test Circuit

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics SA572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The SA572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1µF and 1.0µF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7µF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0µF attack and recovery capacitor, while the attack time remains the same.

The SA572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The SA572 is designed for applications from −40°C to +85°C.

SA572 BASIC APPLICATIONS

Description

The SA572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 4 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}}$$

($V_{BE} = V_T I_{IN} IC/IS$)

$$V_T I_n \left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_T I_n \left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$$V_T I_n \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_T I_n \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6μV in the audio spectrum (10Hz-20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

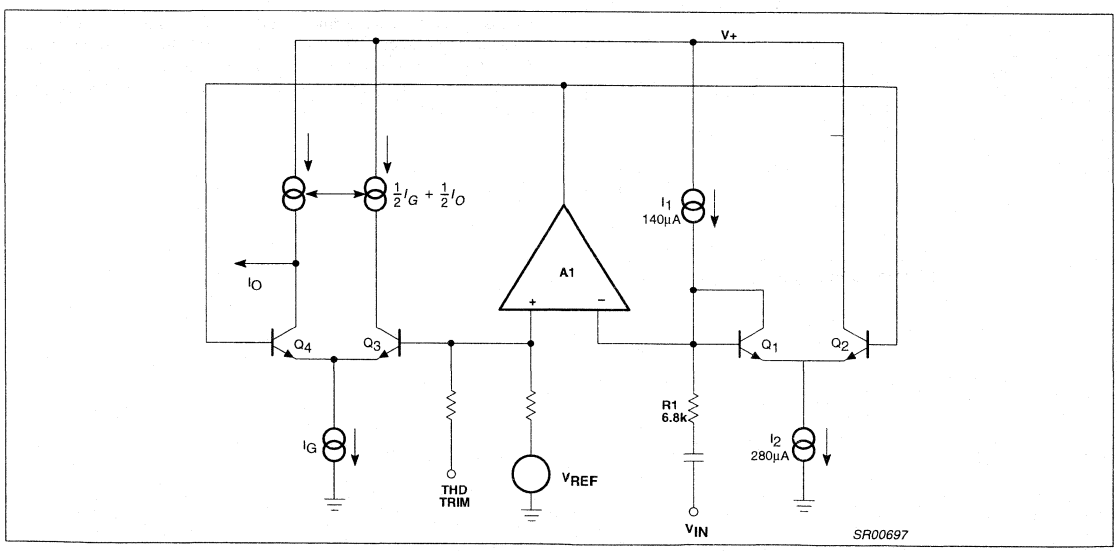


Figure 4. Basic Gain Cell Schematic

Rectifier

The rectifier is a full-wave design as shown in Figure 5. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \qquad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300µA. Within a ±1dB error band the input range of the rectifier is about 52dB.

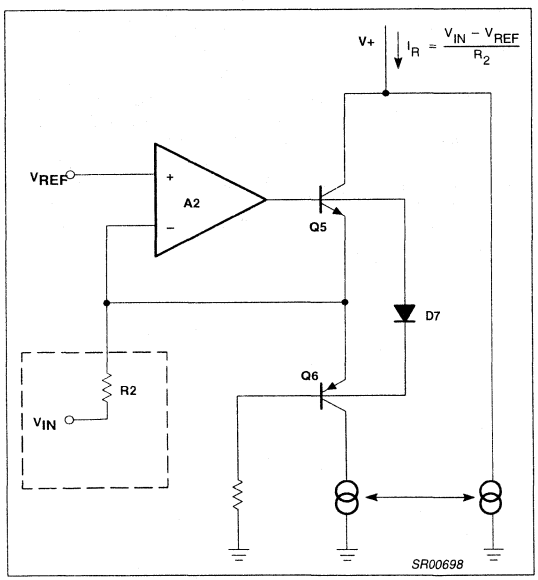


Figure 5. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 6, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT}=Initial Gain

Ga_{FNL}=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL})\, e^{\frac{-t}{\tau_R}} + G_{RFNL}$$

$G_R(t) = (G_{R\,INT} - G_{R\,FNL})\, e + G_{R\,FNL}$

$\tau R = R_R \bullet CR = 10k \bullet CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3µA.

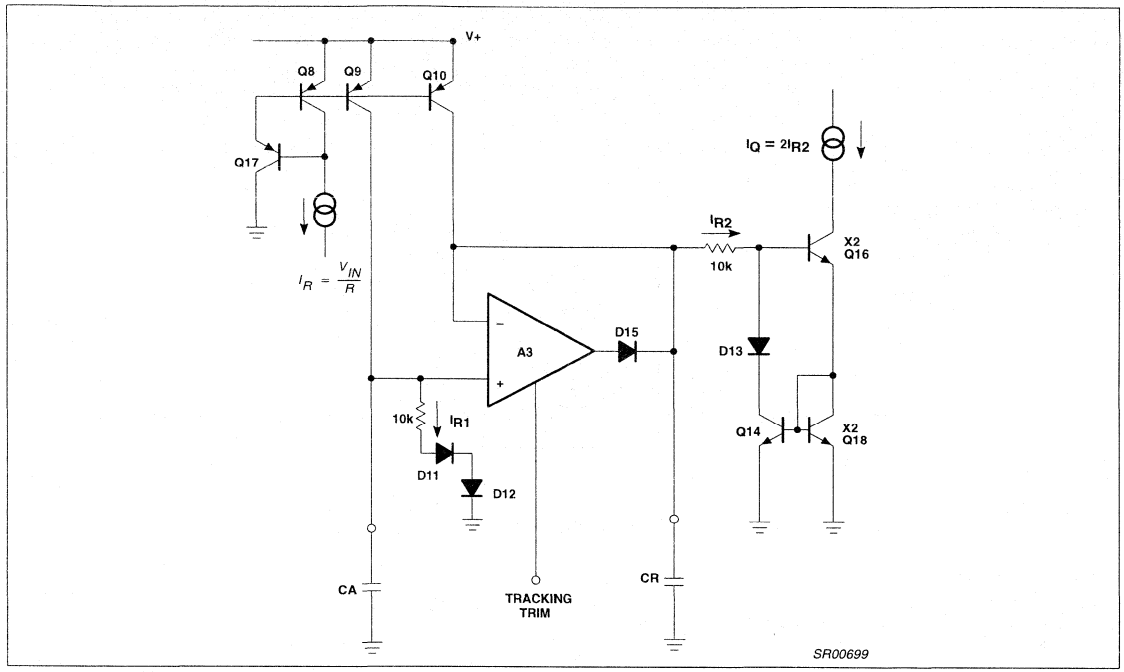


Figure 6. Buffer Amplifier Schematic

Basic Expandor

Figure 7 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

(I_1=140μA)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

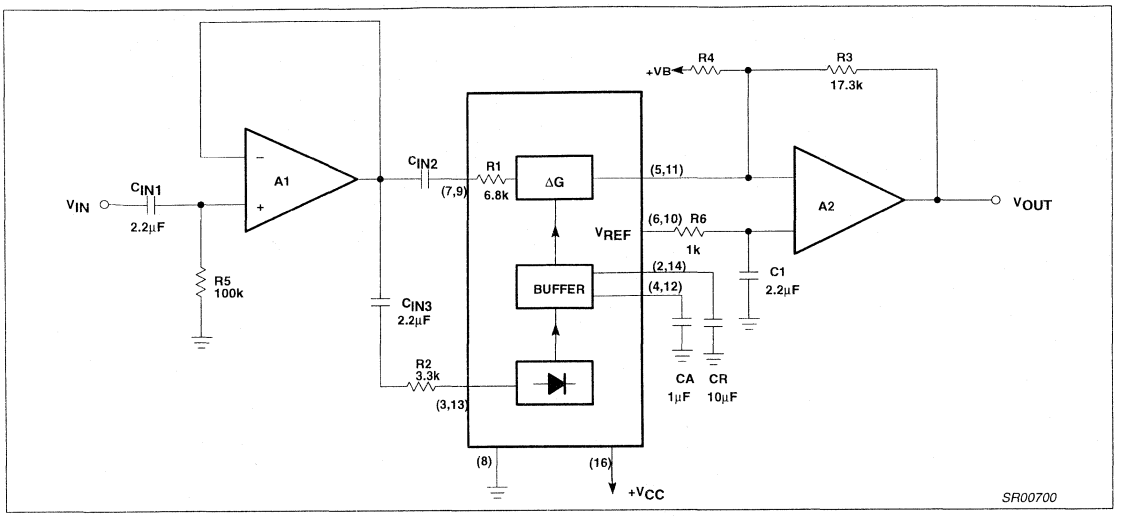


Figure 7. Basic Expandor Schematic

Basic Compressor

Figure 8 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{\frac{1}{2}} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) \quad (8)$$

$$- V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

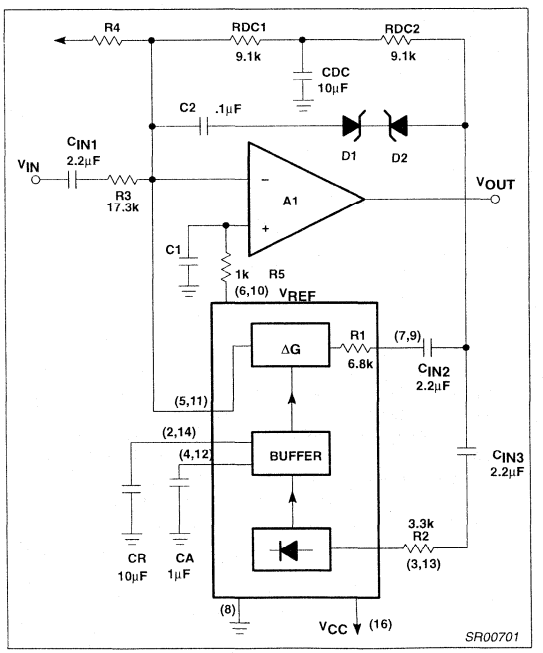


Figure 8. Basic Compressor Schematic

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 9 shows the system level diagram for reference.

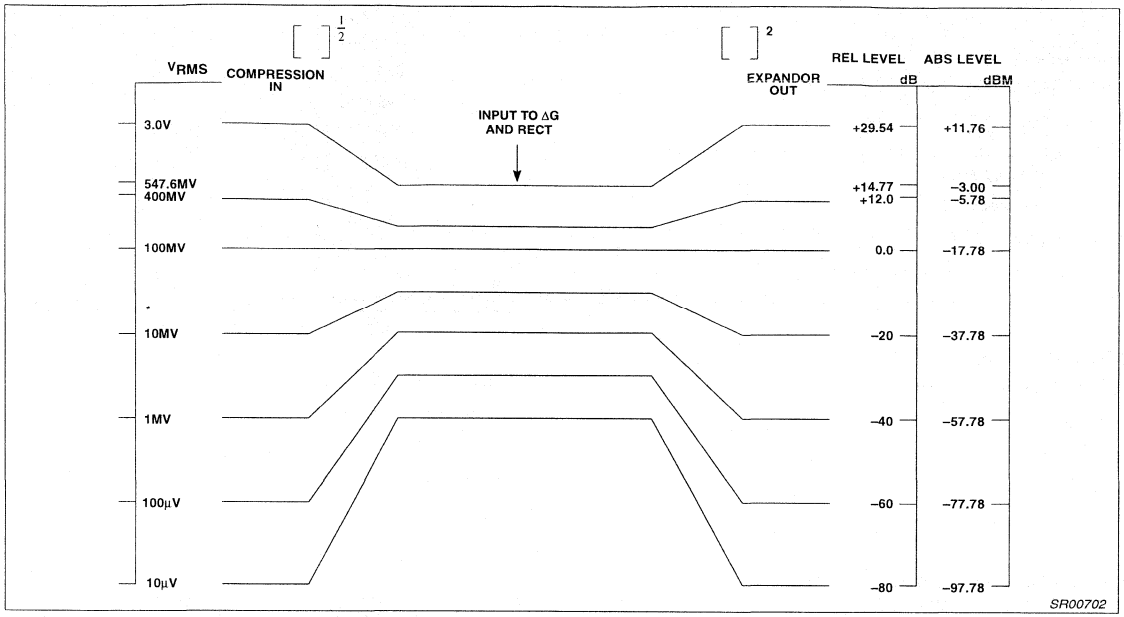


Figure 9. SA572 System Level

Low voltage compandor — SA575

DESCRIPTION

The SA575 is a precision dual gain control circuit designed for low voltage applications. The SA575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

- Operating voltage range from 3V to 7V
- Reference voltage of 100mV$_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION

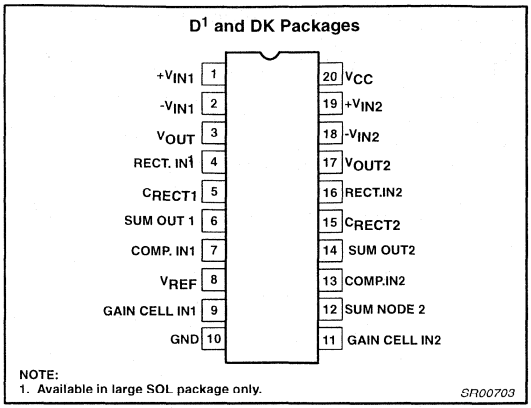


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic Small Outline Large	-40 to +85°C	SA575D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA575DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING SA575	UNITS
V_{CC}	Single supply voltage		–0.3 to 8	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range		-40 to +85	°C
T_{STG}	Storage temperature range		-65 to +150	°C
θ_{JA}	Thermal impedance	SOL	112	°C/W
		SSOP	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT

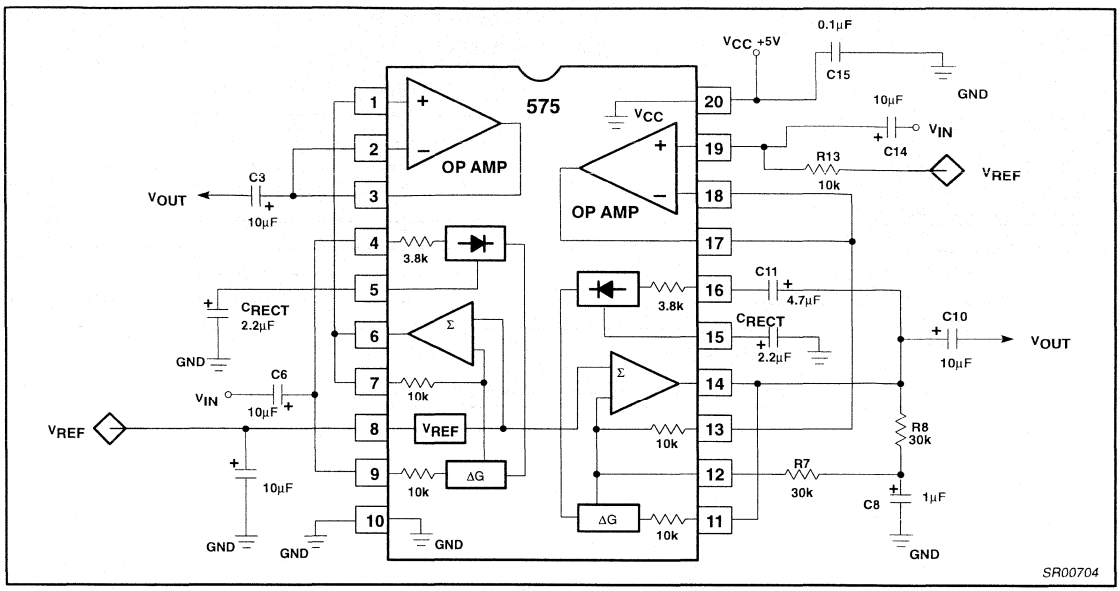


Figure 2. Block Diagram and Test Circuit

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: -40 to +85°C for SA575, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA575 MIN	LIMITS SA575 TYP	LIMITS SA575 MAX	UNITS
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	30	µV
0dB	Unity gain level	1kHz	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-150		150	mV
	Output DC shift	No signal to 0dB	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA575 MIN	LIMITS SA575 TYP	LIMITS SA575 MAX	UNITS
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65	dB
For operational amplifier						
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-1		1	µA
V_{OS}	Input offset voltage			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80		dB
SR	Slew rate	Unity gain		1		V/µs
GBW	Bandwidth	Unity gain		3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 7a and 7b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the SA575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 3, 4, 5 respectively.

The SA575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 6 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 6 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 3. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset

voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.
The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.8k \times 100\mu A}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 4. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.
The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 5. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

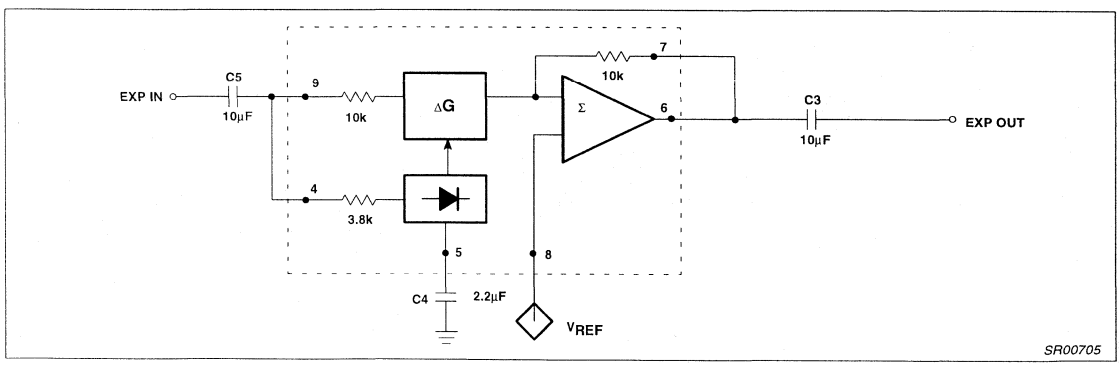


Figure 3. Typical Expandor Configuration

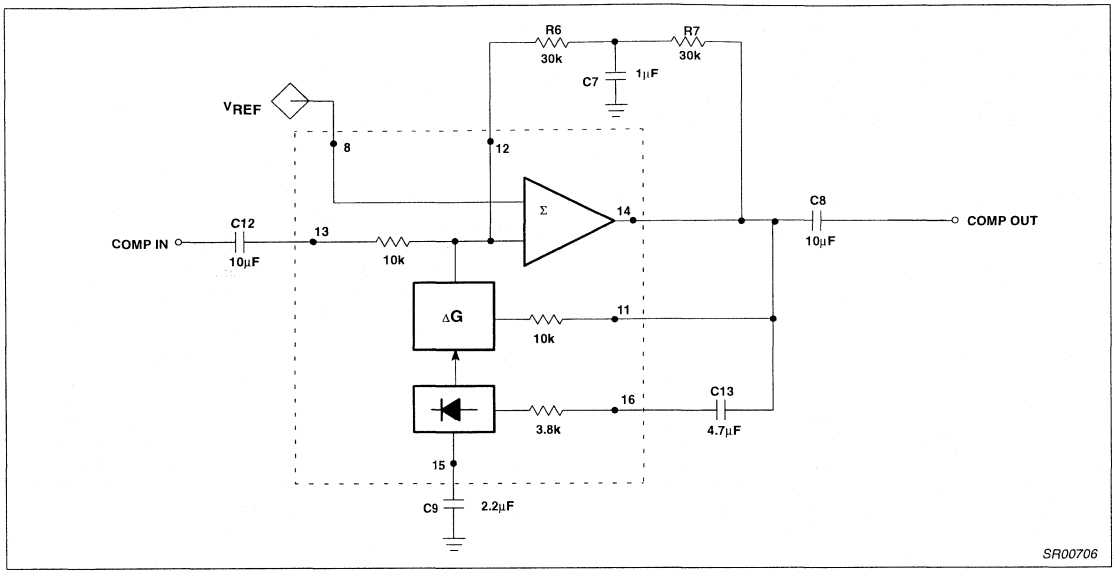


Figure 4. Typical Compressor Configuration

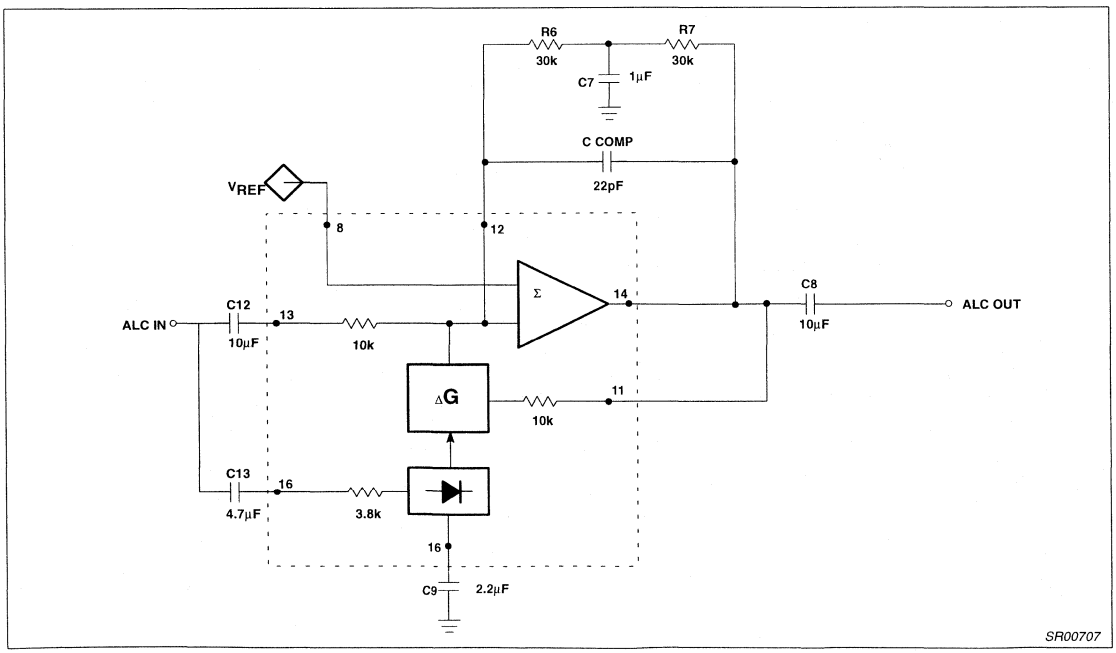


Figure 5. Typical ALC Configuration

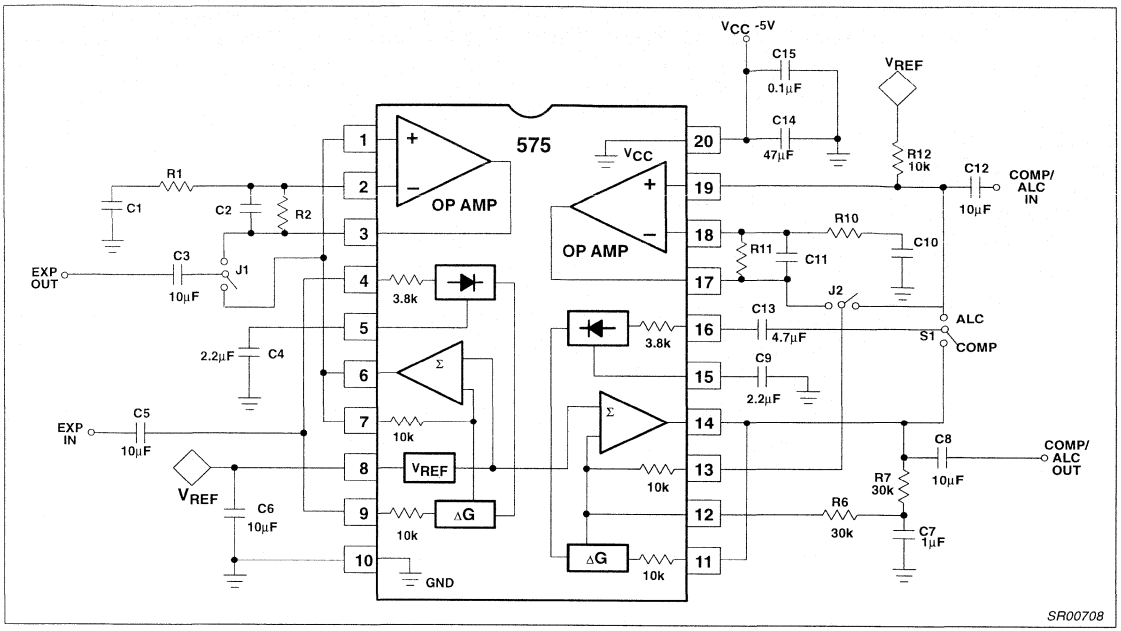
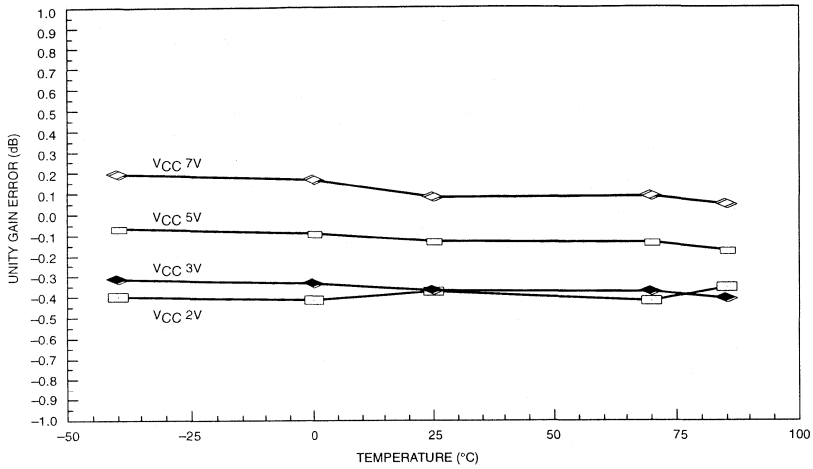
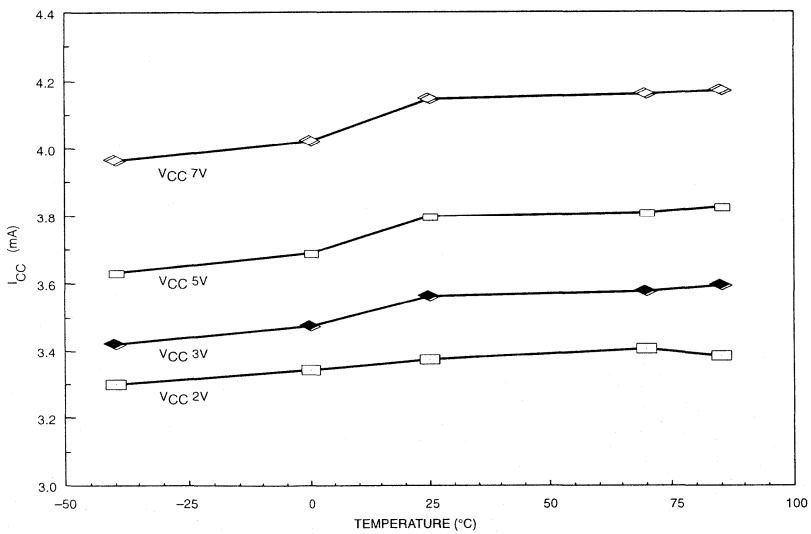


Figure 6. SA575 Low Voltage Expandor/Compressor/ALC Demo Board



a. Unity Gain Error vs Temperature and V_{CC}



b. I_{CC} vs Temperature and V_{CC}

SR00709

Figure 7. Temperature and V_{CC} Curves

TYPICAL PERFORMANCE CHARACTERISTICS

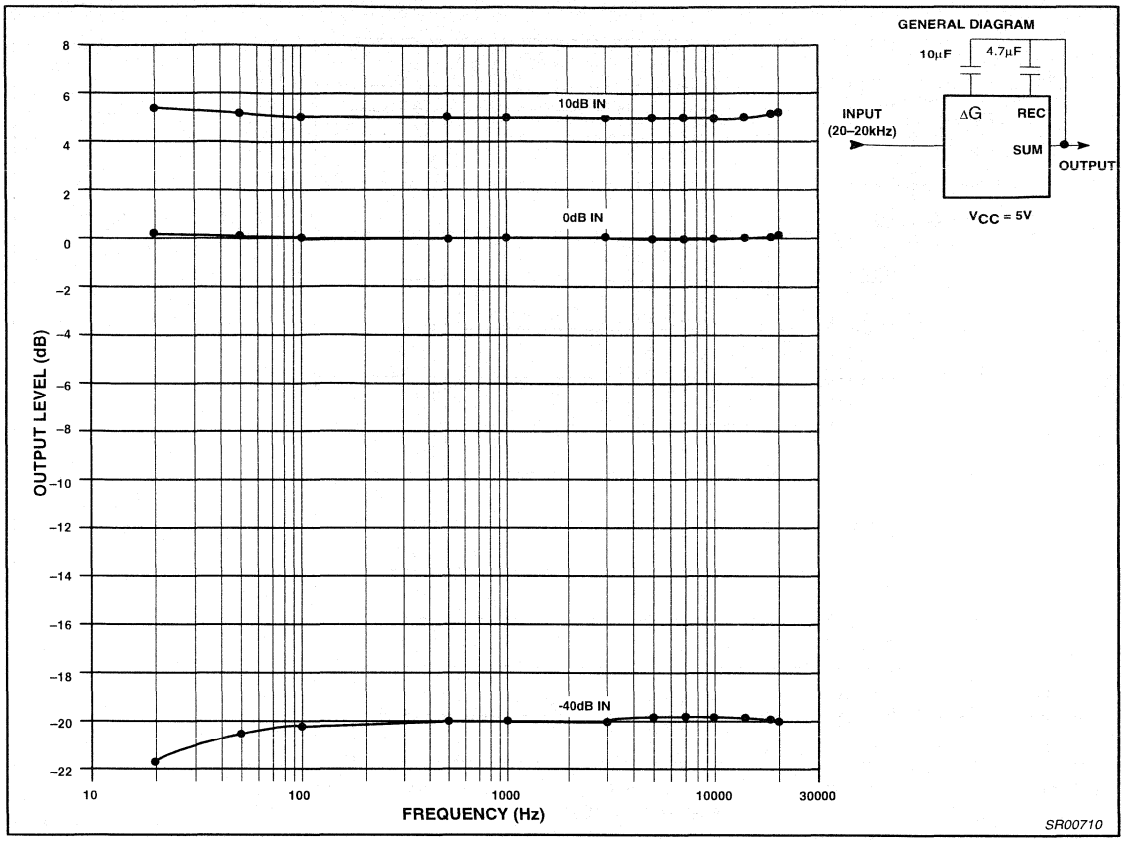


Figure 8. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

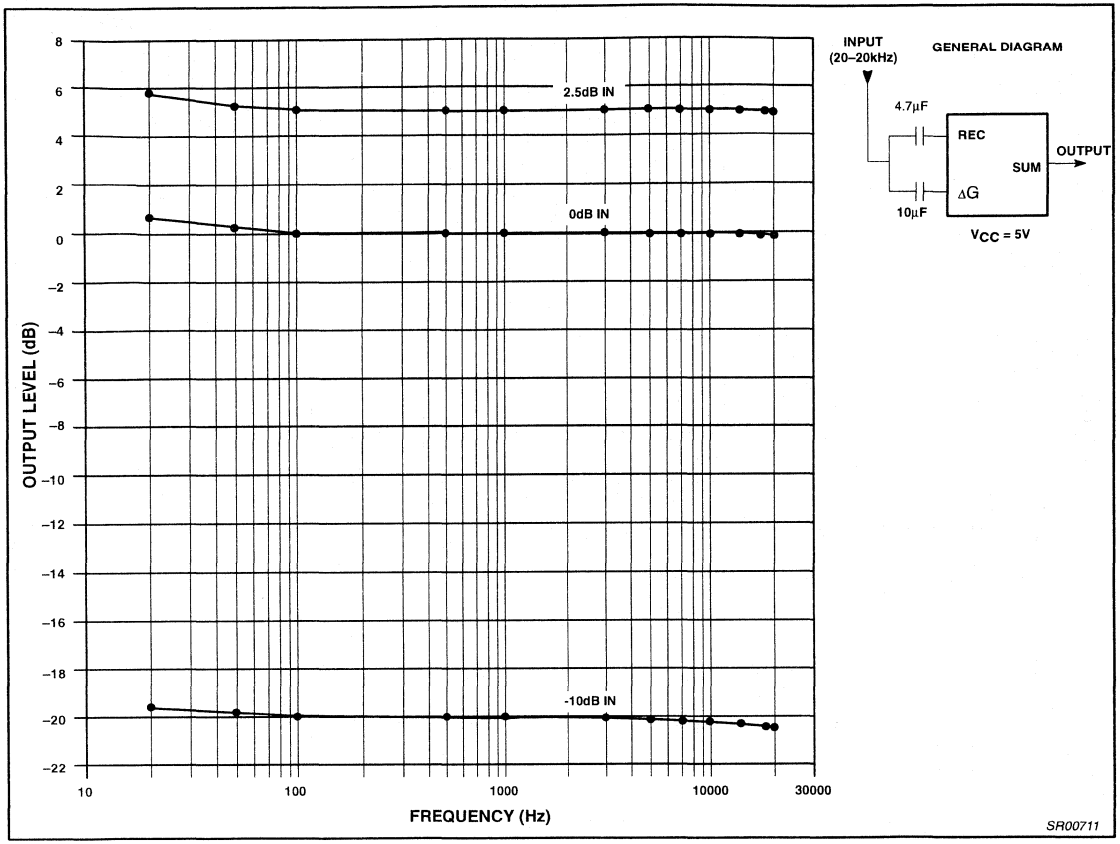


Figure 9. Expandor Output Frequency Response

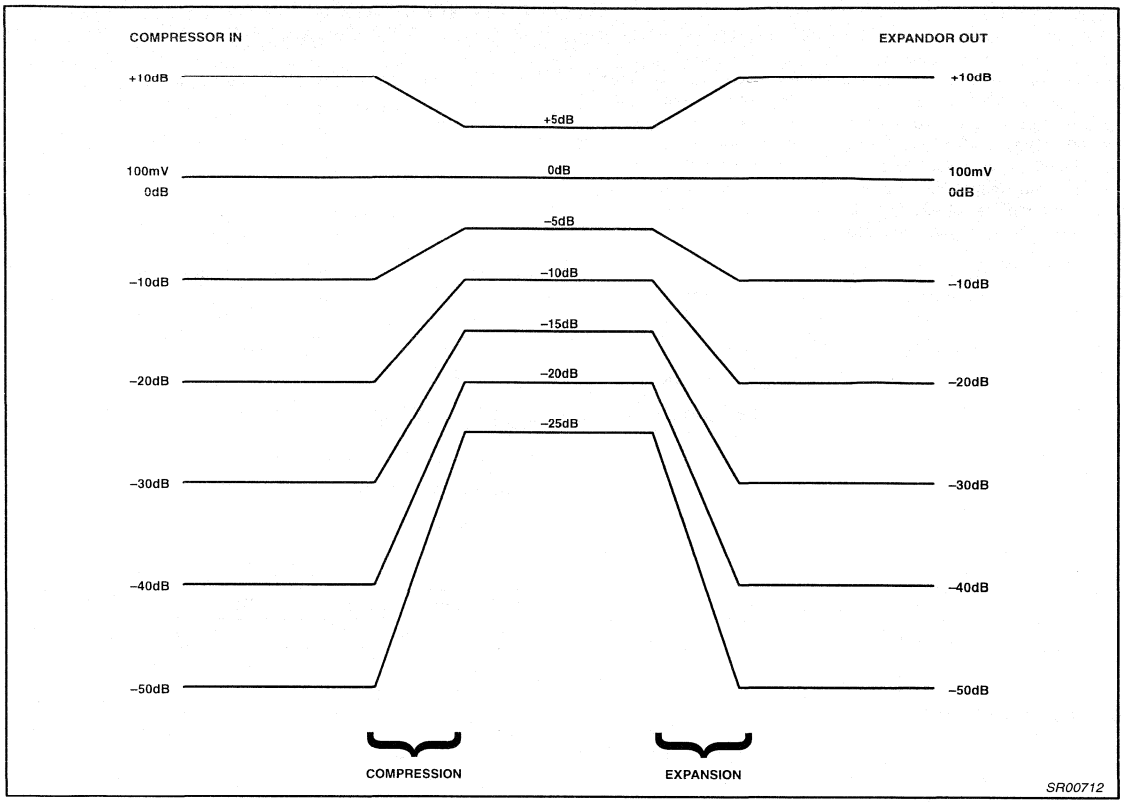


Figure 10. The Companding Function

Low voltage LNA and mixer - 1GHz | SA601

DESCRIPTION

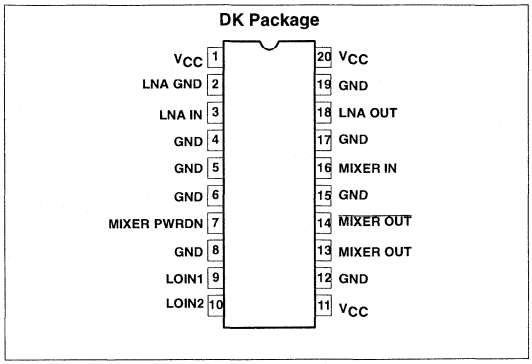
The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -2dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 9.5dB noise figure and IP3 of –2dBm at the input at 900MHz. The nominal current drawn from a single 3V supply is 7.4mA. The Mixer can be powered down to further reduce the supply current to 4.4mA.

FEATURES

- Low current consumption: 7.4mA nominal, 4.4mA with the mixer powered-down
- Outstanding LNA noise figure: 1.6dB at 900MHz
- High system power gain: 18dB (LNA + Mixer) at 900MHz
- Excellent gain stability versus temperature and supply voltage
- External >-7dBm LO can be used to drive the mixer

PIN CONFIGURATION

DK Package



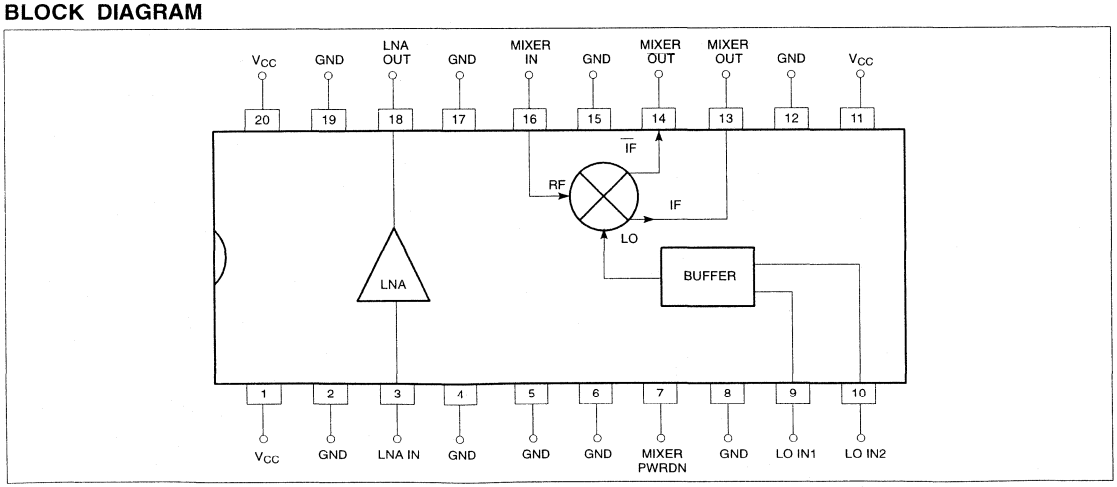
APPLICATIONS

- 900MHz cellular front-end (NADC, GSM, AMPS, TACS)
- 900MHz cordless front-end (CT1, CT2)
- 900MHz receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA601DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 9 and 10 are sensitive to electrostatic discharge (ESD).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current			7.4		mA
		Mixer power-down input low		4.4		
V_{LNA-IN}	LNA input bias voltage			0.78		V
$V_{LNA-OUT}$	LNA output bias voltage			2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -7dBm @ 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	881MHz	10	11.5	13	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	881MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	881MHz		-20		dB
S_{11}	Amplifier input match[1]	881MHz		-10		dB
S_{22}	Amplifier output match[1]	881MHz		-10		dB
P_{-1dB}	Amplifier input 1dB gain compression	881MHz		-16		dBm
IP3	Amplifier input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
NF	Amplifier noise figure	881MHz	1.3	1.6	1.9	dB
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	18.0	19.5	21.0	dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	5.0	6.5	8.0	dB
S_{11M}	Mixer input match[1]	881MHz		-10		dB
NF_M	Mixer SSB noise figure	881MHz	8.0	9.5	11.0	dB
P_{-1dB}	Mixer input 1dB gain compression	881MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
IP_{2INT}	Mixer input second order intercept	881MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	881MHz		-7		dB
P_{LO-IF}	LO feedthrough to IF	881MHz		-25		dB
P_{LO-RFM}	LO to mixer input feedthrough	881MHz		-38		dB
P_{LO-RF}	LO to LNA input feedthrough	881MHz		-40		dB
$P_{LNA-RFM}$	LNA output to mixer input	881MHz		-40		dB
P_{RFM-LO}	Mixer input to LO feedthrough	881MHz		-23		dB
LO_{IN}	LO drive level	964MHz		-7		dBm

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

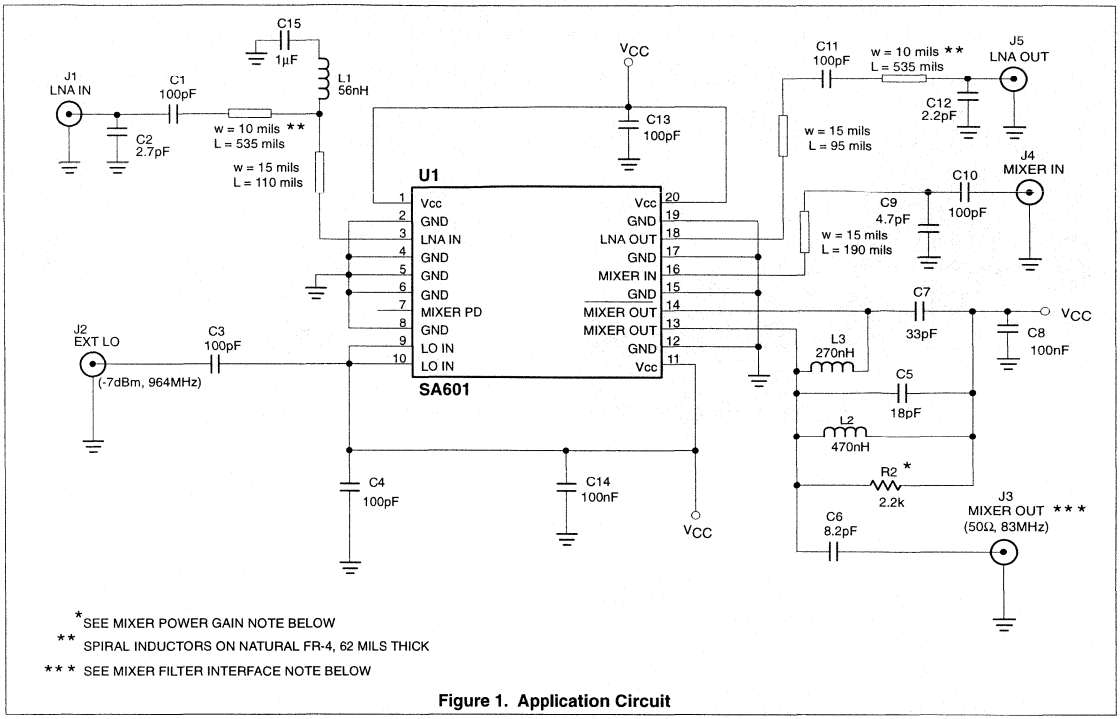


Figure 1. Application Circuit

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 881MHz using suggested L/C elements (Figure 1) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 881MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly decrease the NF and increase S_{21}.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from −40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

LO Drive Level: Resistor R1 can be replaced by an inductor of 4.7nH and C13 should be adjusted to achieve a good return loss at the LO port. Under this condition, the mixer will operate with less than -10dBm LO drive.

IP3 Performance: C9 between Pin 16 and ground can be removed to introduce 3dB mismatch loss, while improving the IP3 to +3dBm. The associated noise figure is 11dB.

Mixer

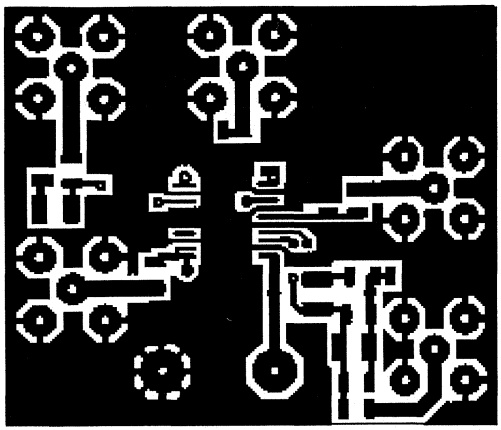
Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Power Gain: The gain can be increased by approximately 1.5dB by placing R2 across C7, instead of C5.

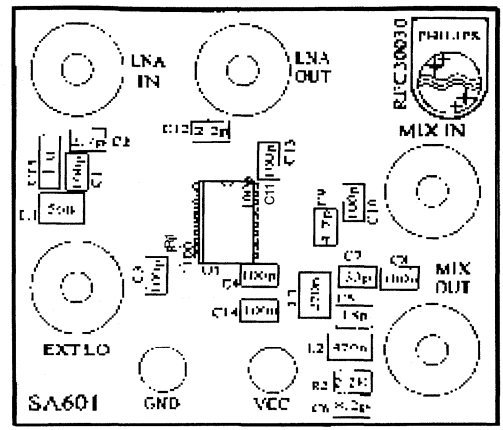
Power Down: The mixer can be disabled by connecting Pin 7 to ground. When the mixer is disabled, 3mA is saved.

Power Combining: The mixer output circuit features passive power combining (patent pending) to optimize conversion gain and noise figure performance without using extra DC current or degrading the IP3. For IF frequencies significantly different than 83MHz, the component values must be altered accordingly.

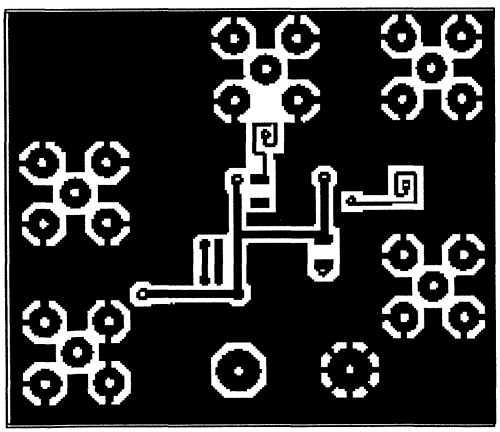
Filter Interface: For system integration where a high impedance filter of 1kΩ is to be cascaded at the mixer IF output, capacitors C5 and C6 need to be changed to 27pF and 1000pF, respectively.



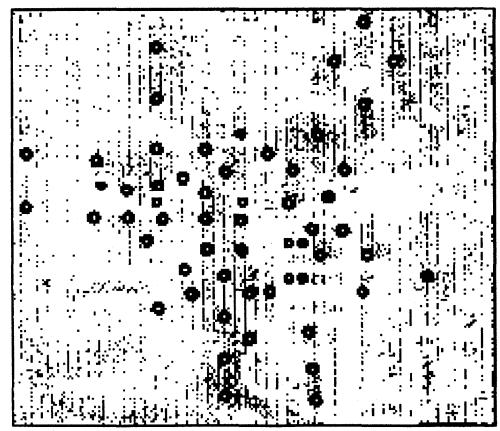
Top View



Silk Screen



Bottom View



Via Layer

Figure 2. SA601 Demoboard Layout (Not Actual Size)

TYPICAL PERFORMANCE CHARACTERISTICS

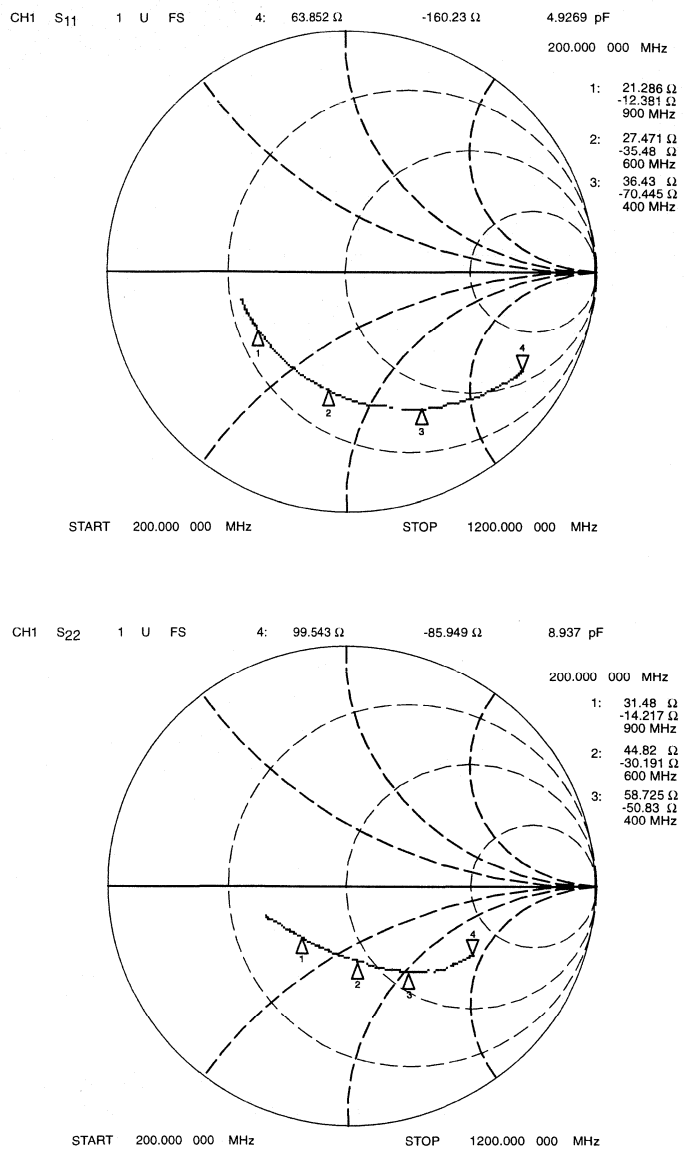


Figure 3. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

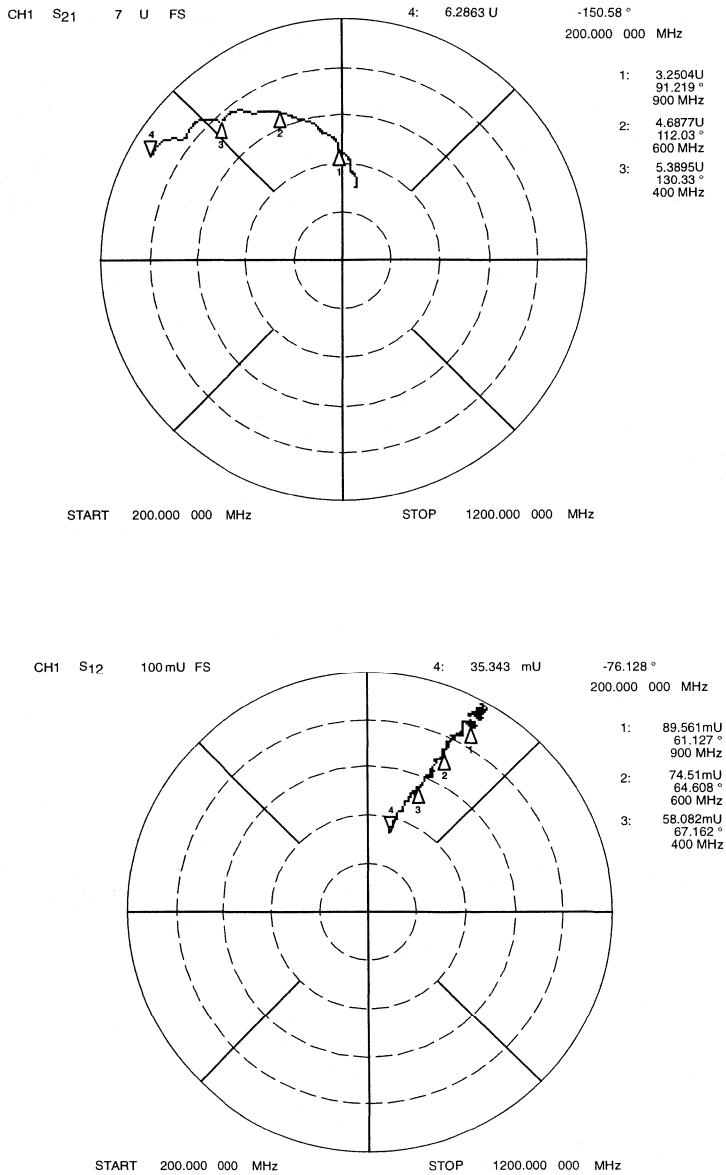


Figure 4. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

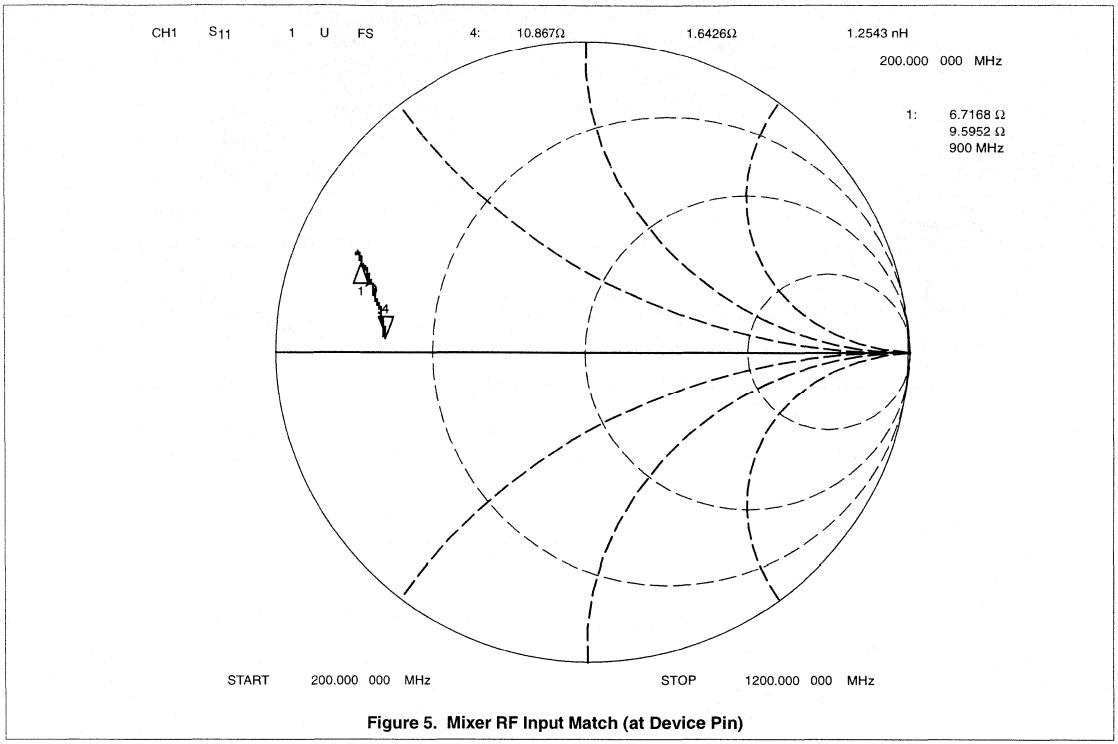


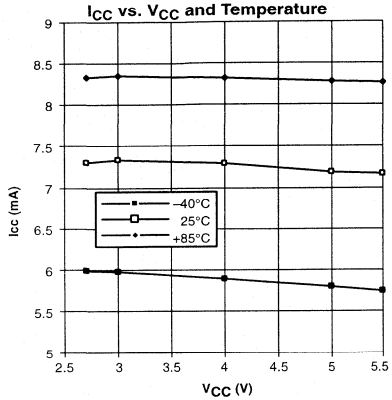
Figure 5. Mixer RF Input Match (at Device Pin)

Table 1. Typical LNA and Mixer S-Parameters

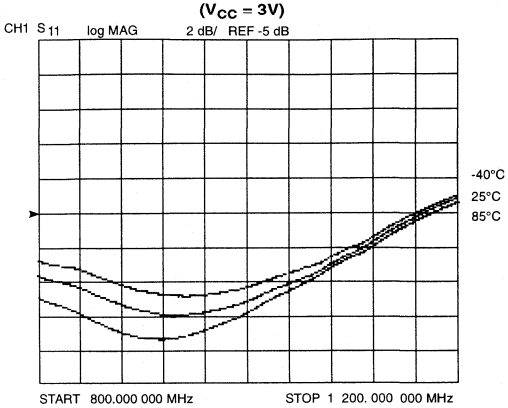
	LNA				Mixer
f	**S_{11}**	**S_{22}**	**S_{21}**	**S_{12}**	**S_{11}**
200MHz	63.852Ω – j 160.23Ω	99.543Ω – j 85.949Ω	6.2863U ∠ 150.58°	35.343mU ∠ 76.128°	10.867Ω + j 1.6426Ω
300MHz	44.879Ω – j 101.69Ω	73.387Ω – j 67.707Ω	5.8096U ∠ 140.47°	47.946mU ∠ 71.169°	10.4Ω + j 3.4609Ω
400MHz	36.43Ω – j 70.445Ω	58.725Ω – j 50.83Ω	5.3895U ∠ 130.33°	58.082mU ∠ 67.162°	10.067Ω + j 4.897Ω
500MHz	30.395Ω – j 48.393Ω	49.928Ω – j 38.813Ω	5.0428U ∠ 120.5°	66.44mU ∠ 66.388°	9.394Ω + j 6.0142Ω
600MHz	27.471Ω – j 35.48Ω	44.82Ω – j 30.191Ω	4.6877U ∠ 112.03°	74.51mU ∠ 64.608°	8.8945Ω + j 7.2227Ω
700MHz	24.428Ω – j 25Ω	39.268Ω – j 24.502Ω	4.2409U ∠ 104.44°	82.235mU ∠ 65.002°	8.1353Ω + j 8.1597Ω
800MHz	22.434Ω – j 17.255Ω	34.664Ω – j 18.59Ω	3.7491U ∠ 97.765°	86.582mU ∠ 62.743°	7.976Ω + j 9.1958Ω
900MHz	21.286Ω – j 12.381Ω	31.48Ω – j 14.217Ω	3.2504U ∠ 91.219°	89.561mU ∠ 61.127°	6.7168Ω + j 9.5952Ω
1000MHz	20.261Ω – j 8.7109Ω	27.887Ω – j 10.77Ω	2.8785U ∠ 84.957°	95.135mU ∠ 60.539°	6.2393Ω + j 10.271Ω
1100MHz	19.718Ω – j 6.252Ω	25.741Ω – j 8.2607Ω	2.5752U ∠ 82.893°	97.348mU ∠ 62.202°	6.0791Ω + j 10.571Ω
1200MHz	19.101Ω – j 4.9316Ω	23.584Ω – j 6.2715Ω	2.1386U ∠ 80.257°	96.558mU ∠ 61.563°	5.8185Ω + j 10.288Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

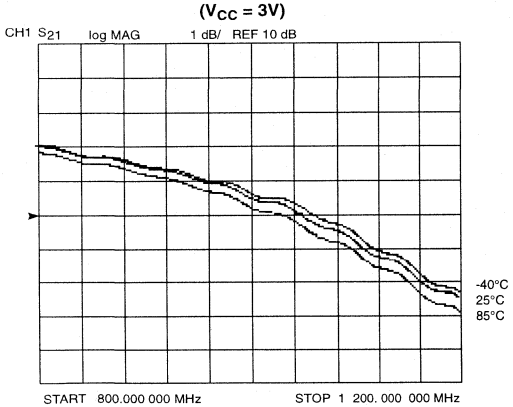
I_{CC} vs. V_{CC} and Temperature



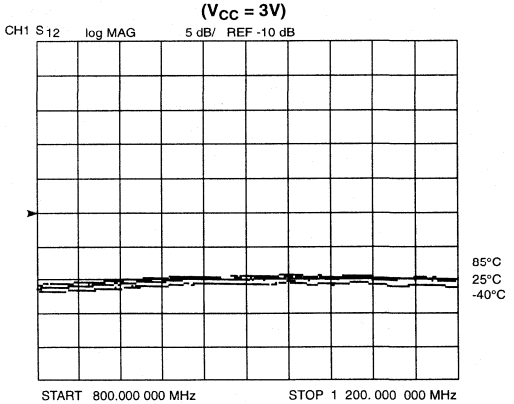
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



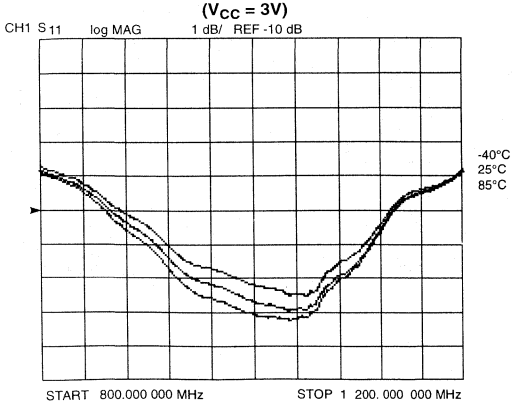
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



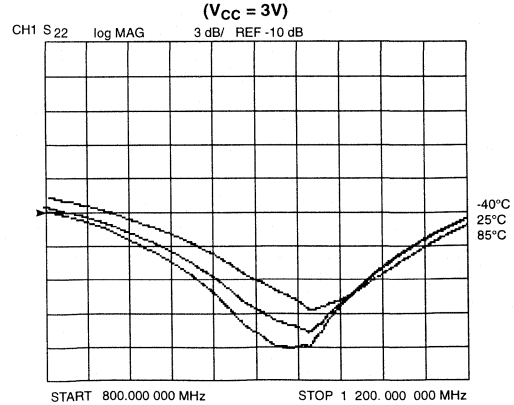
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



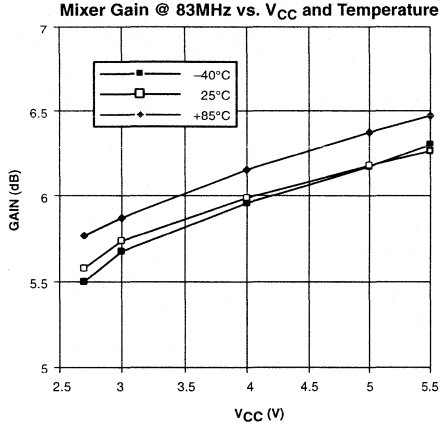
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)



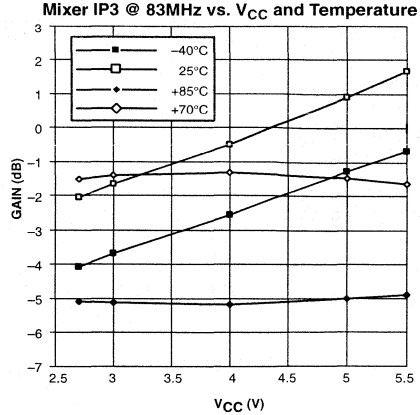
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)



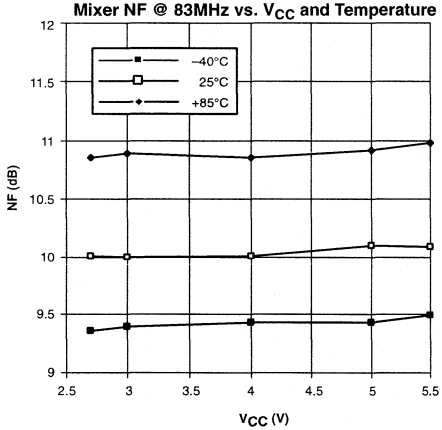
Mixer Gain @ 83MHz vs. V_{CC} and Temperature



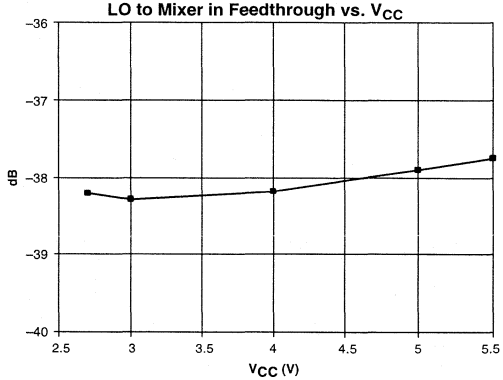
Mixer IP3 @ 83MHz vs. V_{CC} and Temperature



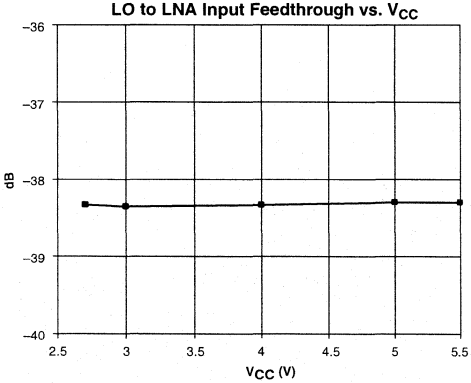
Mixer NF @ 83MHz vs. V_{CC} and Temperature



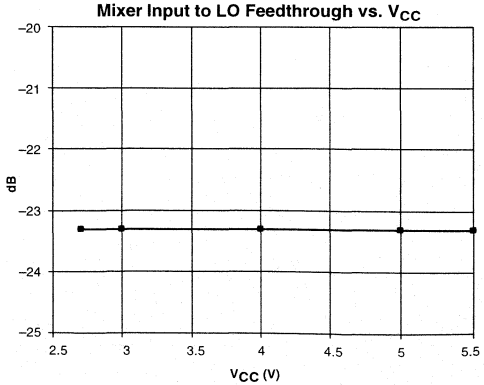
LO to Mixer in Feedthrough vs. V_{CC}



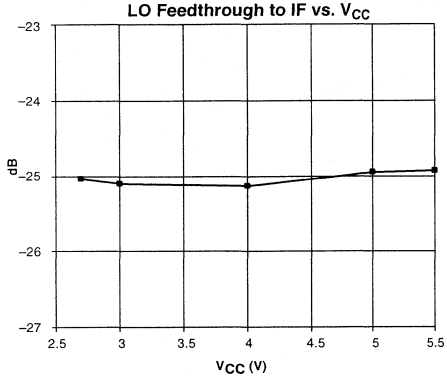
LO to LNA Input Feedthrough vs. V_{CC}



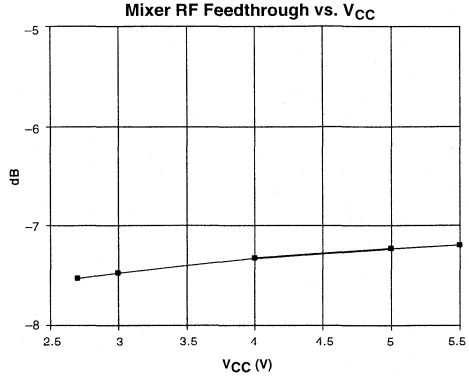
Mixer Input to LO Feedthrough vs. V_{CC}



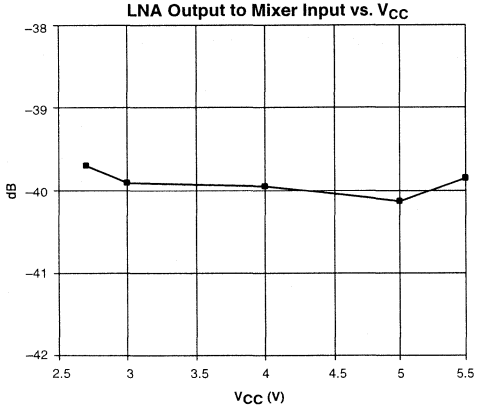
LO Feedthrough to IF vs. V_{CC}



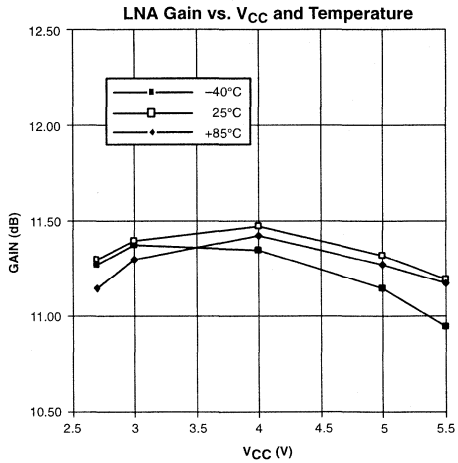
Mixer RF Feedthrough vs. V_{CC}



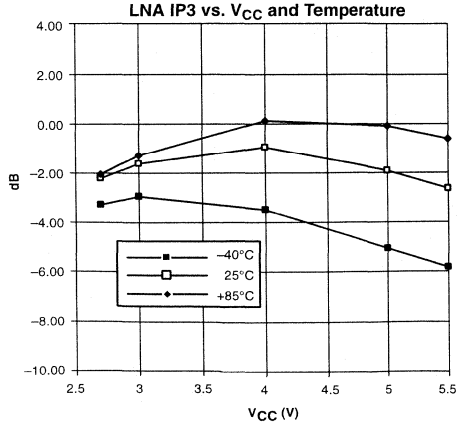
LNA Output to Mixer Input vs. V_{CC}



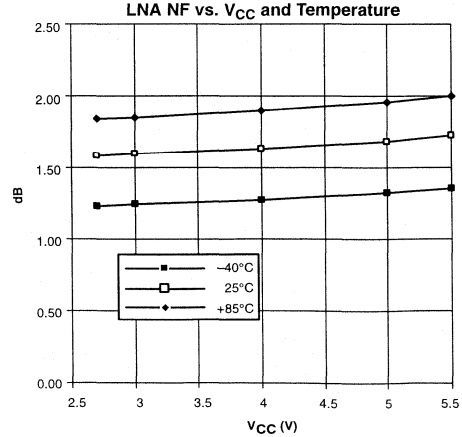
LNA Gain vs. V_{CC} and Temperature



LNA IP3 vs. V_{CC} and Temperature



LNA NF vs. V_{CC} and Temperature



Double-balanced mixer and oscillator SA602A

DESCRIPTION

The SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

PIN CONFIGURATION

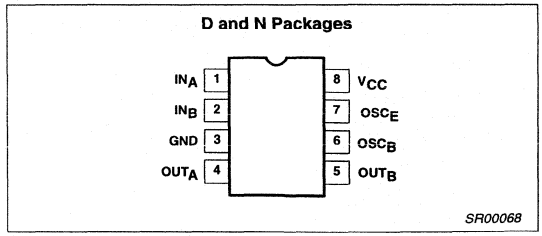


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA602AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA602AD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

BLOCK DIAGRAM

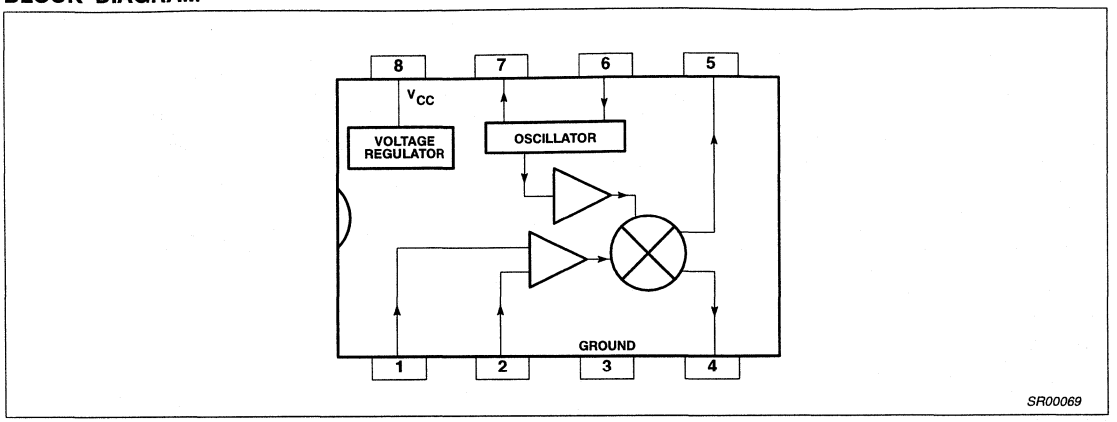


Figure 2. Block Diagram

AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the SA602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV$_{P-P}$.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 8 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

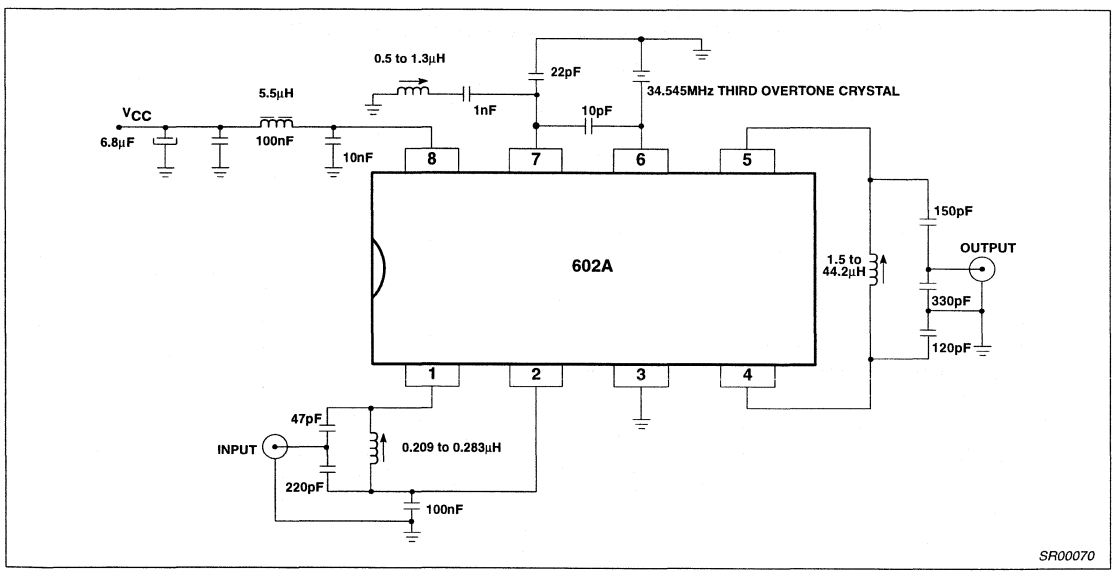


Figure 3. Test Configuration

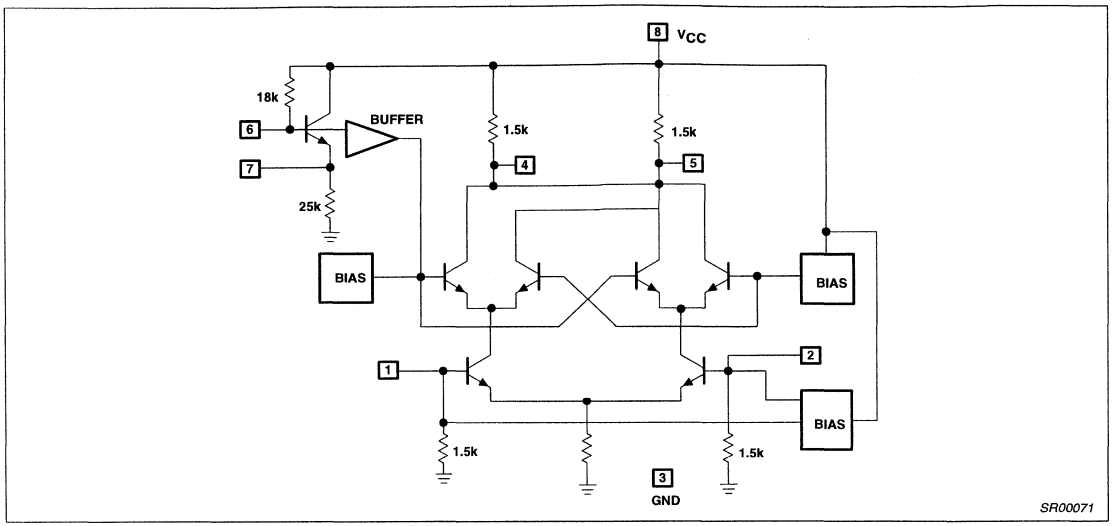


Figure 4. Equivalent Circuit

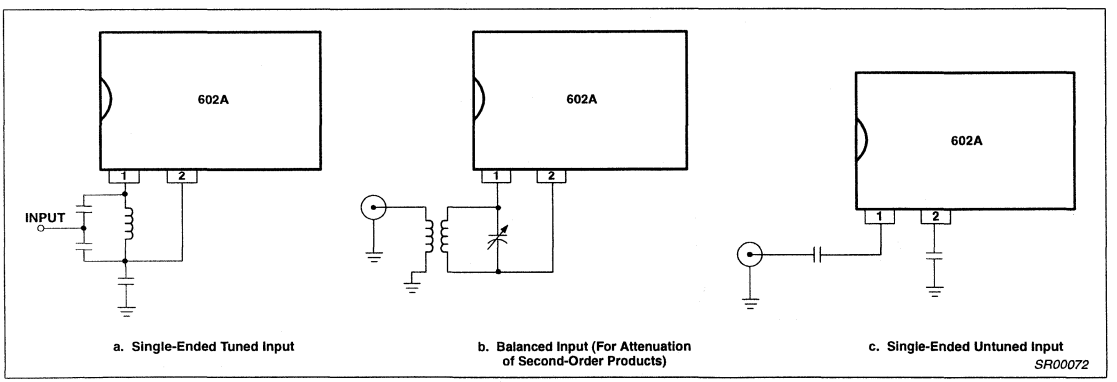


Figure 5. Input Configuration

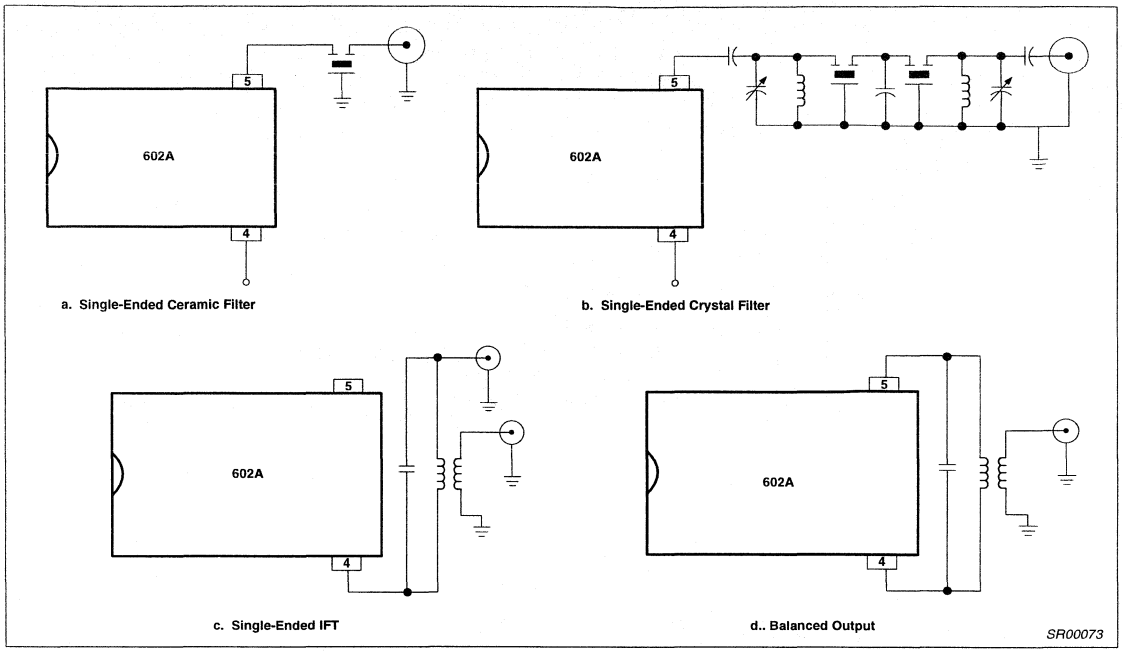


Figure 6. Output Configuration

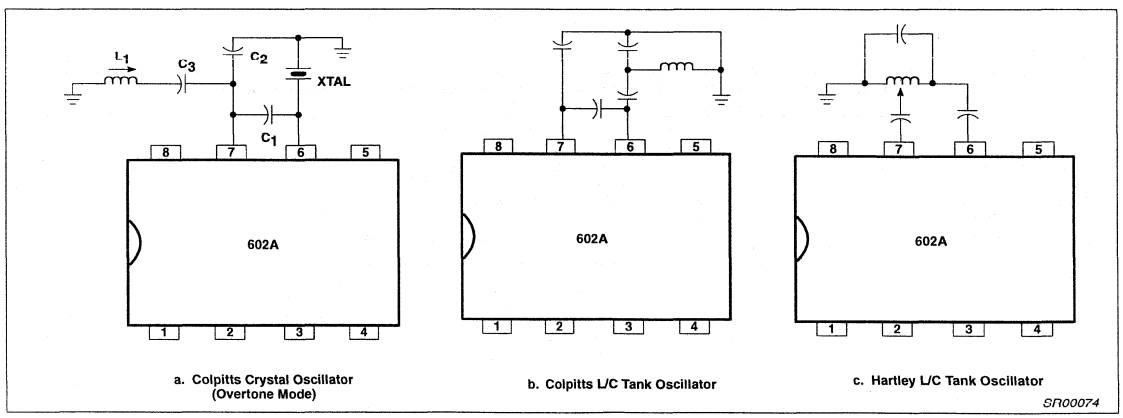


Figure 7. Oscillator Circuits

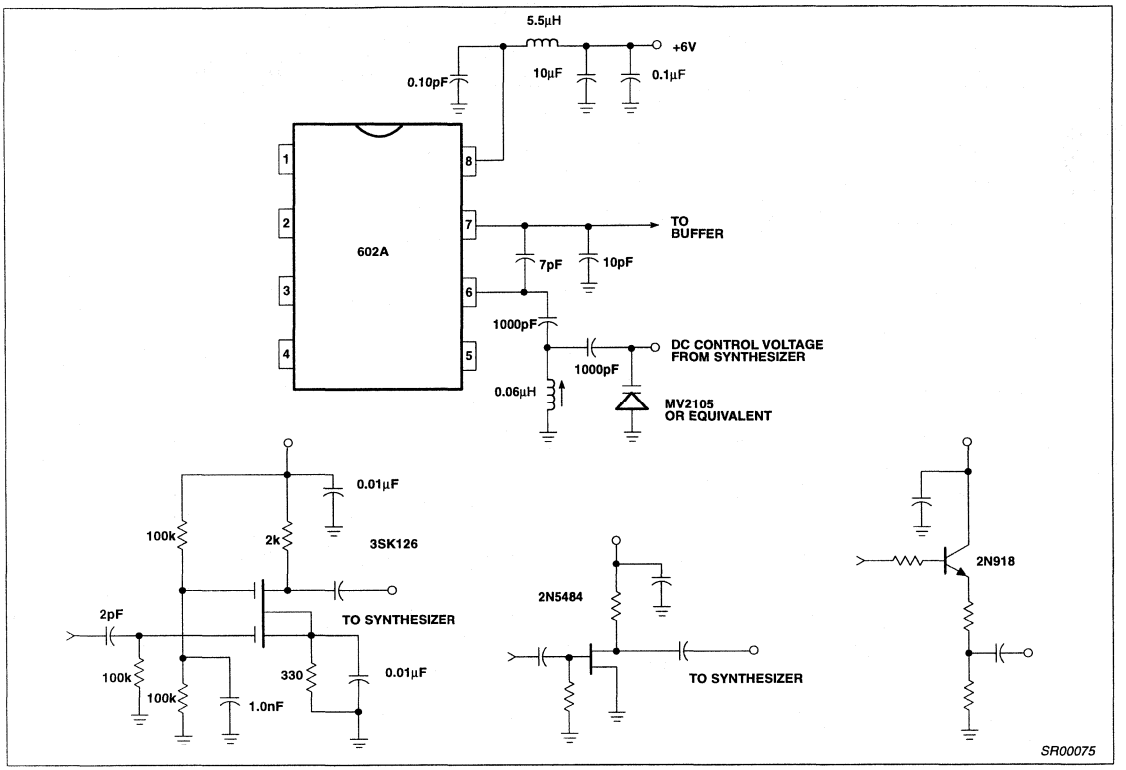


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

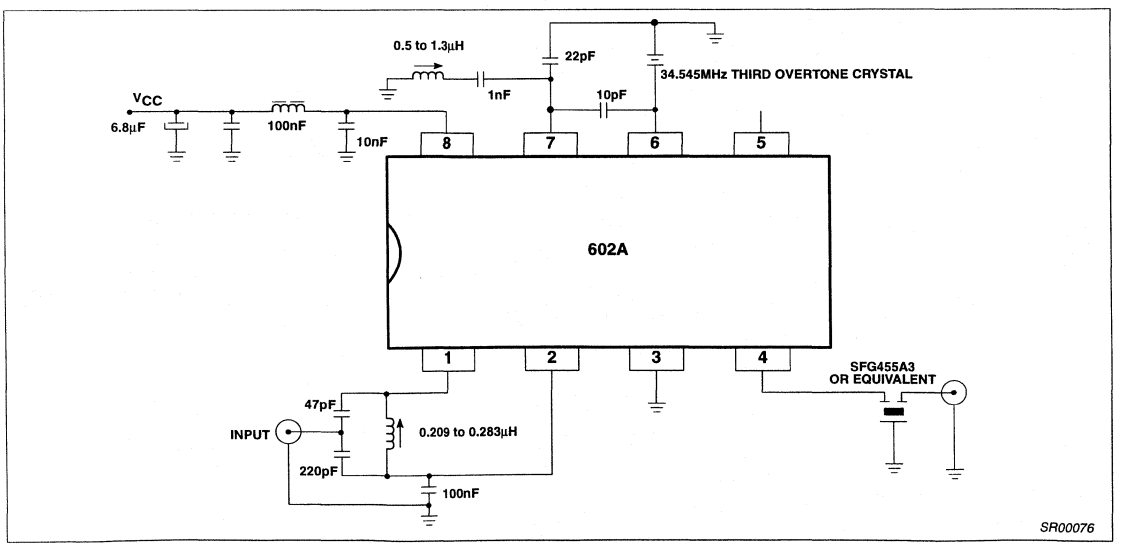


Figure 9. Typical Application for Cellular Radio

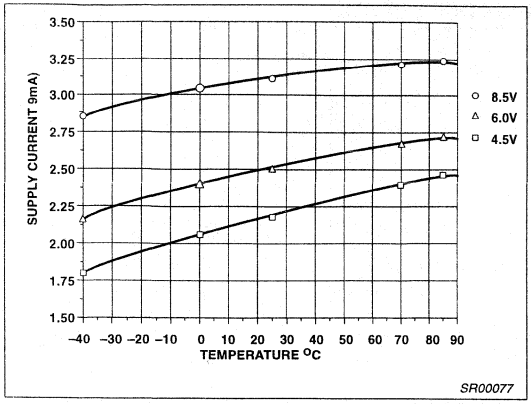


Figure 10. I_{CC} vs Supply Voltage

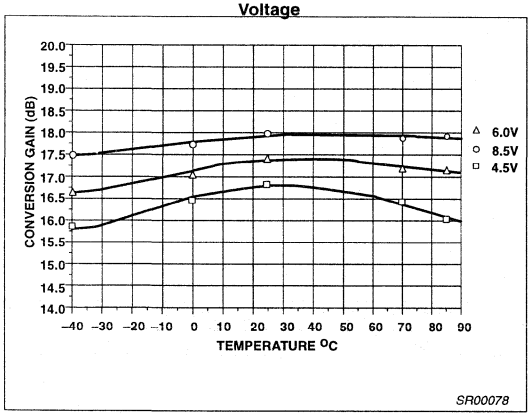


Figure 11. Conversion Gain vs Supply Voltage

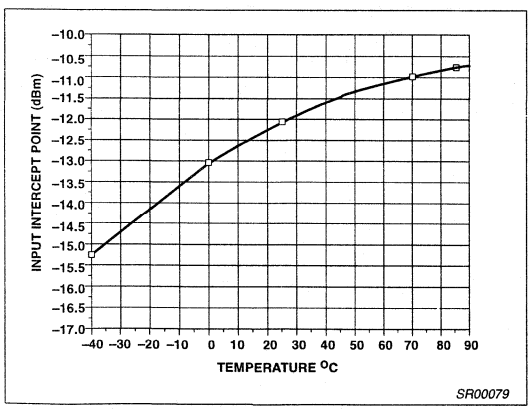


Figure 12. Third-Order Intercept Point

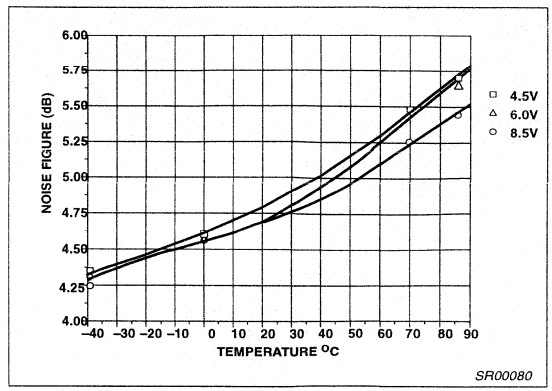


Figure 13. Noise Figure

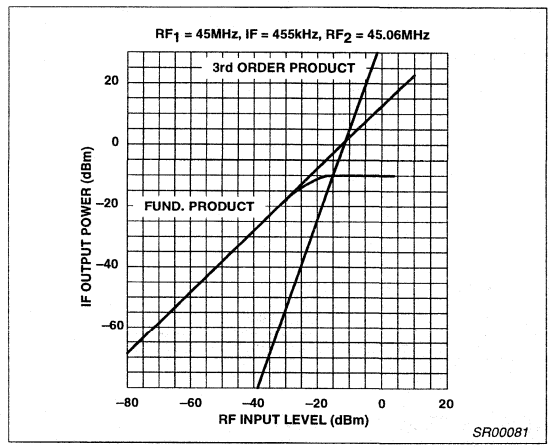


Figure 14. Third-Order Intercept and Compression

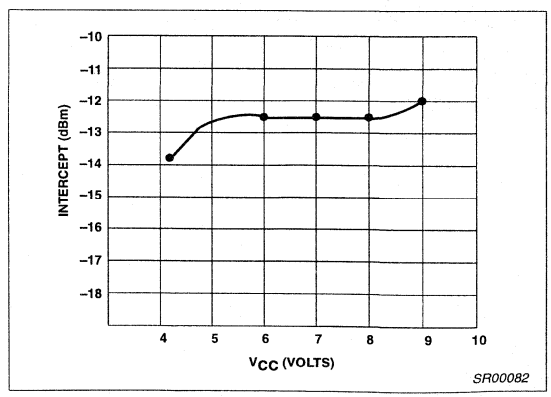


Figure 15. Input Third-Order Intermod Point vs V_{CC}

High performance low power FM IF system SA604A

DESCRIPTION

The SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the SA604. The SA604A is available in a 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

PIN CONFIGURATION

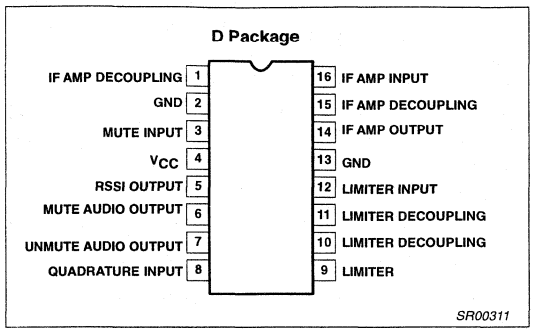


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA604AD	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA604A	40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W

BLOCK DIAGRAM

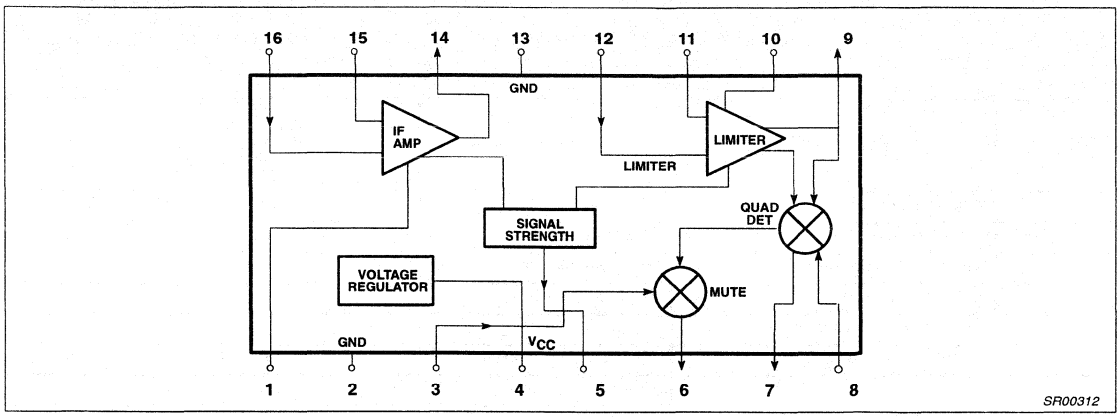


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA604A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

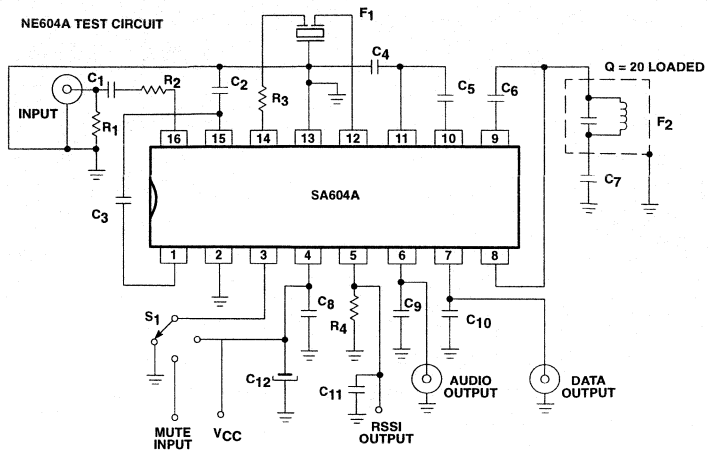
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA604A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		dB
	Recovered audio level	15nF de-emphasis	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	RSSI output[1]	RF level = -118dBm	0	160	650	mV
		RF level = -68dBm	1.9	2.65	3.1	V
		RF level = -18dBm	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

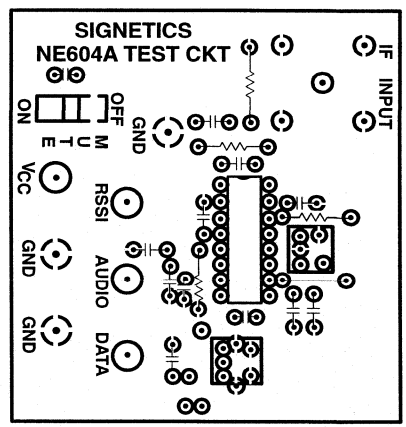
1. SA604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

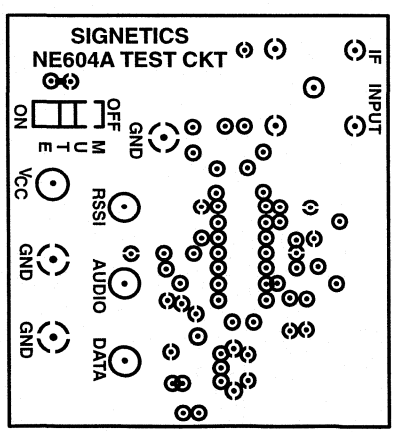
SA604 (50)	SA604A (1.5k)/SA605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

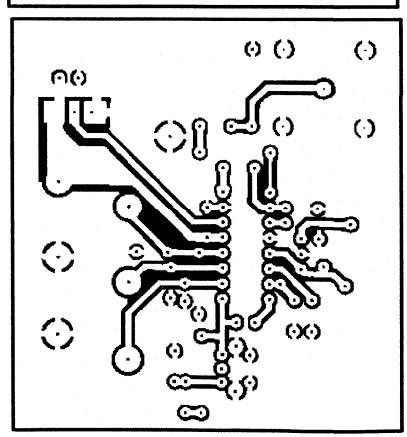
The SA605 and SA604A are both derived from the same basic die. The SA605 performance plots are directly applicable to the SA604A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film







SR00313

Figure 3. SA604A Test Circuit

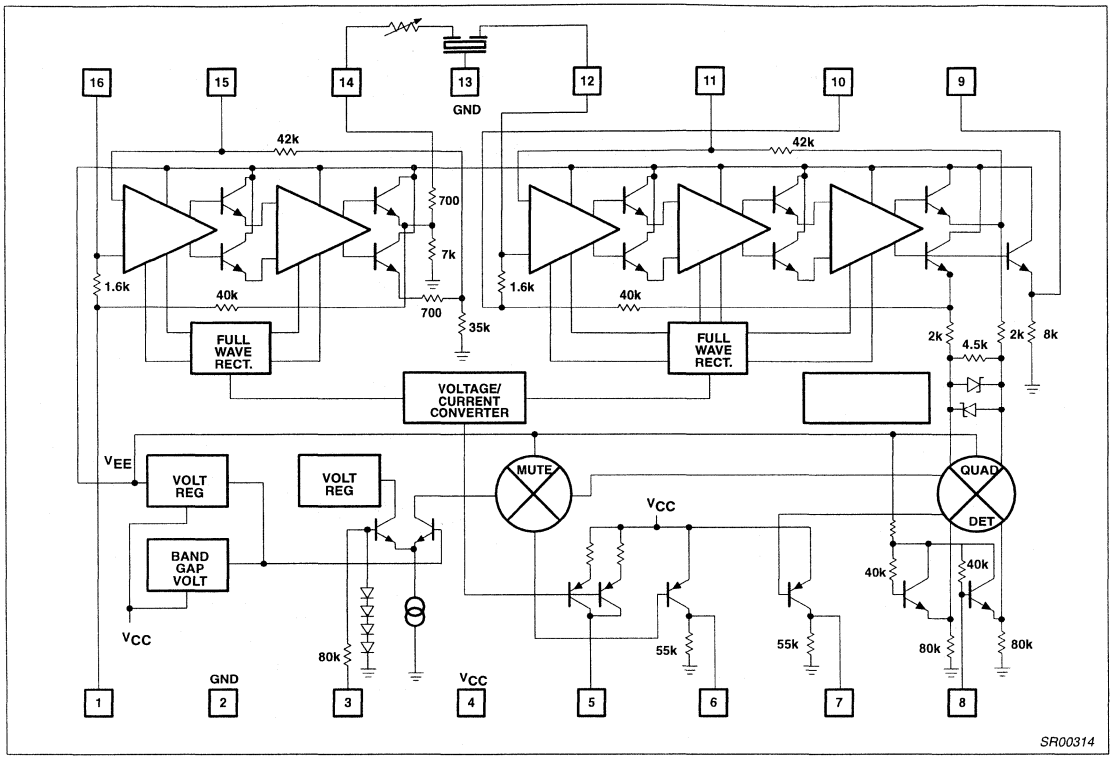


Figure 4. Equivalent Circuit

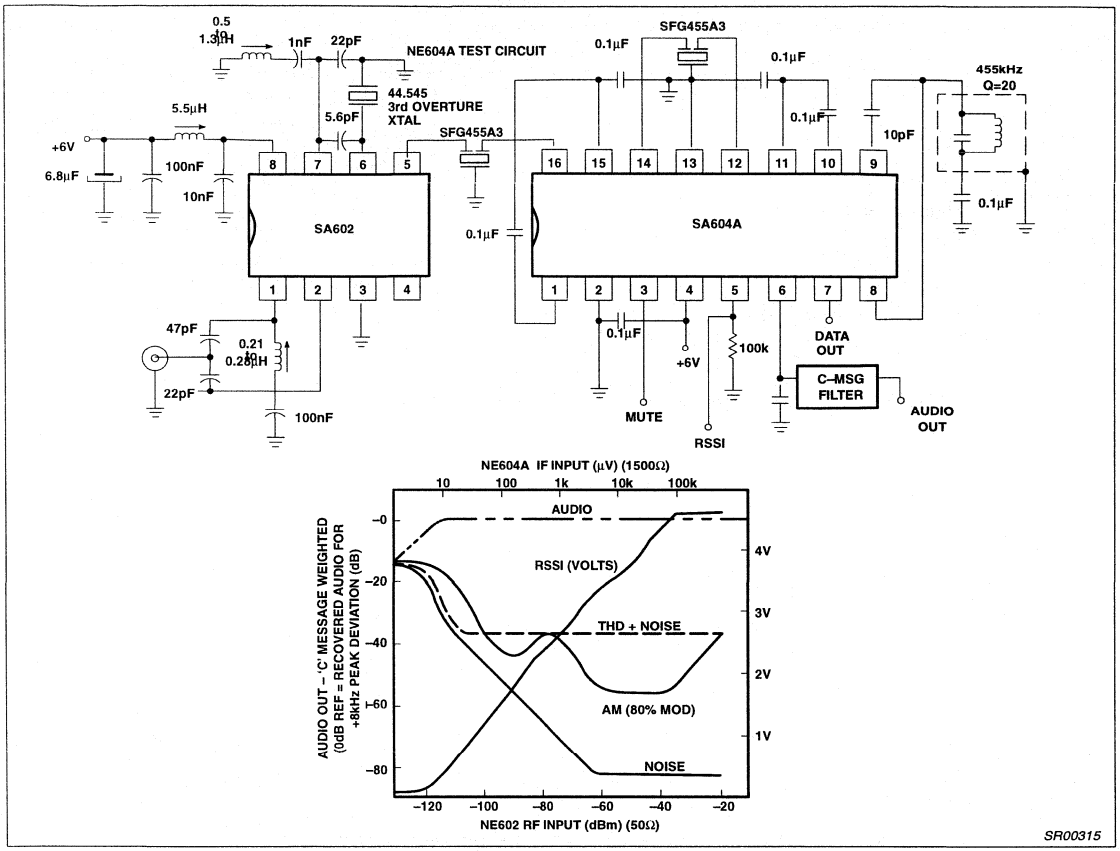


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

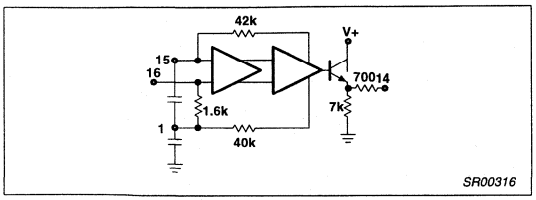


Figure 6. First Limiter Bias

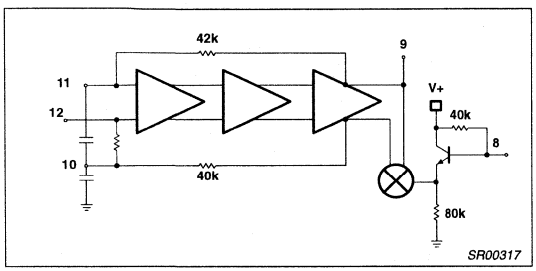


Figure 7. Second Limiter and Quadrature Detector

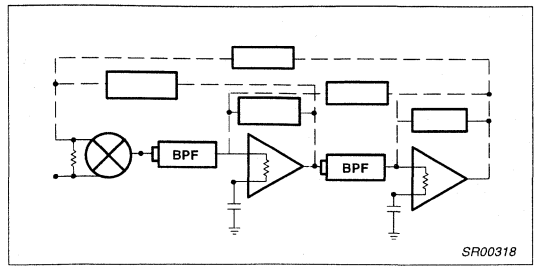


Figure 8. Feedback Paths

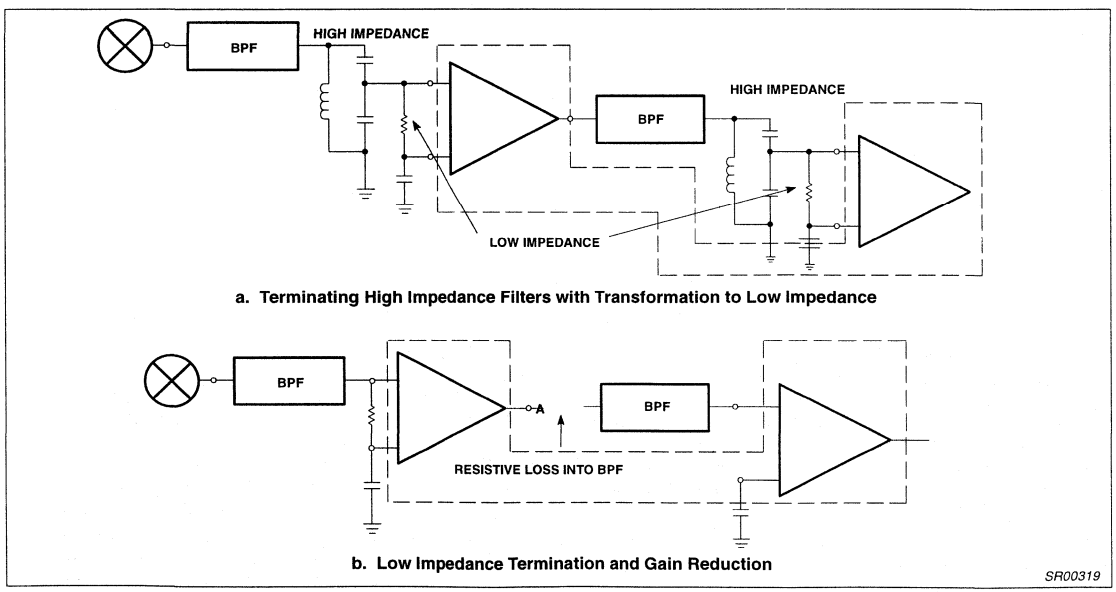


Figure 9. Practical Termination

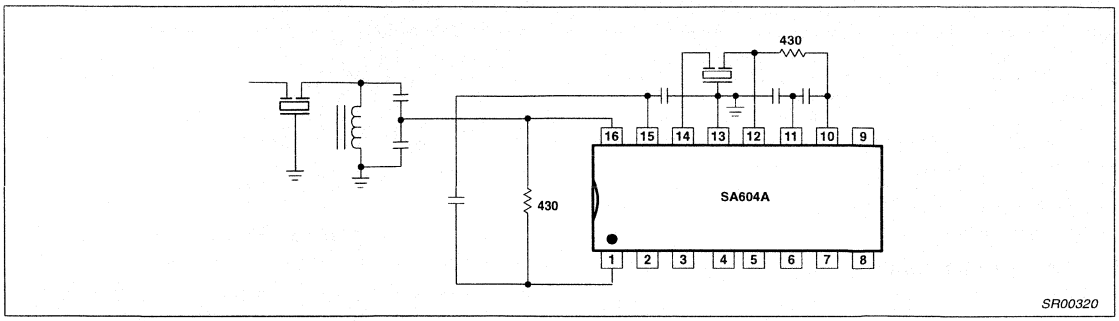


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the SA604A IF amplifiers, which is not specified, is low phase shift. The SA604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the SA604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the SA604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for SA604A

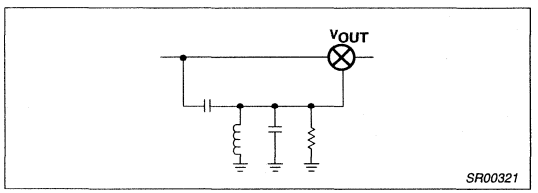


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \quad (4)$$

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}\,A^2\,\text{Cos}\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2}\,A^2\,\text{Sin}\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\,\frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output

differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the SA604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the SA604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

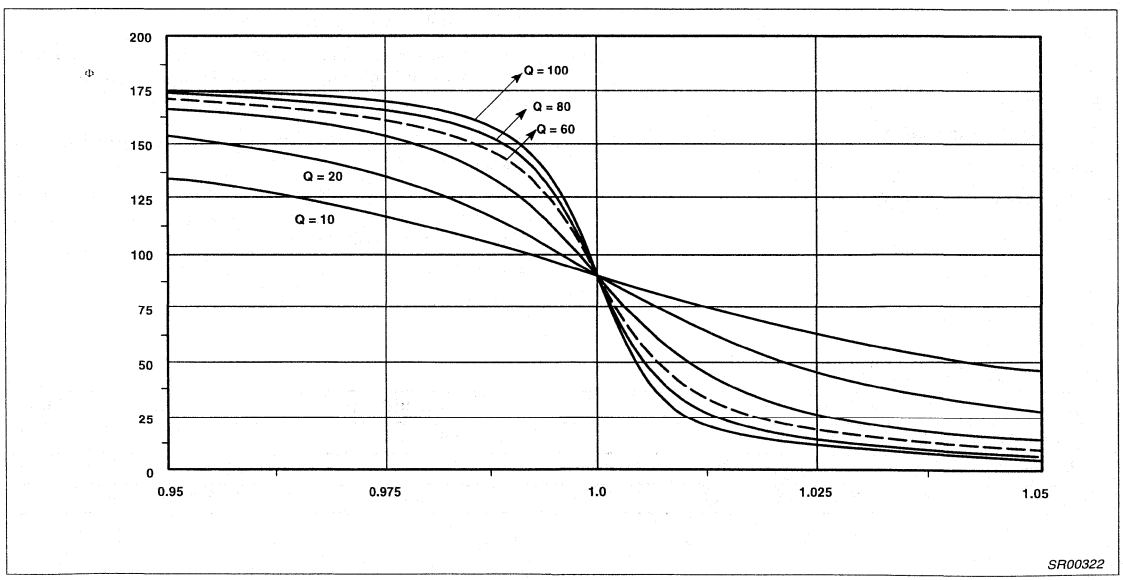


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

High performance low power mixer FM IF system SA605

DESCRIPTION

The SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The SA605 combines the functions of Signetics' SA602 and SA604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The SA605 and SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the SA605. Both the SA605 and SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

PIN CONFIGURATION

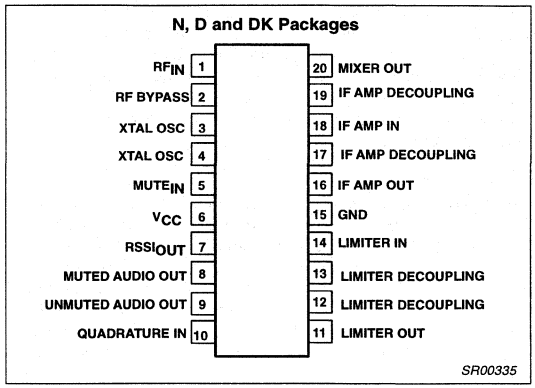


Figure 1. Pin Configuration

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA605N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA605D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA605DK	SOT266-1

BLOCK DIAGRAM

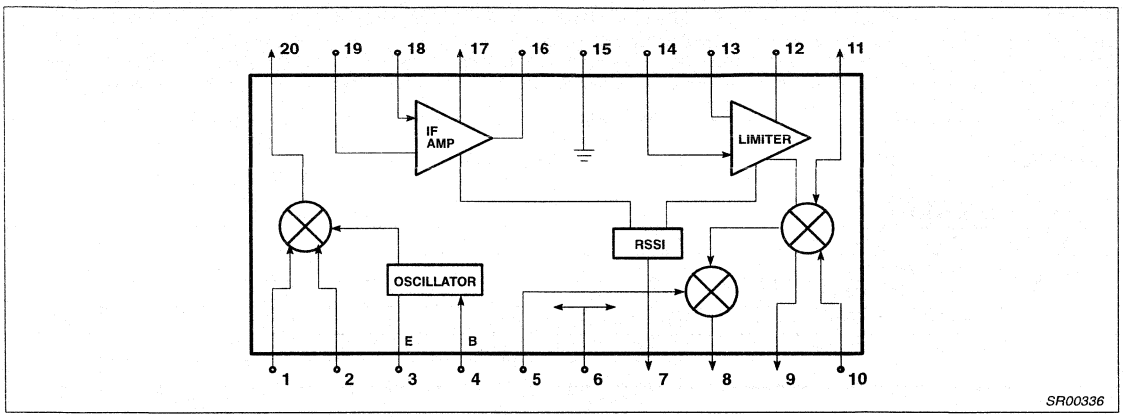


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA605	–40 to +85	°C
θ_{JA}	Thermal impedance D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA605			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA605			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10	13	15	dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113		dBm
	AM rejection	80% AM 1kHz	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480		mV
	SINAD sensitivity	RF level -118dB		16		dB
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	650	mV
		IF level = -68dBm	1.9	2.5	3.1	V
		IF level = -18dBm	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

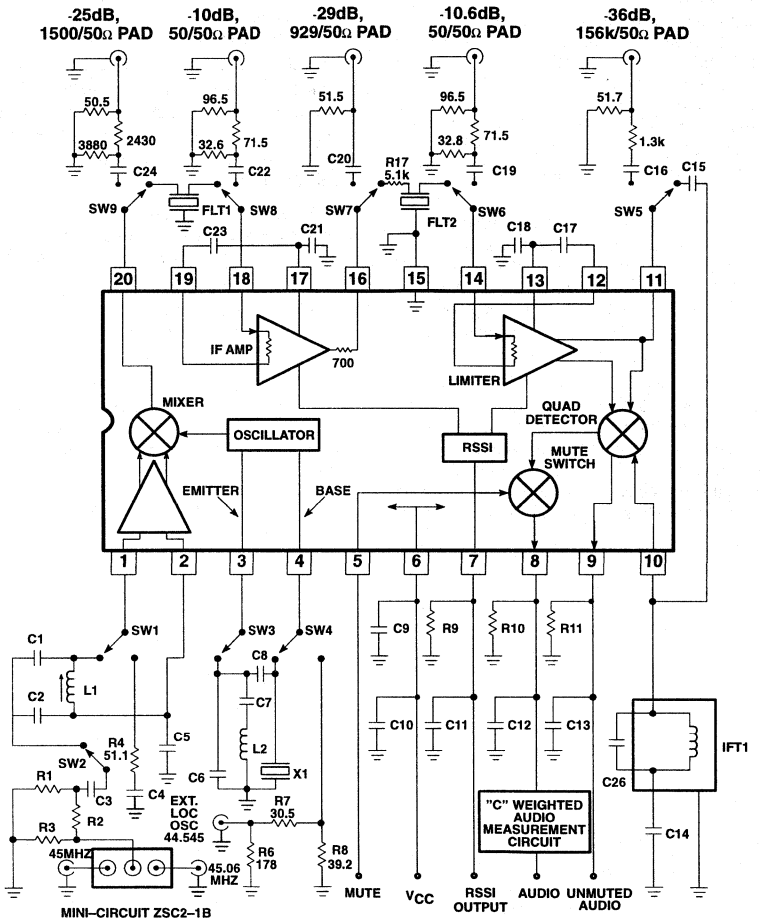
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



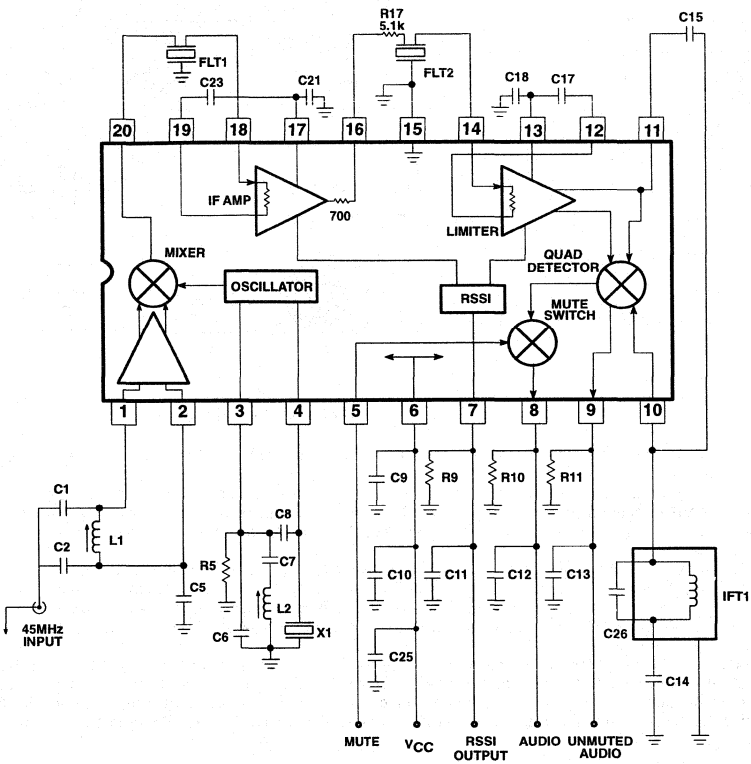
Automatic Test Circuit Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

SR00337

Figure 3. SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

SR00338

Figure 4. SA605 45MHz Application Circuit

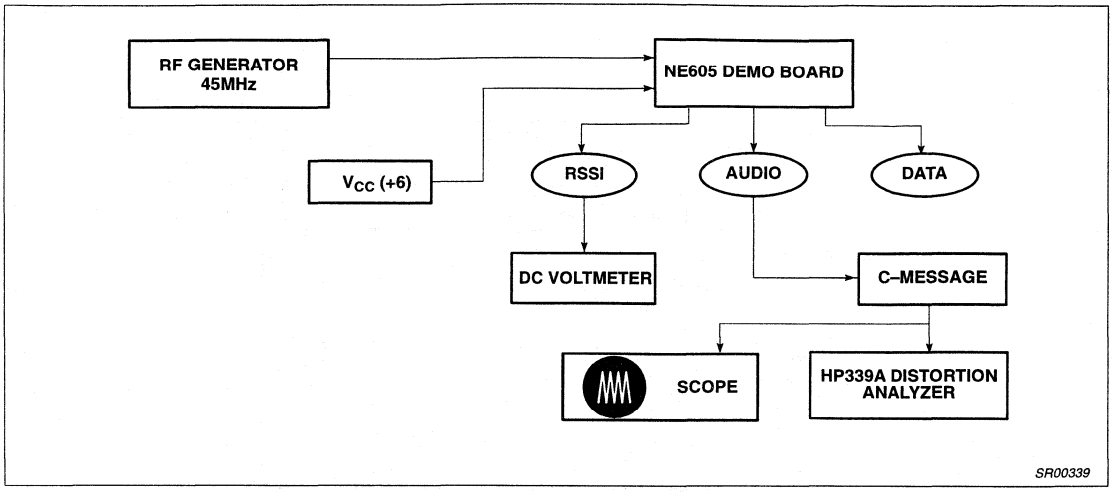


Figure 5. SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

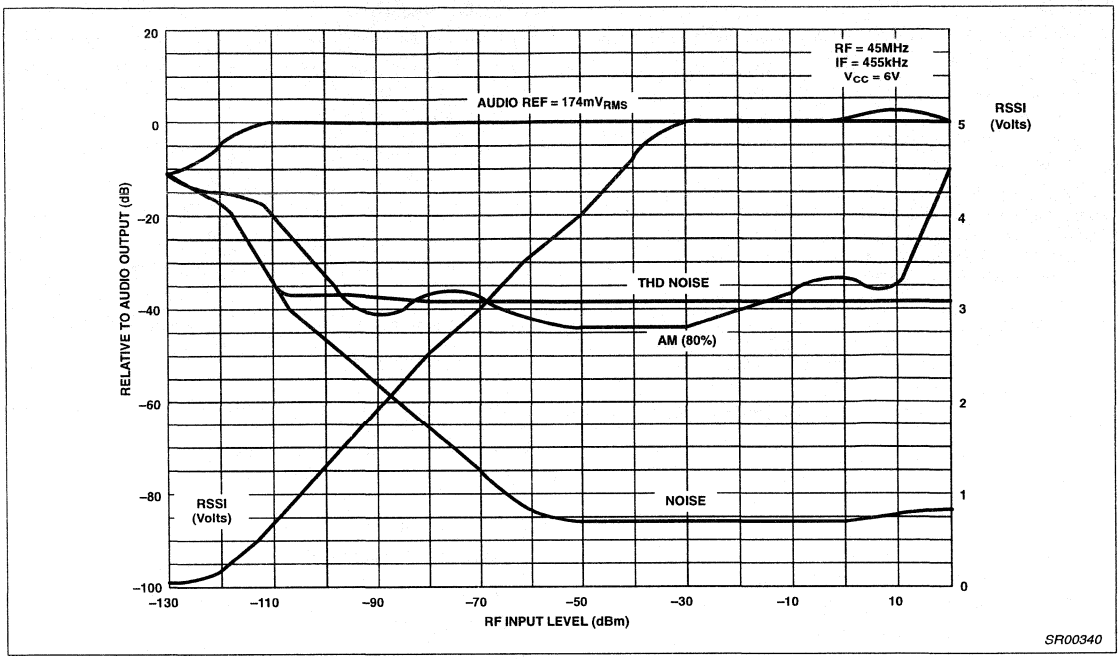


Figure 6. SA605 Application Board at 25°C

Low-voltage high performance mixer FM IF system SA606

DESCRIPTION

The SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA606 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs

PIN CONFIGURATION

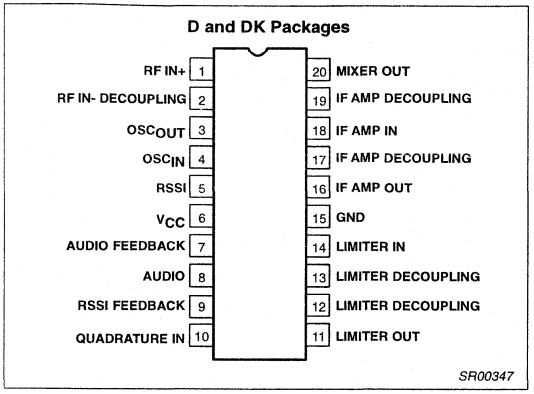


Figure 1. Pin Configuration

- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA606D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA606DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C
θ_{JA}	Thermal impedance D package DK package	90 117	°C/W

BLOCK DIAGRAM

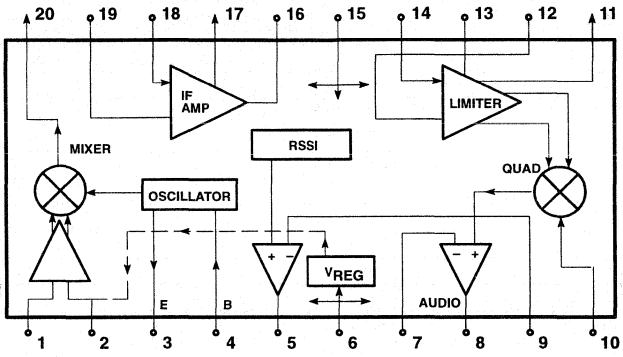


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion voltage gain	Matched 14.5dBV step-up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level -110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
THD	Total harmonic distortion		-35	-50		dB
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_9 = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	1.80	V
		RF level = -23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

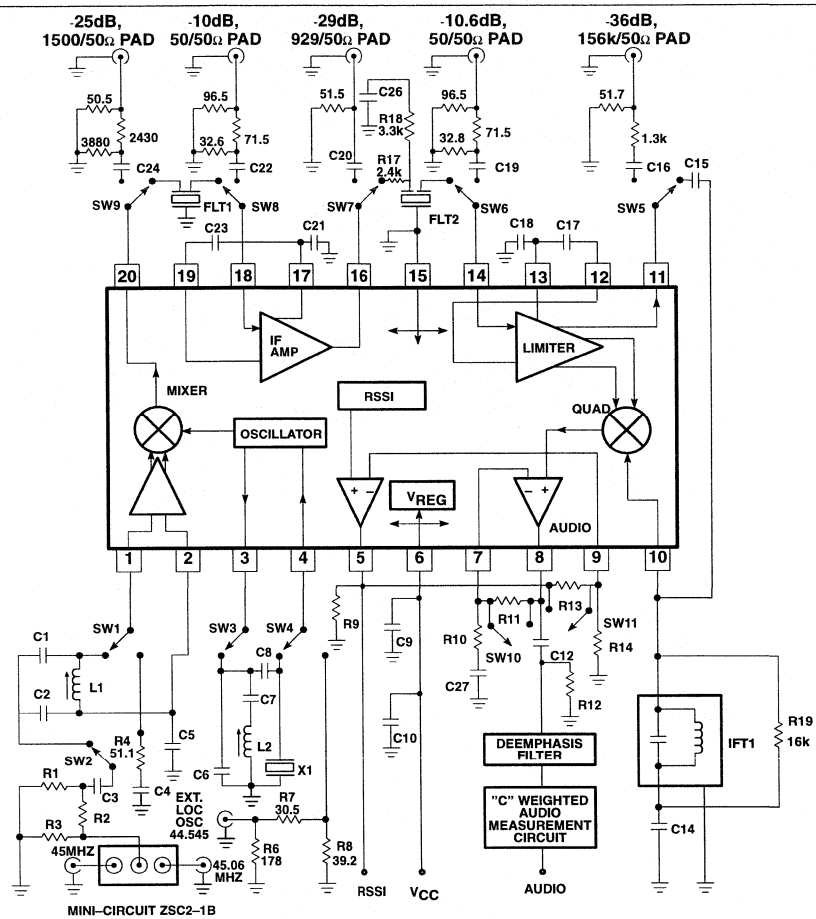
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



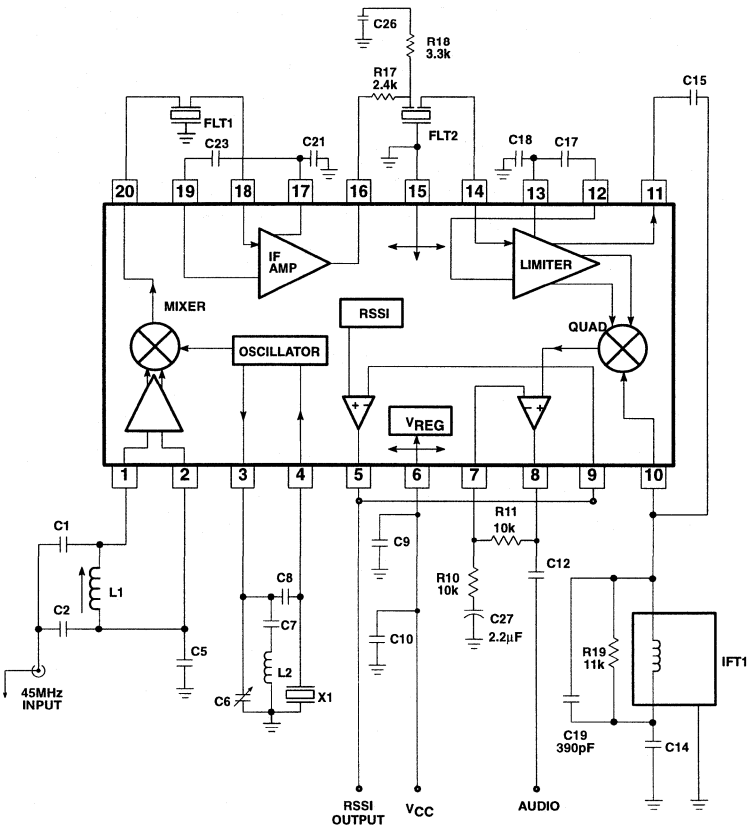
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	10μF Tantalum (minimum) *	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	10kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

*NOTE: This value can be reduced when a battery is the power source.

SR00349

Figure 3. SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

SR00350

Figure 4. SA606 45MHz Application Circuit

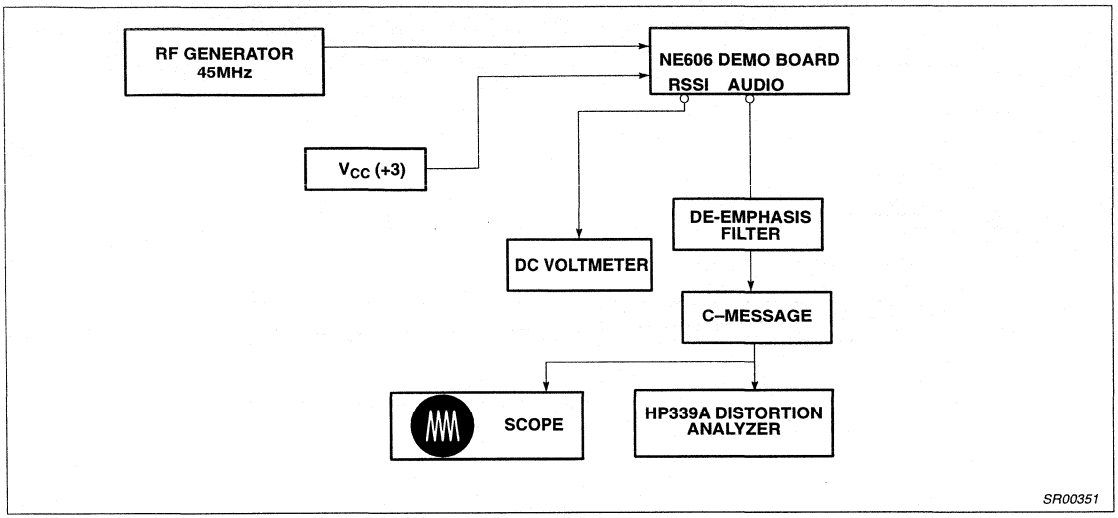


Figure 5. SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

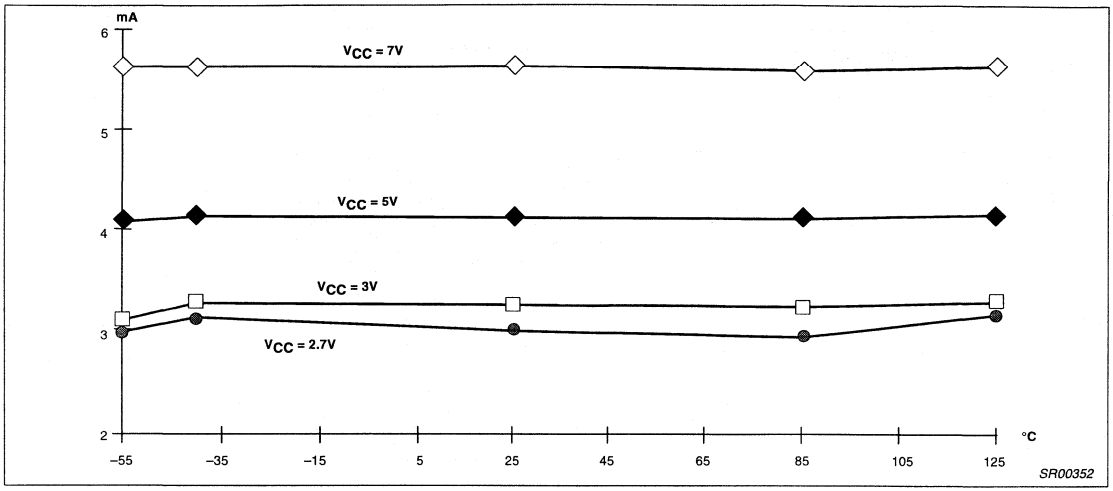


Figure 6. I_{CC} vs Temperature

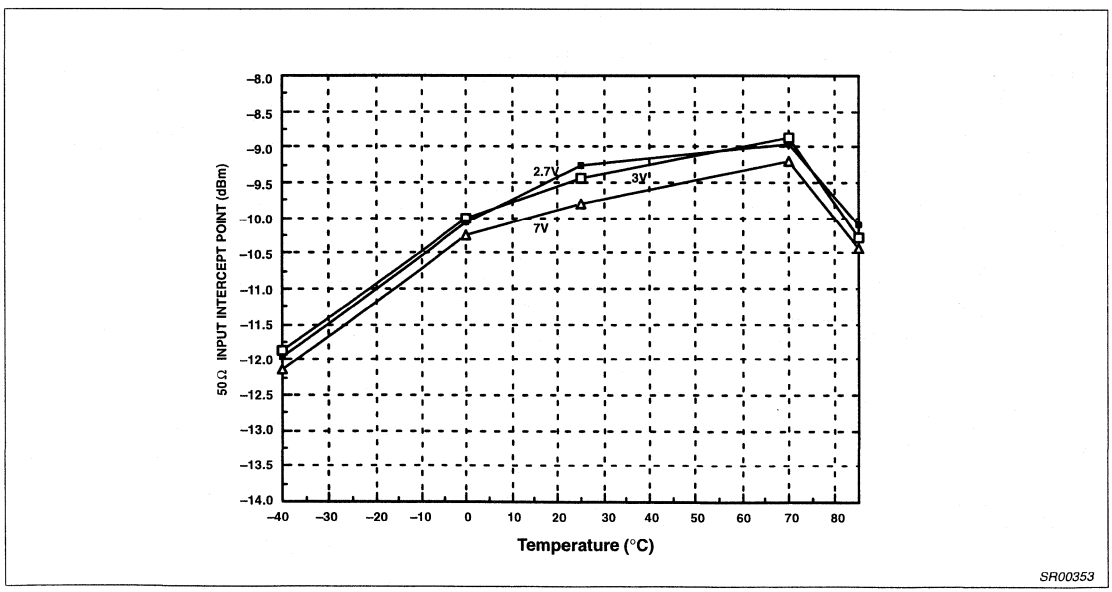


Figure 7. Third Order Intercept Point vs Supply Voltage

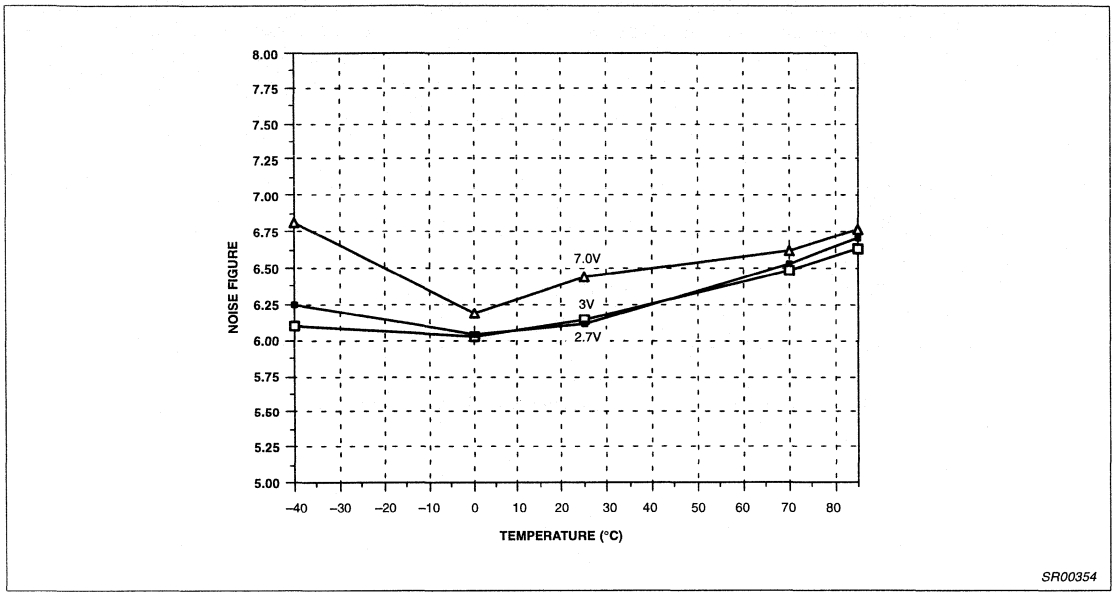


Figure 8. Mixer Noise Figure vs Supply Voltage

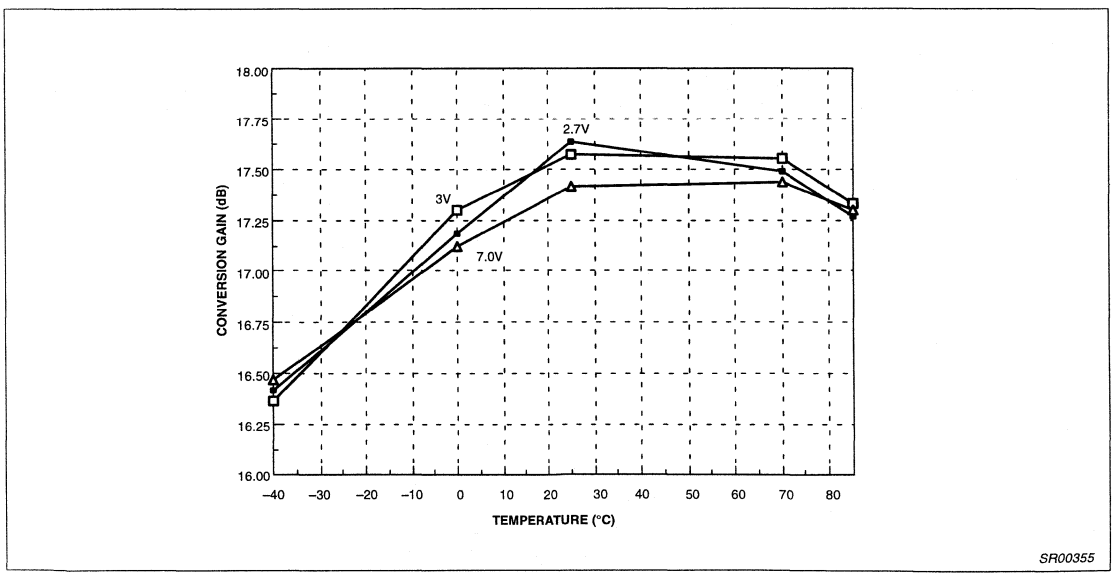


Figure 9. Conversion Gain vs Supply Voltage

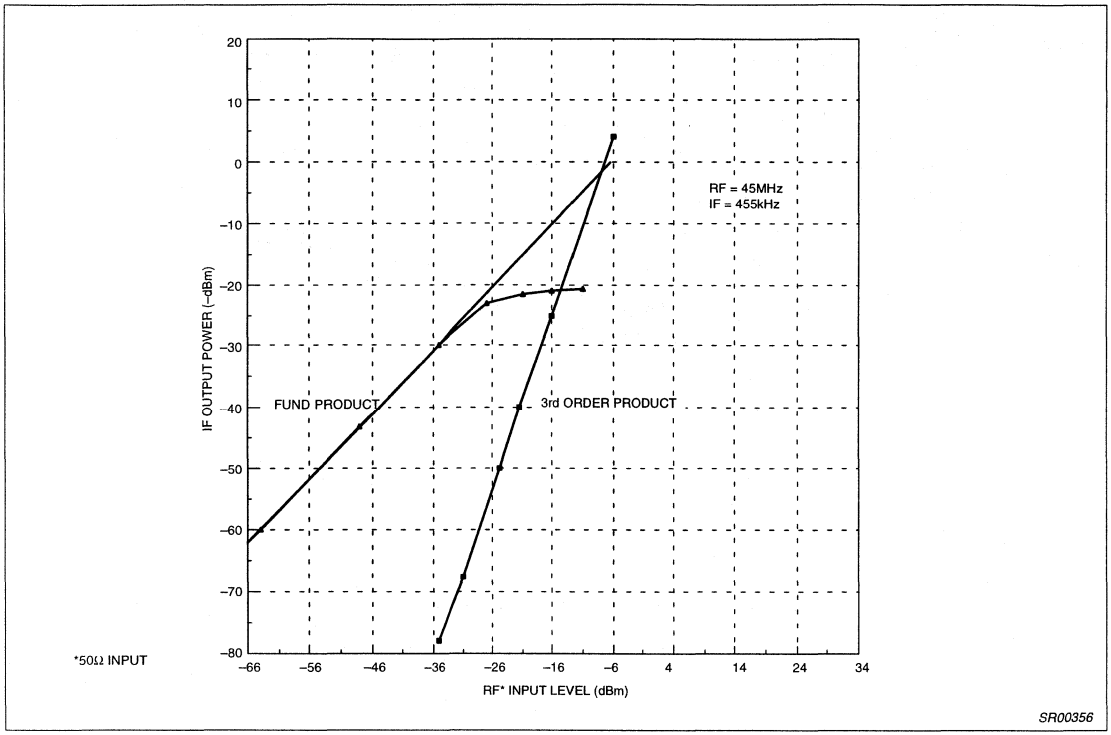


Figure 10. Mixer Third Order Intercept and Compression

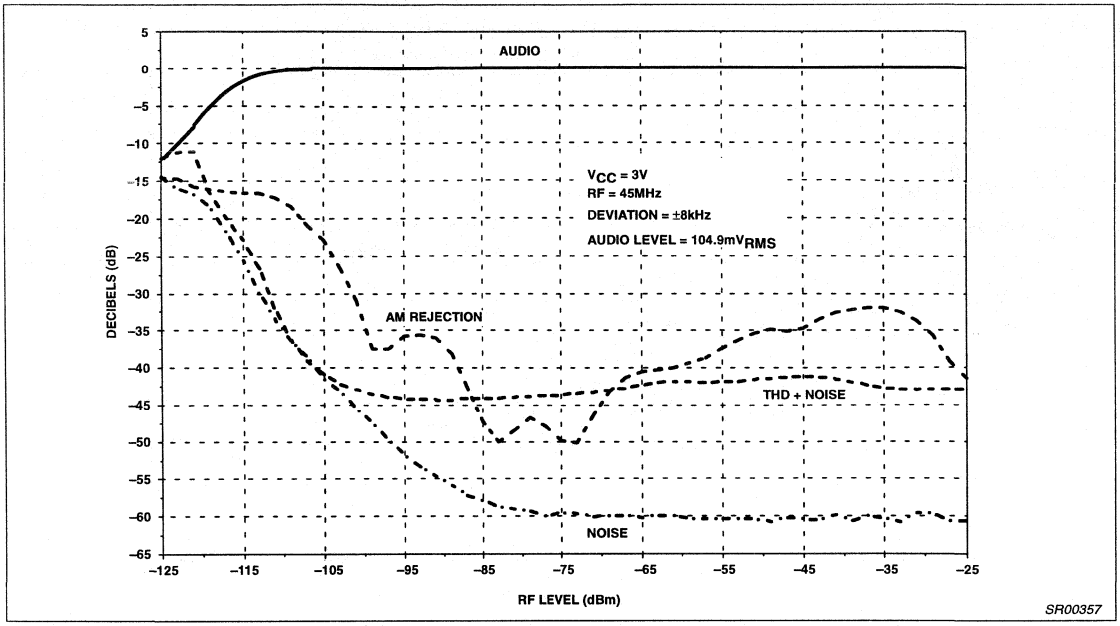


Figure 11. Sensitivity vs RF Level (-40°C)

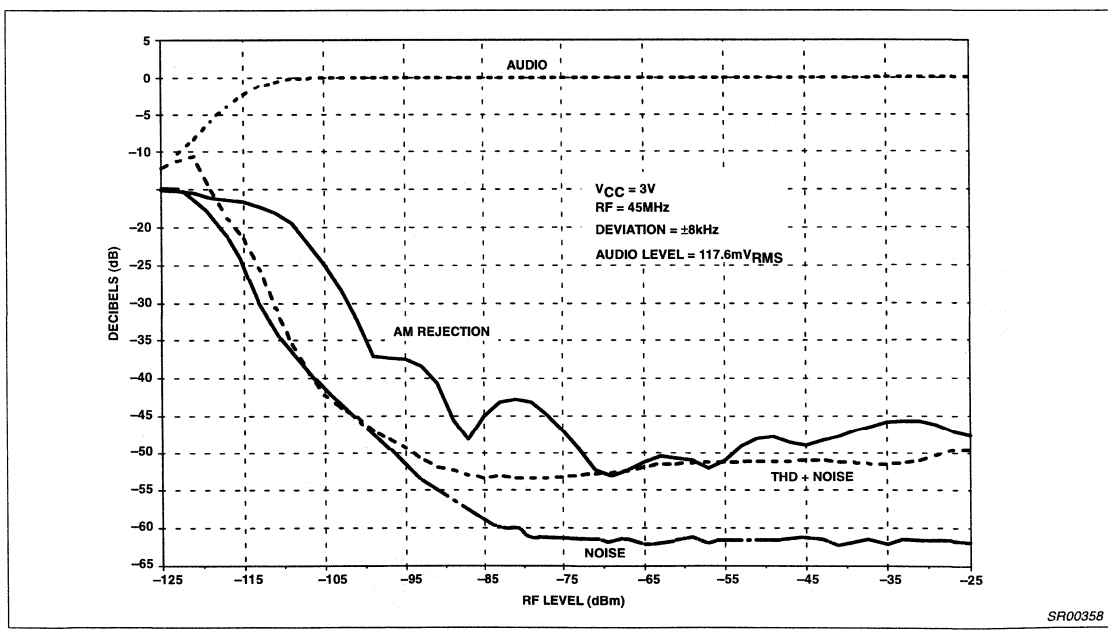


Figure 12. Sensitivity vs RF Level (+25°C)

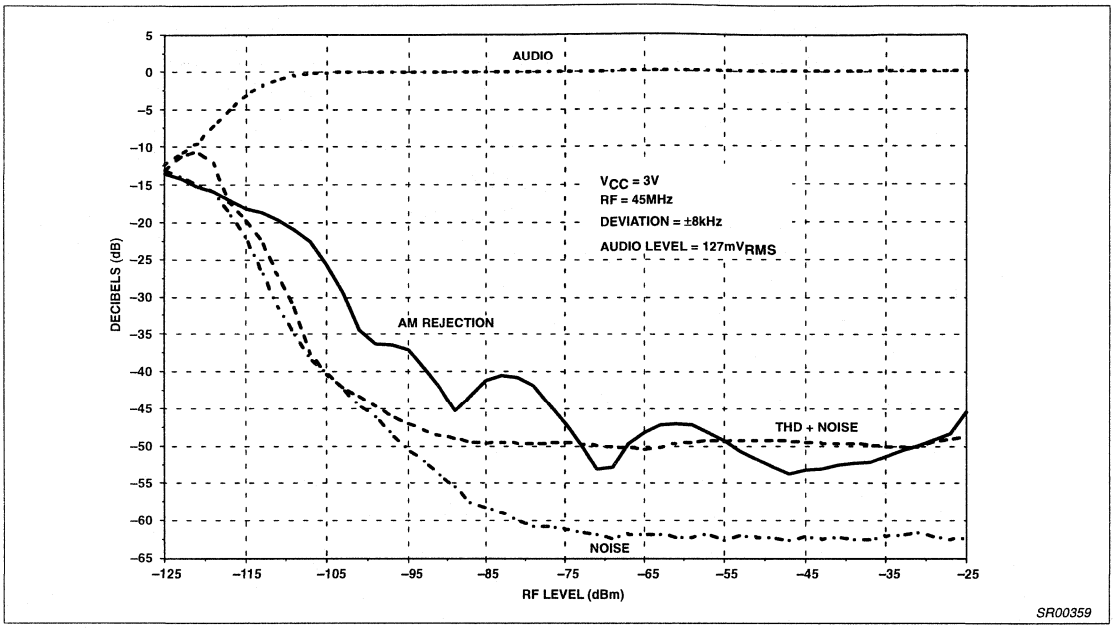


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

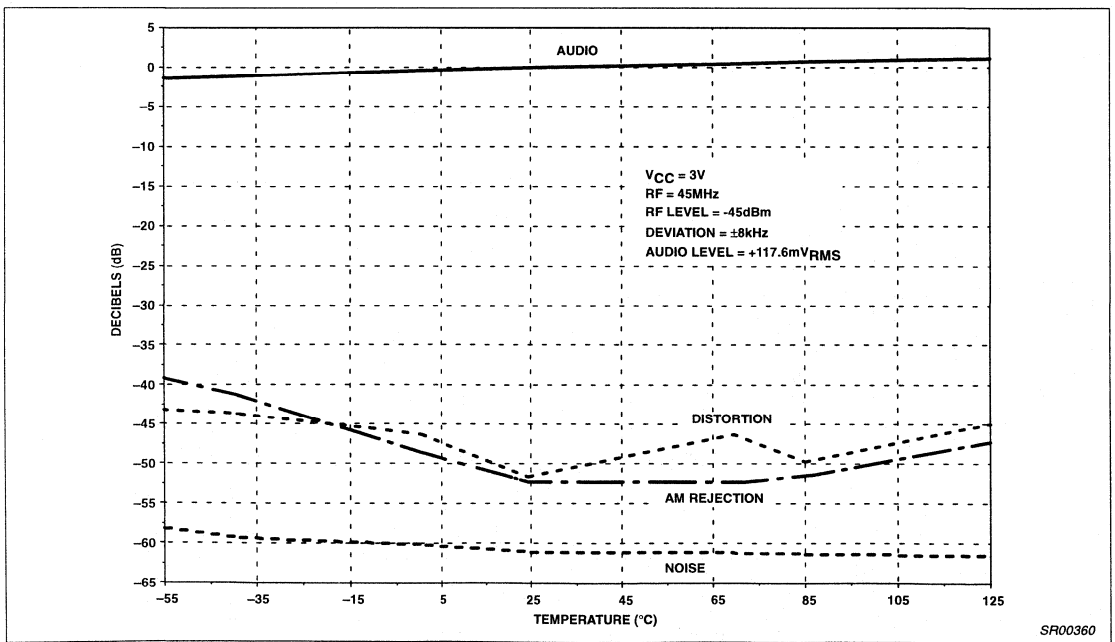


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

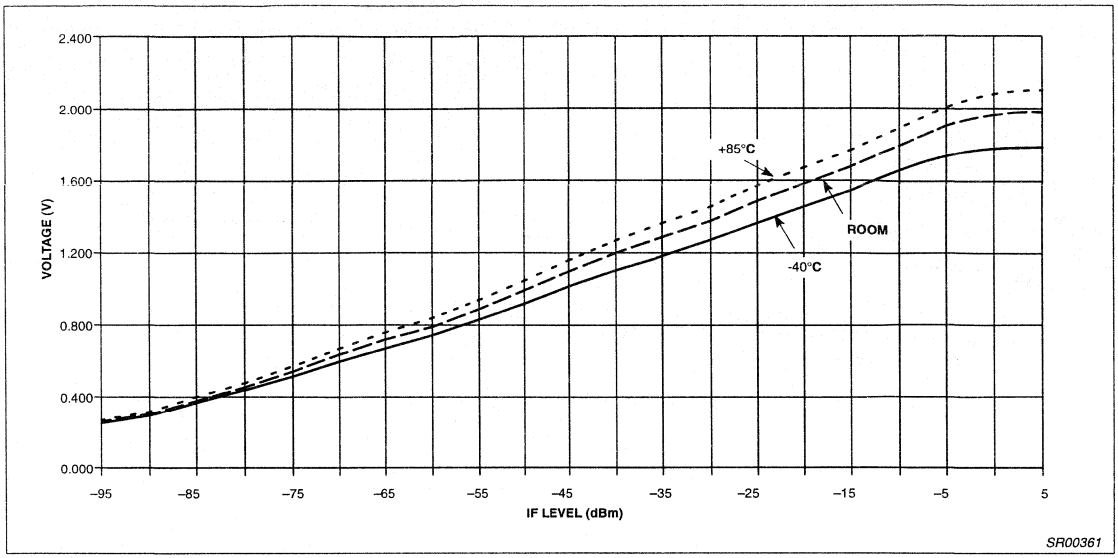


Figure 15. RSSI (455kHz IF @ 3V)

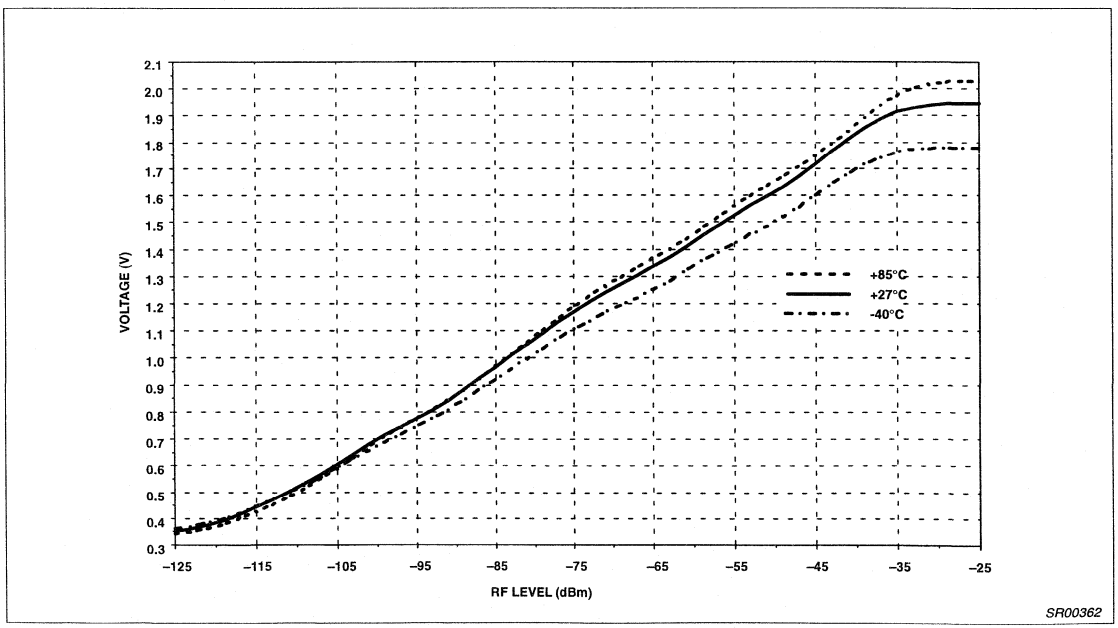


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

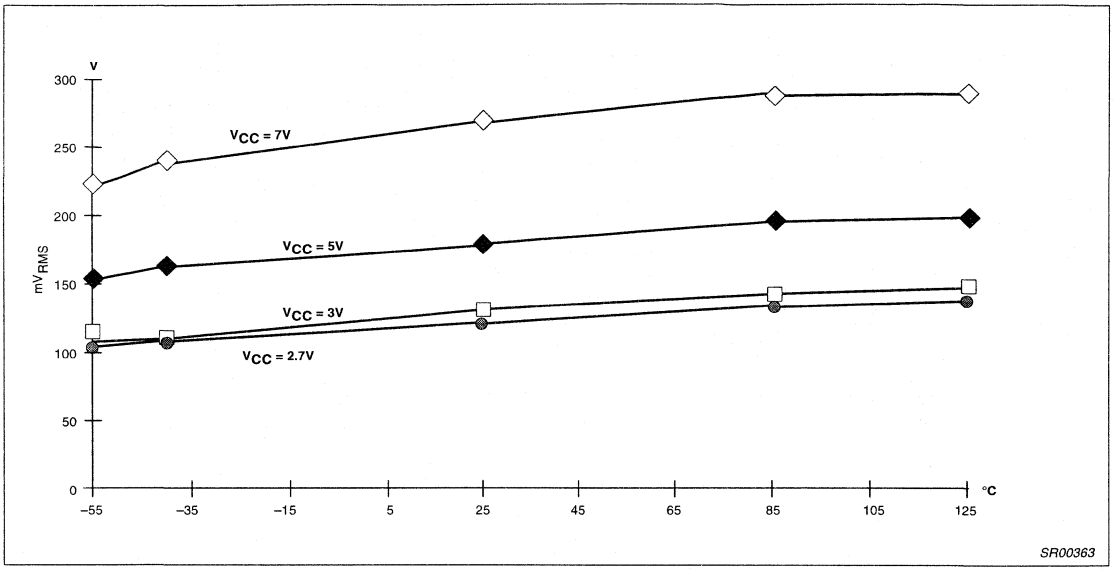
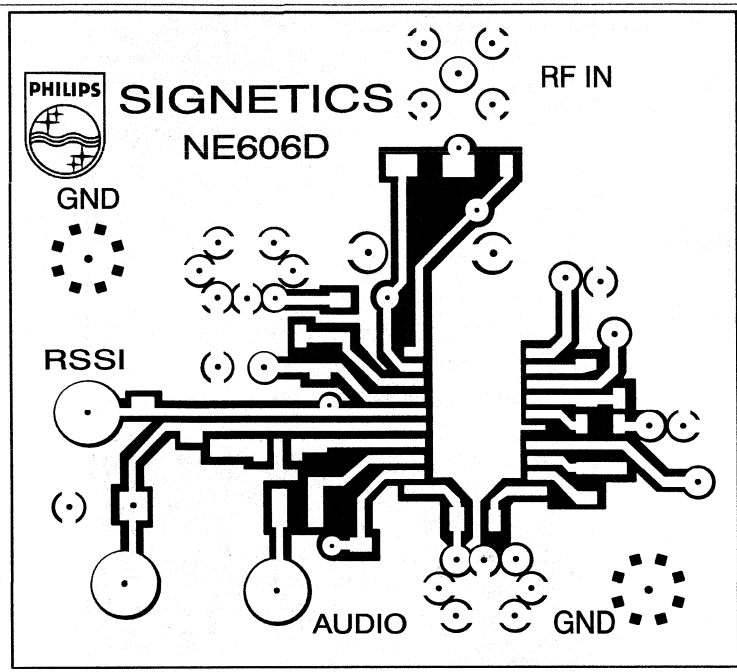


Figure 17. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

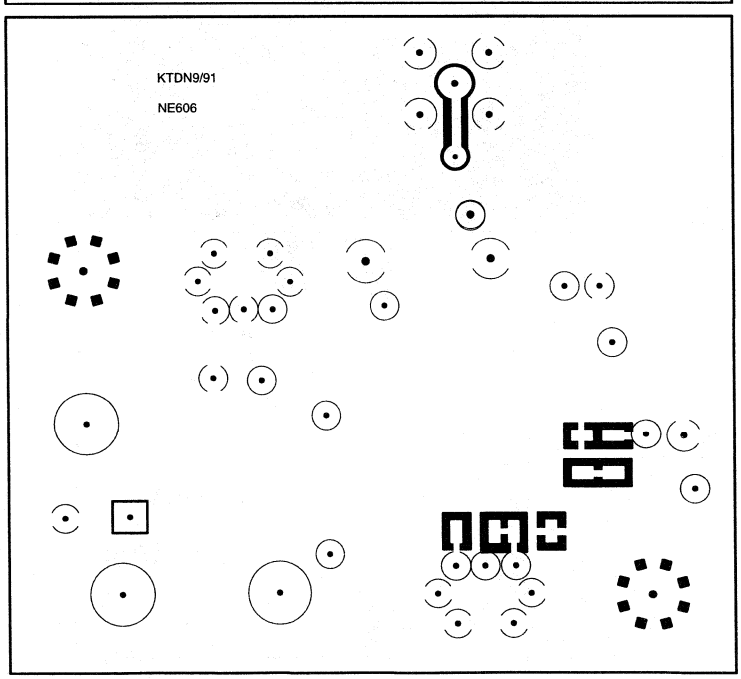


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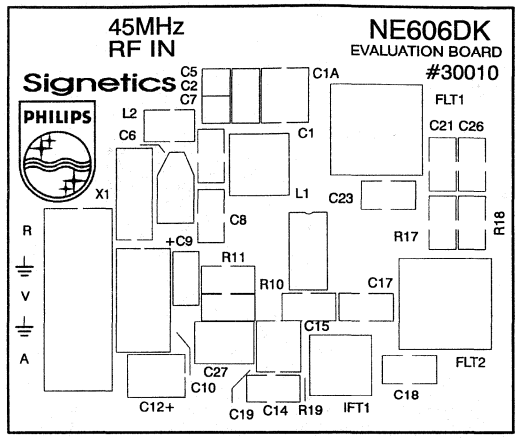
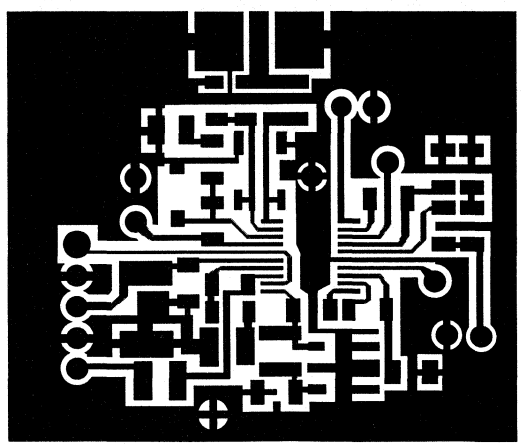
Figure 18. SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

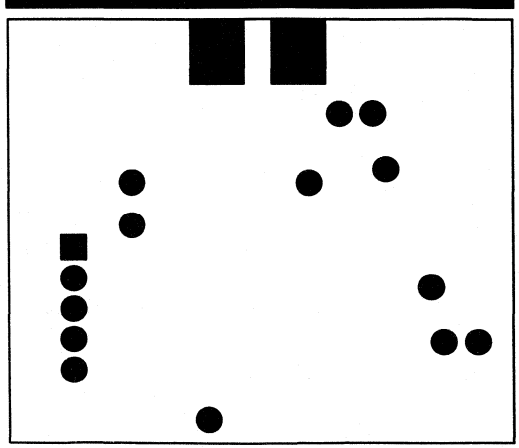
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00366

Figure 19.

Low voltage high performance mixer FM IF system SA607

DESCRIPTION

The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp

PIN CONFIGURATION

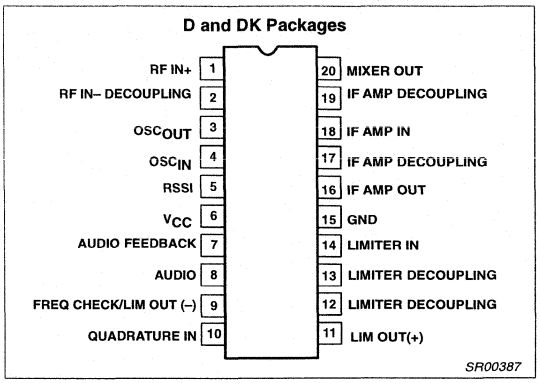


Figure 1. Pin Configuration

- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA607D	SOT163-1
20-Pin Plastic Shirnk Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA607DK	SOT266-1

BLOCK DIAGRAM

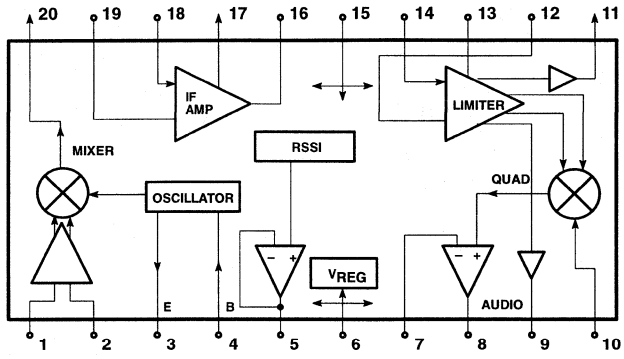


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package	90 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA607 MIN	LIMITS SA607 TYP	LIMITS SA607 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

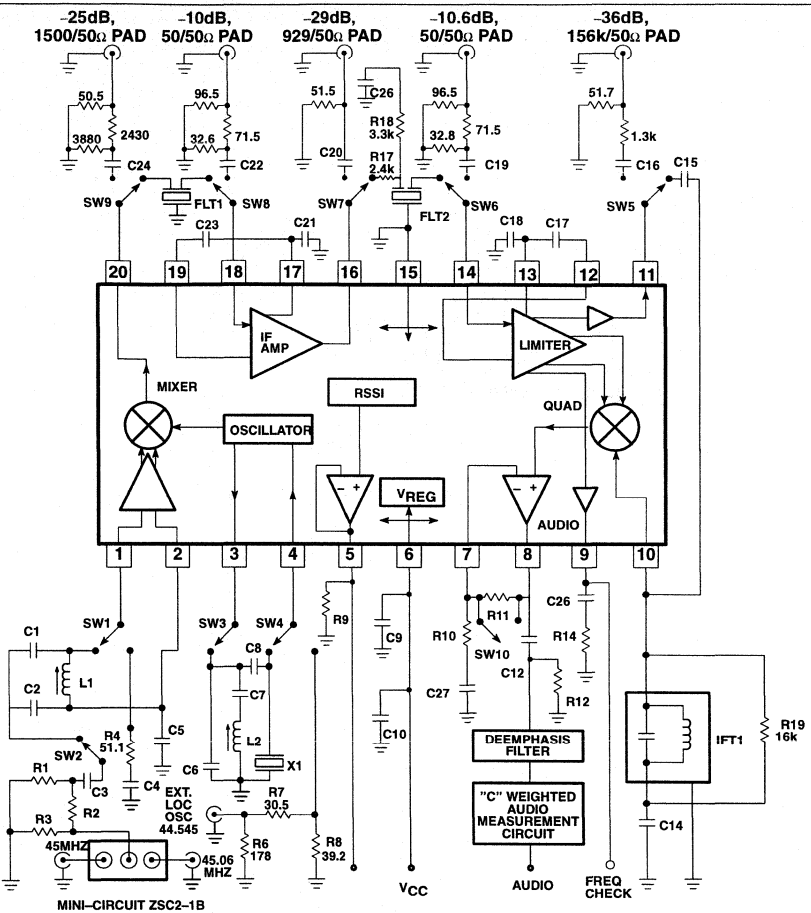
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

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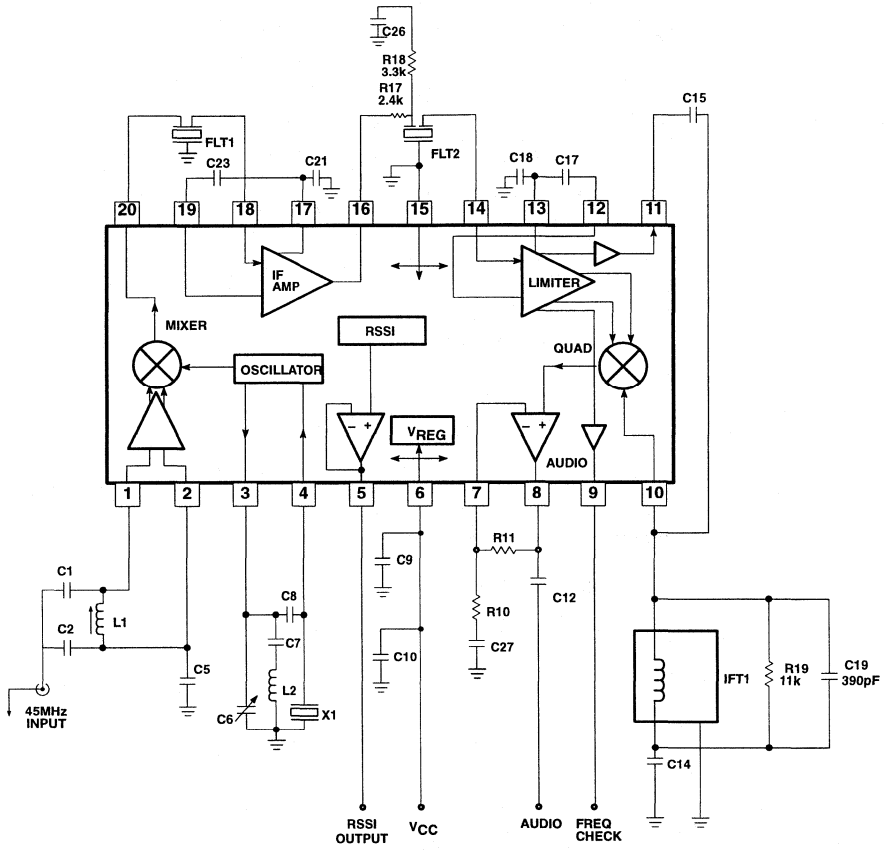
Figure 3. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH Coilcraft 1008C S-122
X1	44.545MHz Crystal Hy-Q
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

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Figure 4. SA607 45MHz Application Circuit

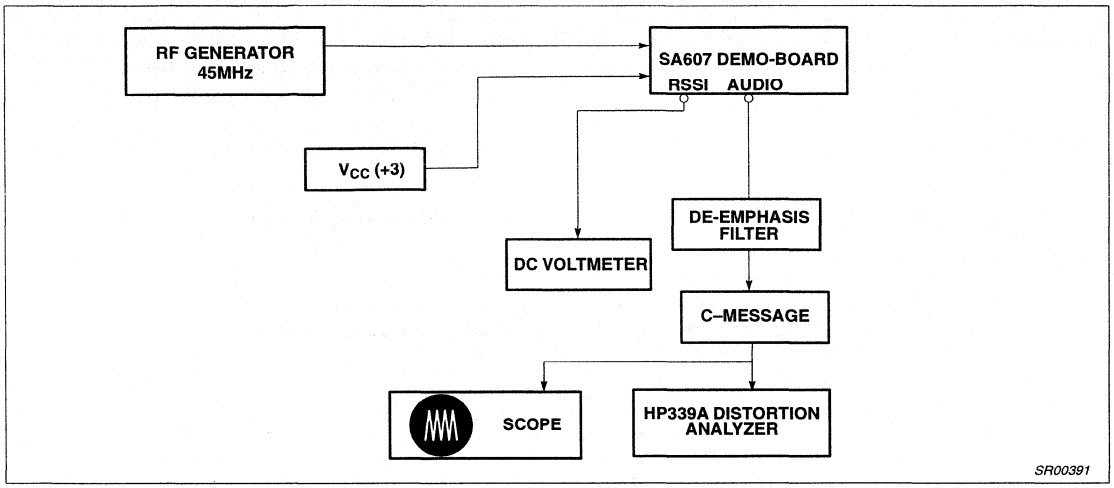


Figure 5. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

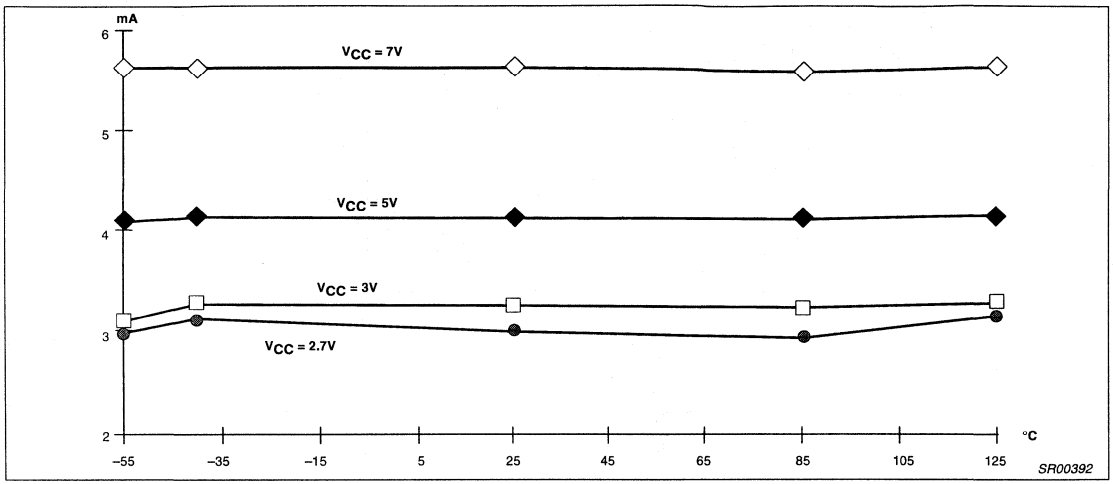


Figure 6. I_{CC} vs Temperature

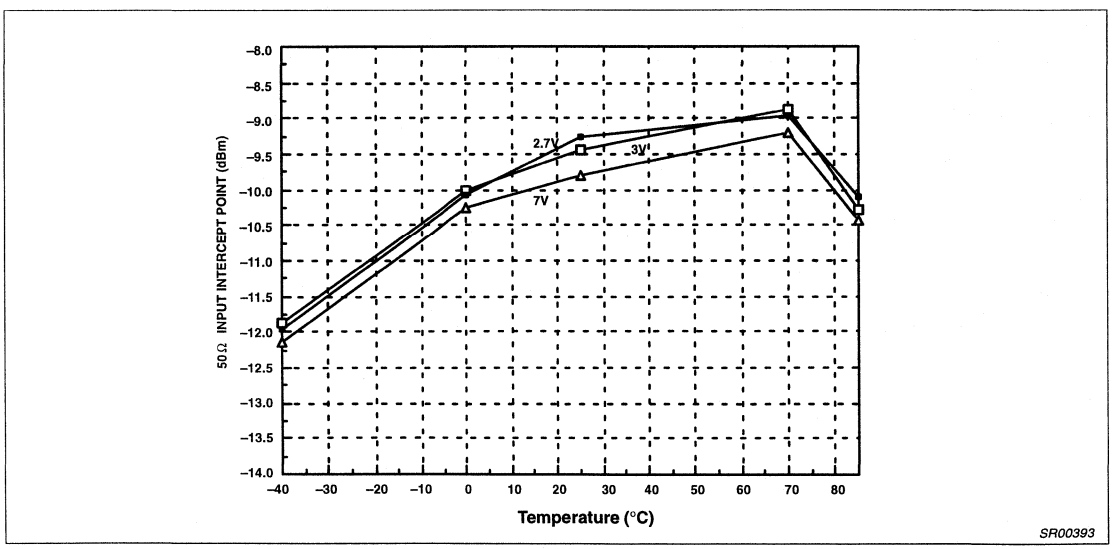


Figure 7. Third Order Intercept Point vs Supply Voltage

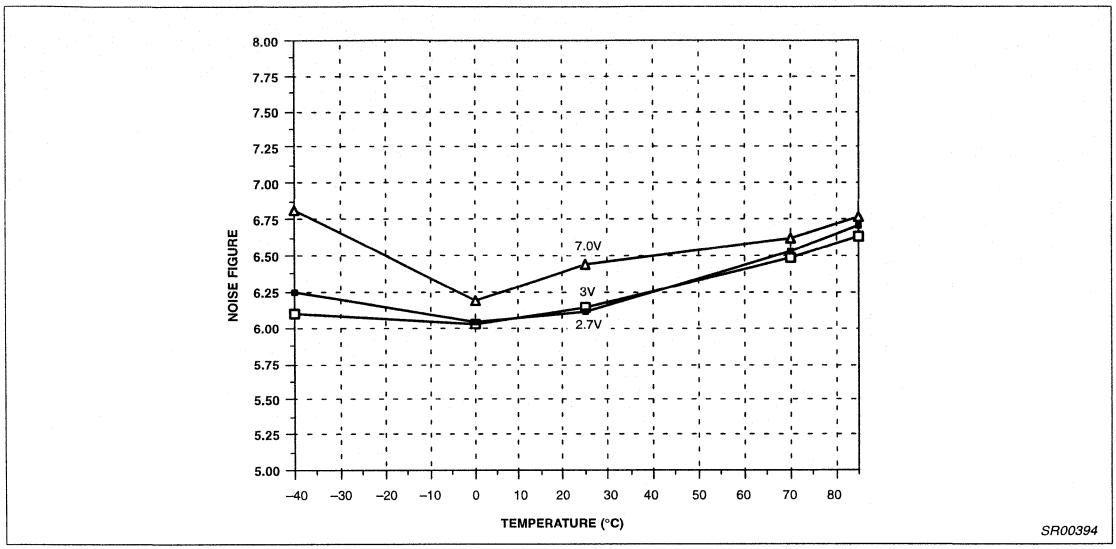


Figure 8. Mixer Noise Figure vs Supply Voltage

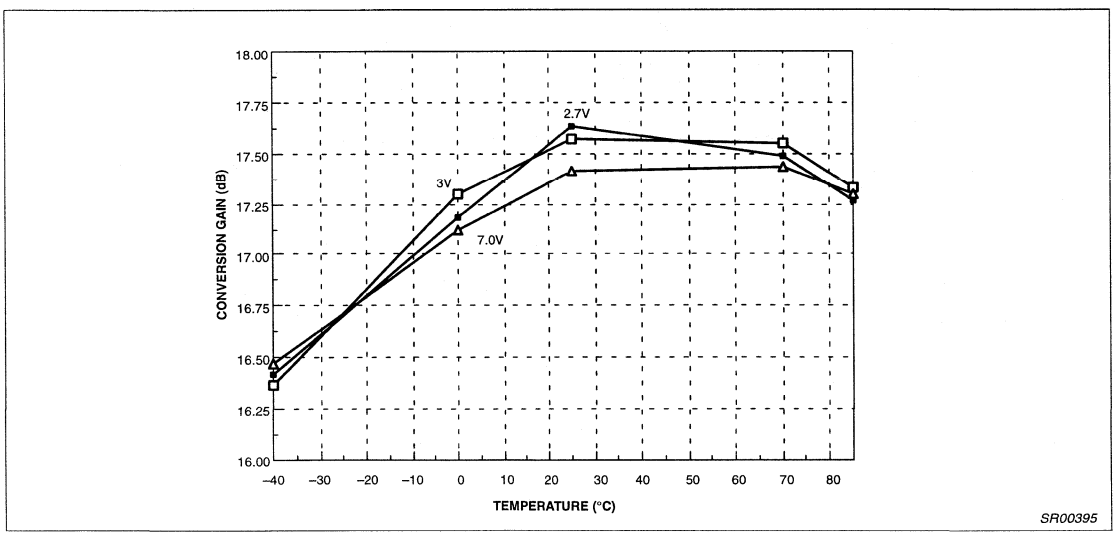


Figure 9. Conversion Gain vs Supply Voltage

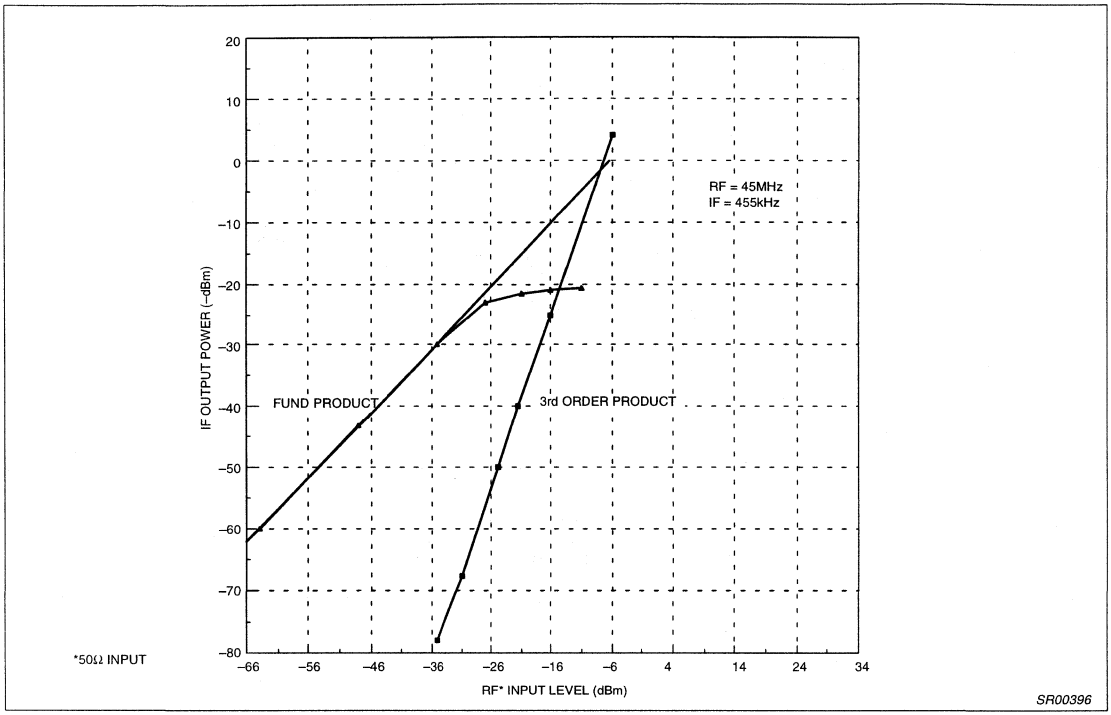


Figure 10. Mixer Third Order Intercept and Compression

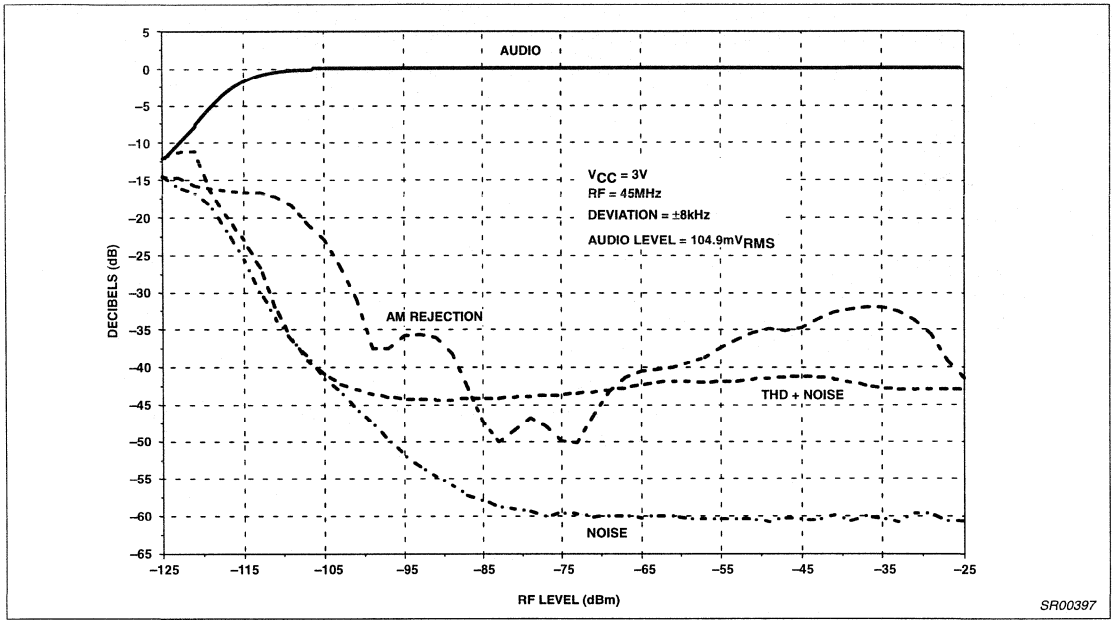


Figure 11. Sensitivity vs RF Level (–40°C)

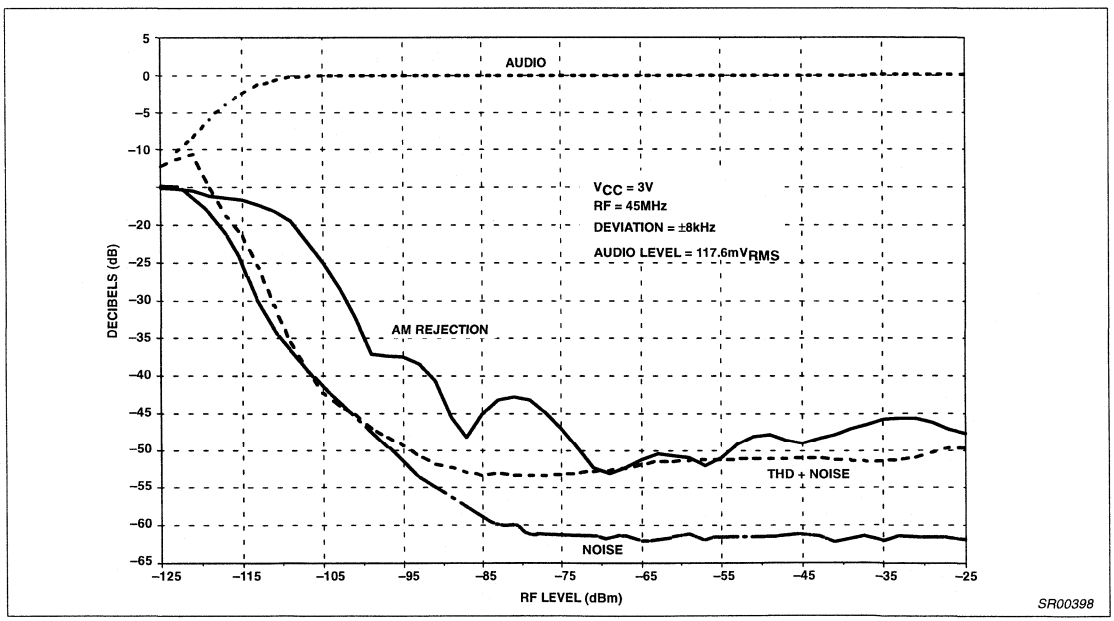


Figure 12. Sensitivity vs RF Level (+25°C)

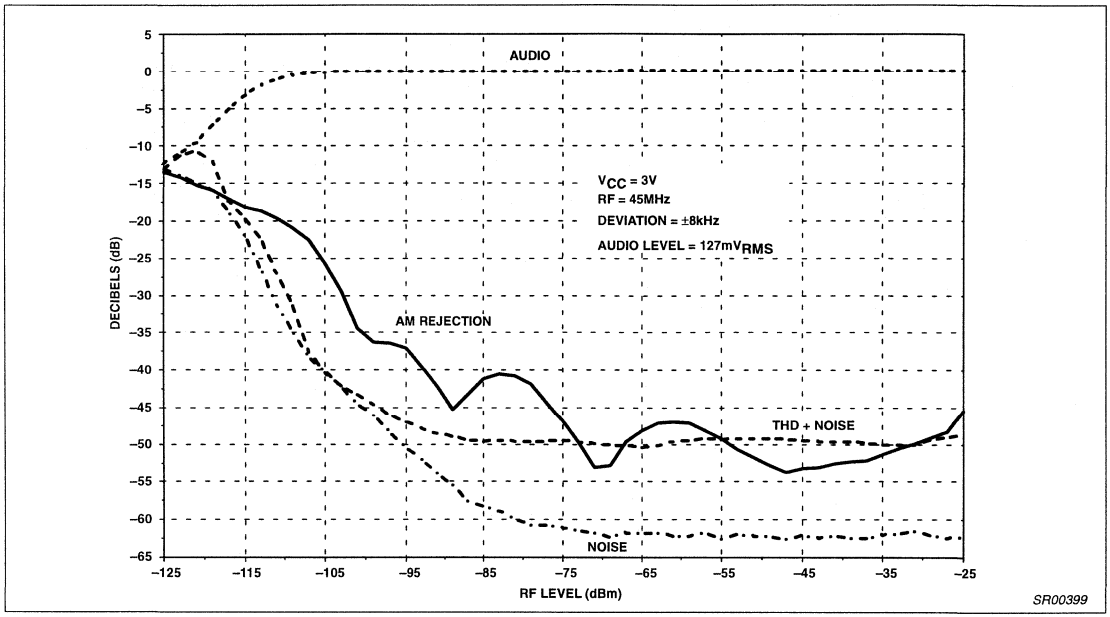


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

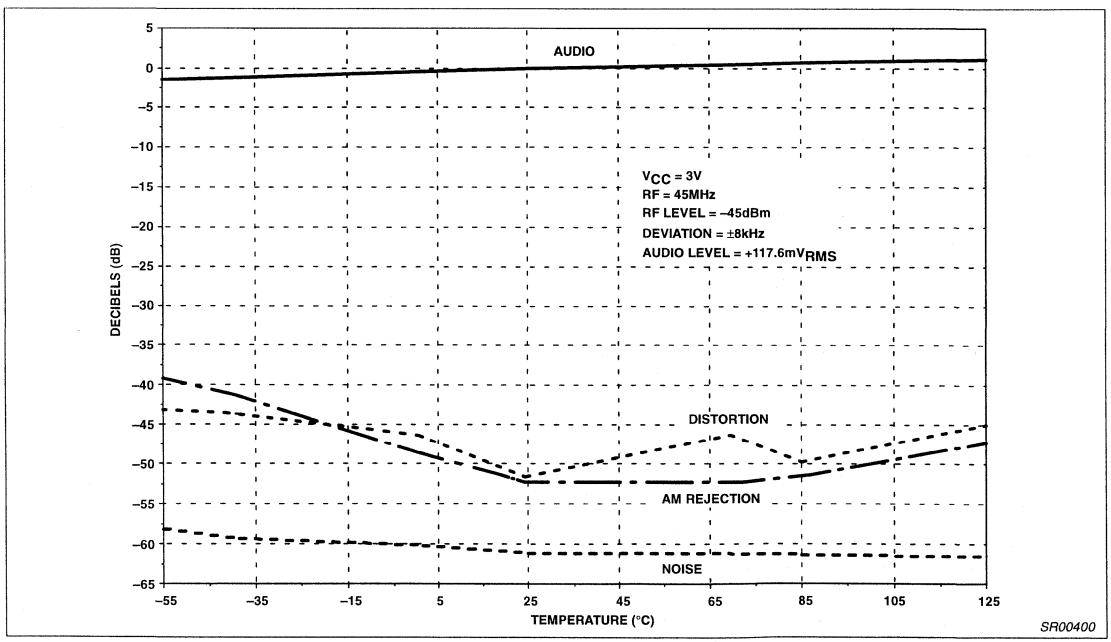


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

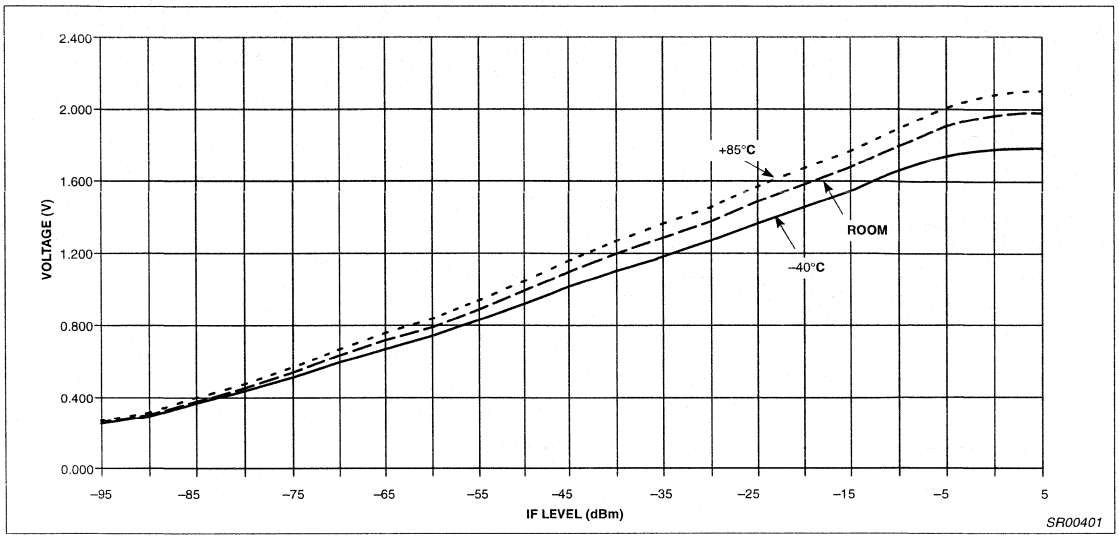


Figure 15. RSSI (455kHz IF @ 3V)

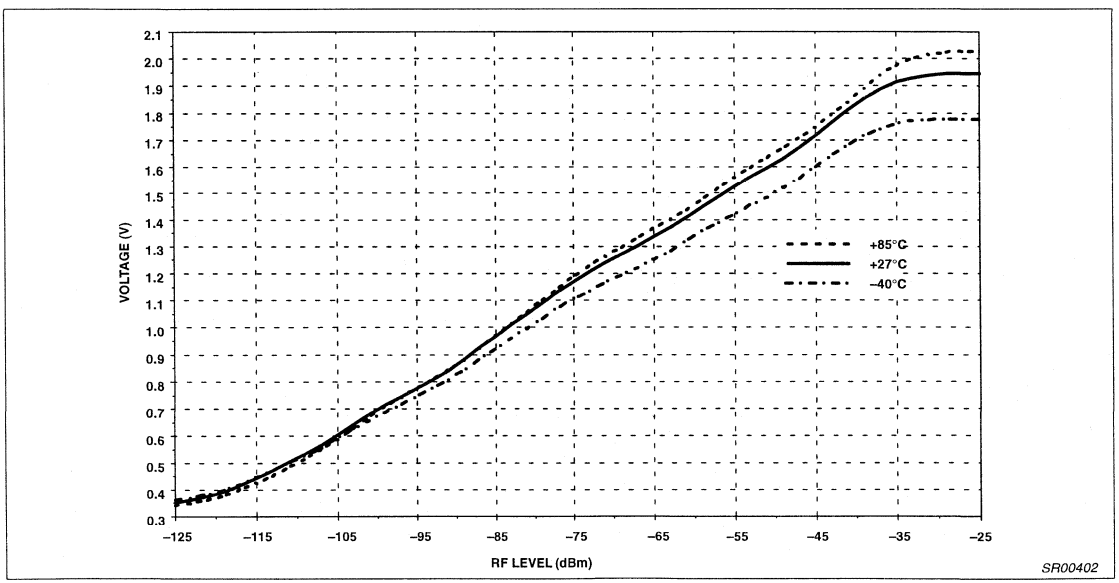


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

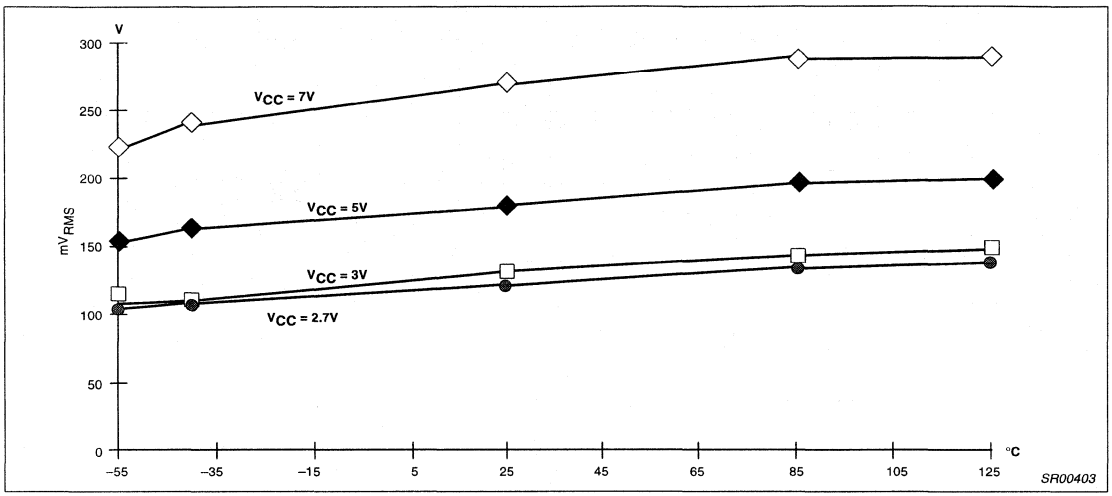
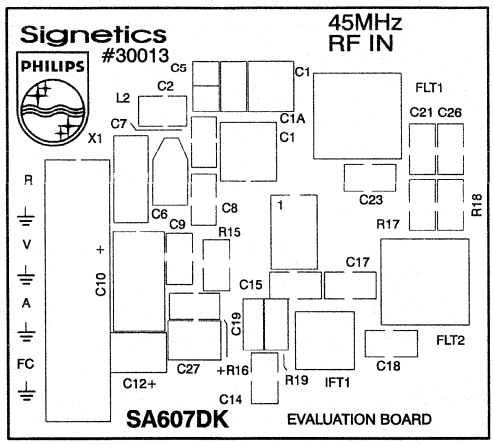
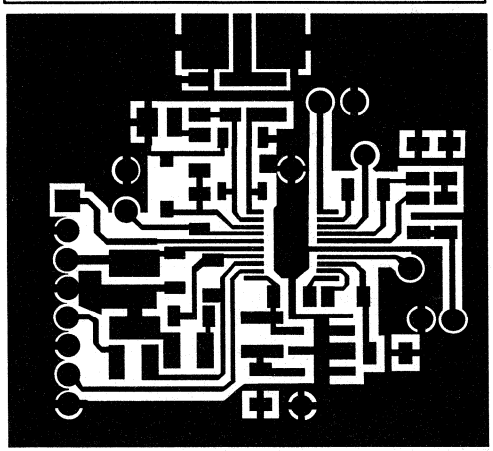


Figure 17. Audio Output vs Temperature

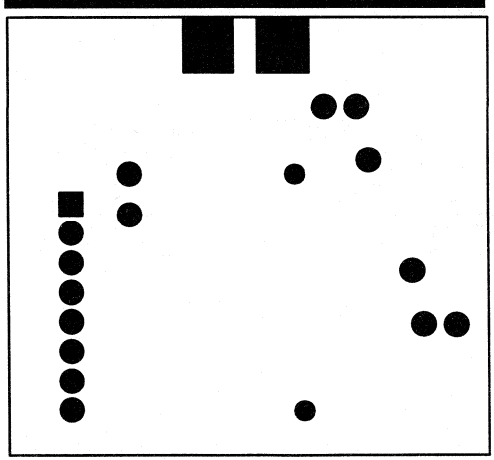
607 Silk Screen



607 TOP



607 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00404

Figure 18.

Low voltage high performance mixer FM IF system — SA608

DESCRIPTION

The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

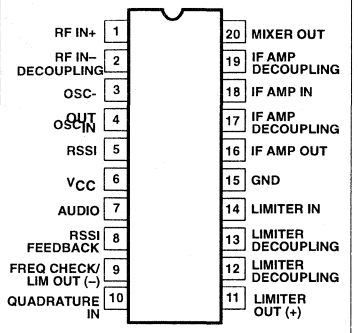
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

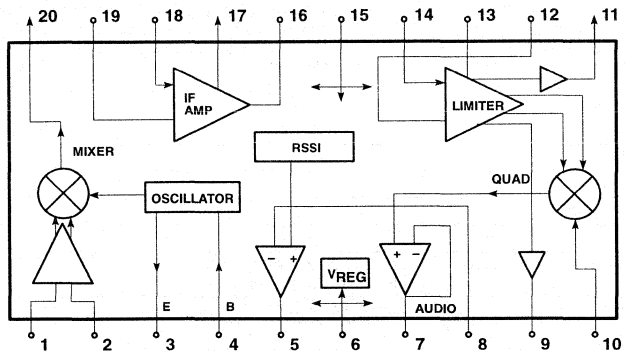
D, DK and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA608N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA608D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA608DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range SA608		–40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA608			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^{\circ}C$; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the "available power" at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ.

With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

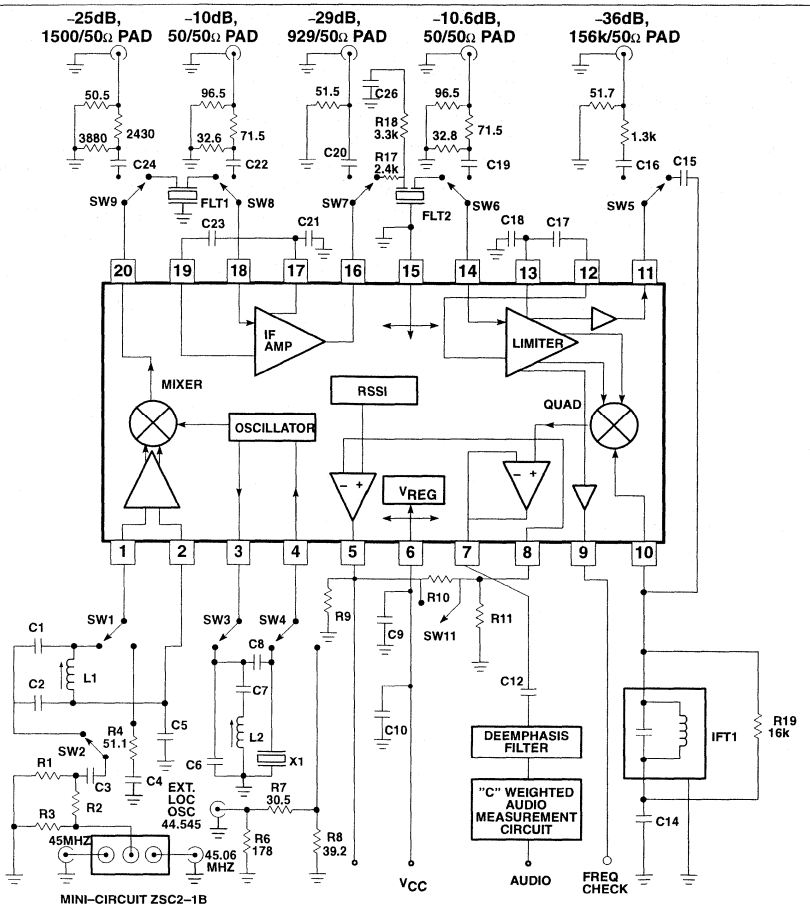
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain 120mV_{RMS} output level.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

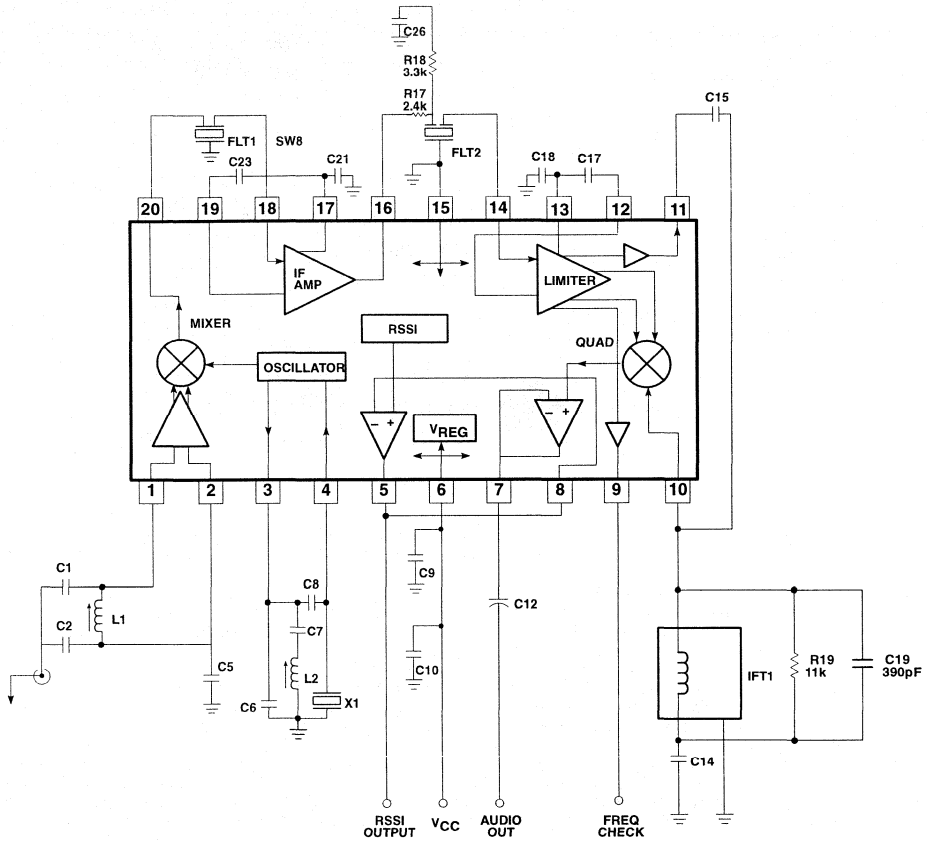


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA608 45MHz Test Circuit (Relays as shown)

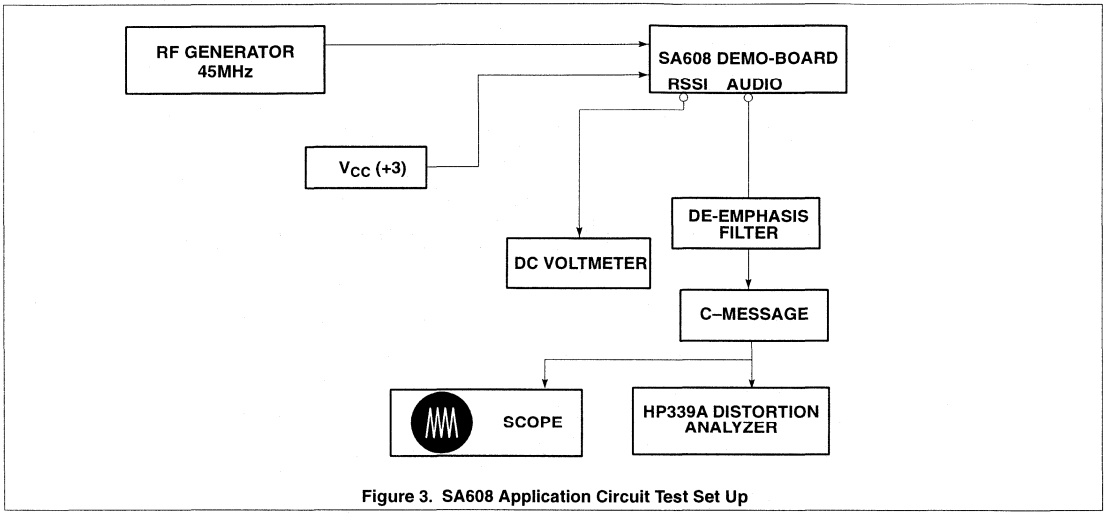


Figure 3. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

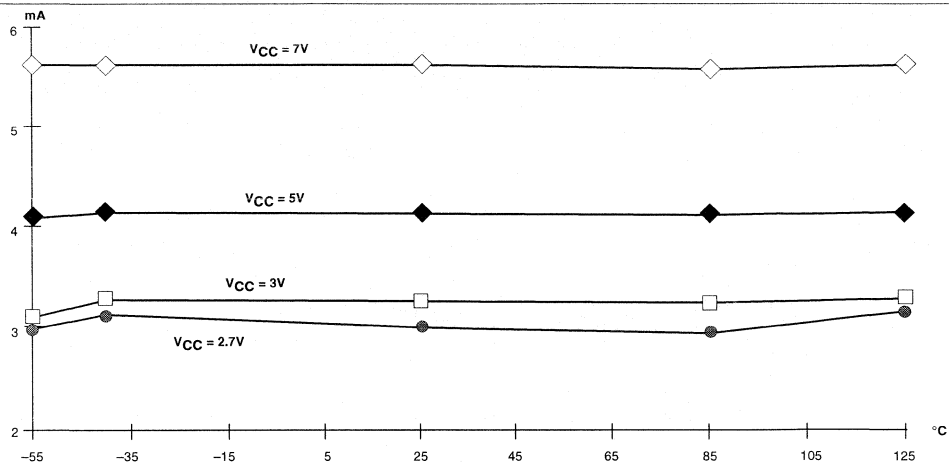


Figure 4. I_{CC} vs Temperature

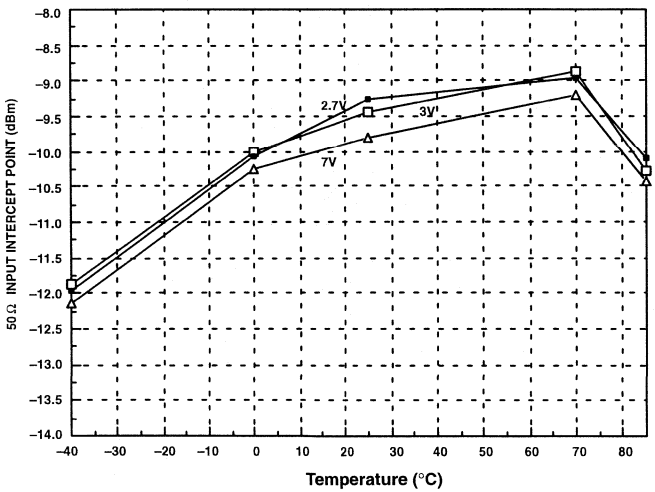


Figure 5. Third Order Intercept Point vs Supply Voltage

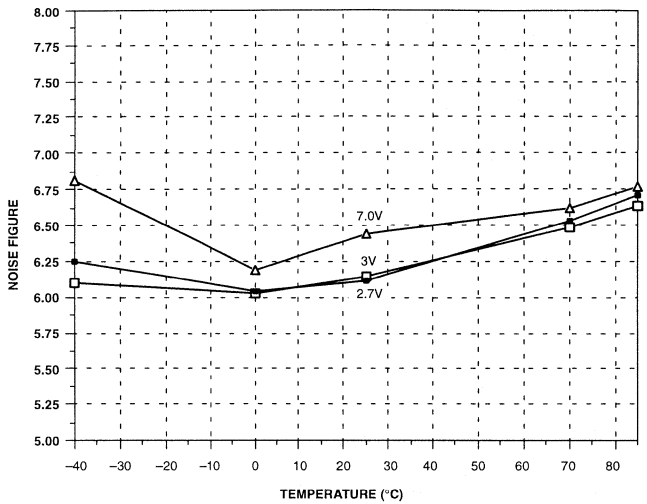


Figure 6. Mixer Noise Figure vs Supply Voltage

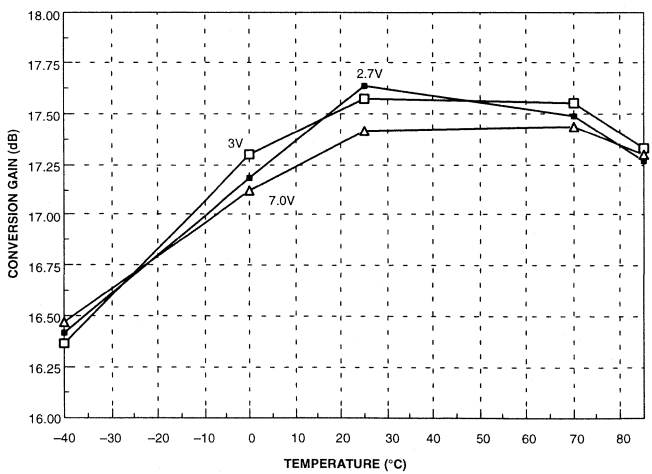


Figure 7. Conversion Gain vs Supply Voltage

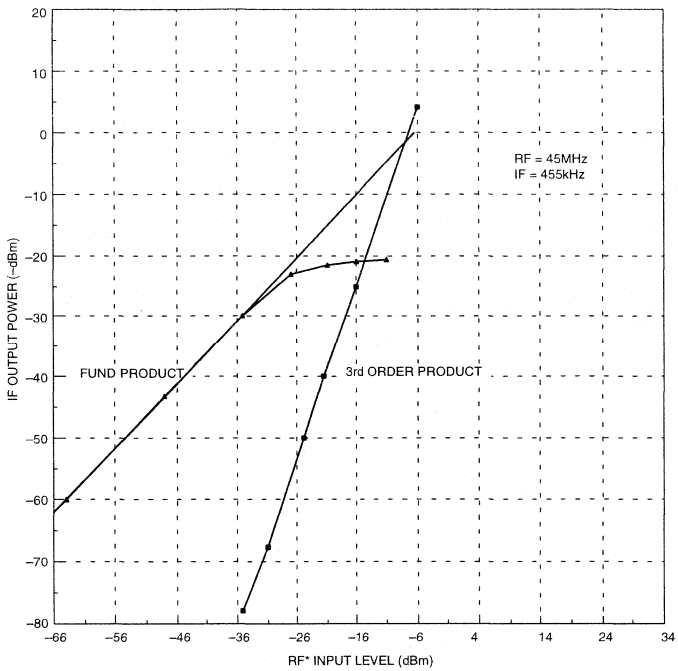


Figure 8. Mixer Third Order Intercept and Compression

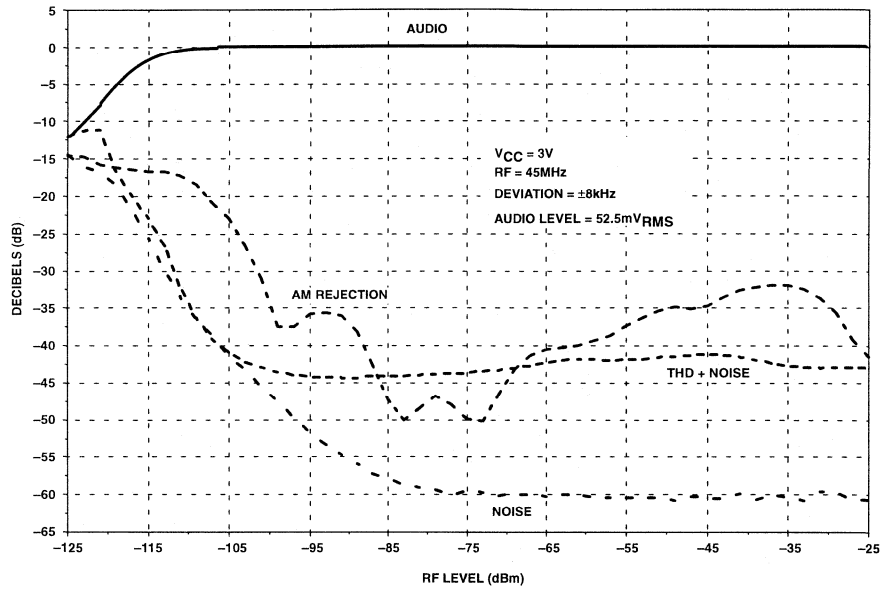


Figure 9. Sensitivity vs RF Level (–40°C)

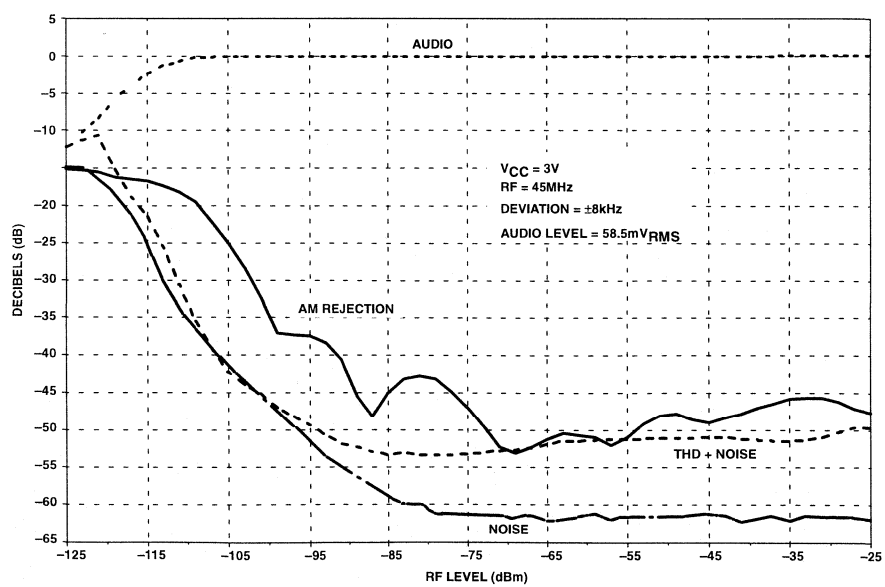


Figure 10. Sensitivity vs RF Level (+25°C)

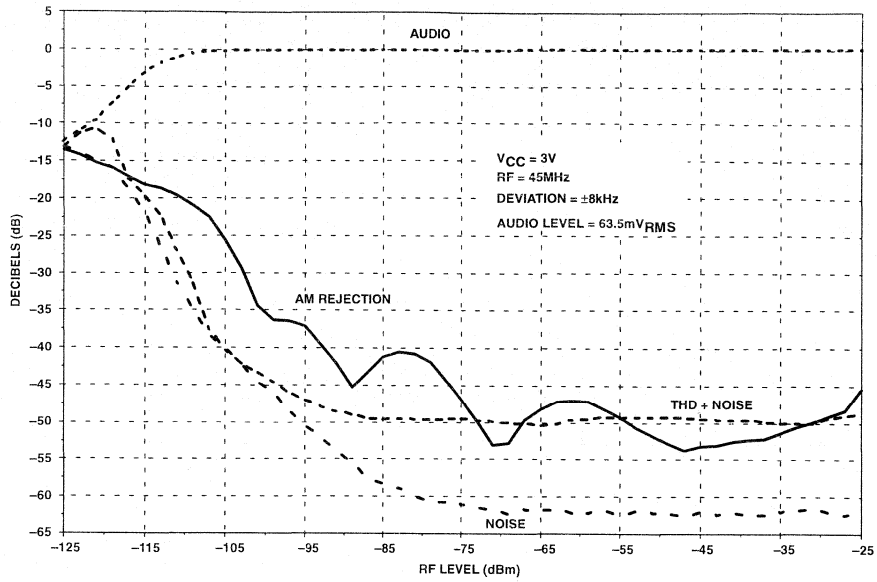


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

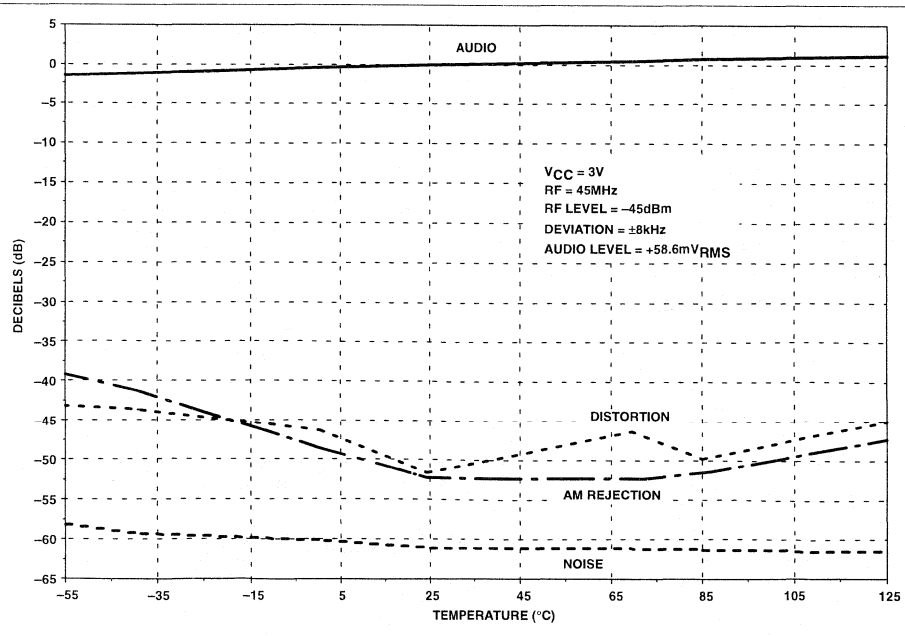


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

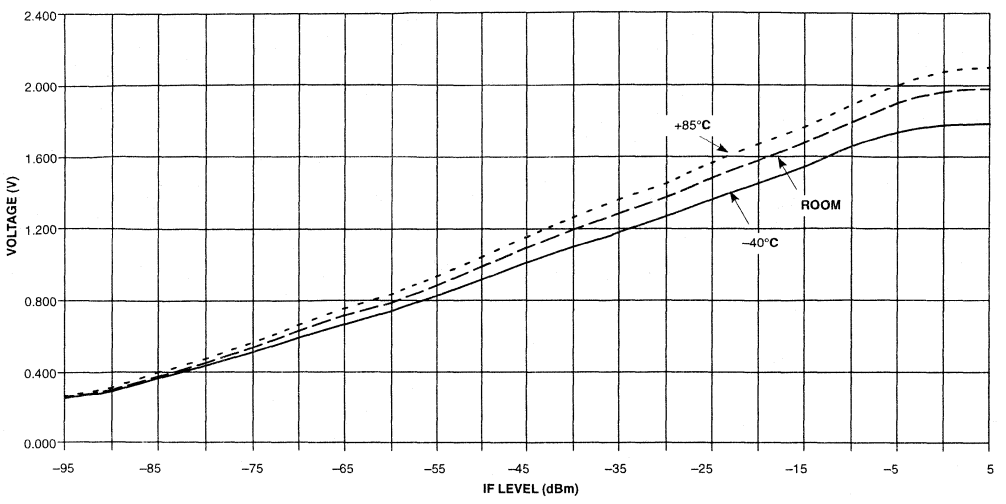


Figure 13. RSSI (455kHz IF @ 3V)

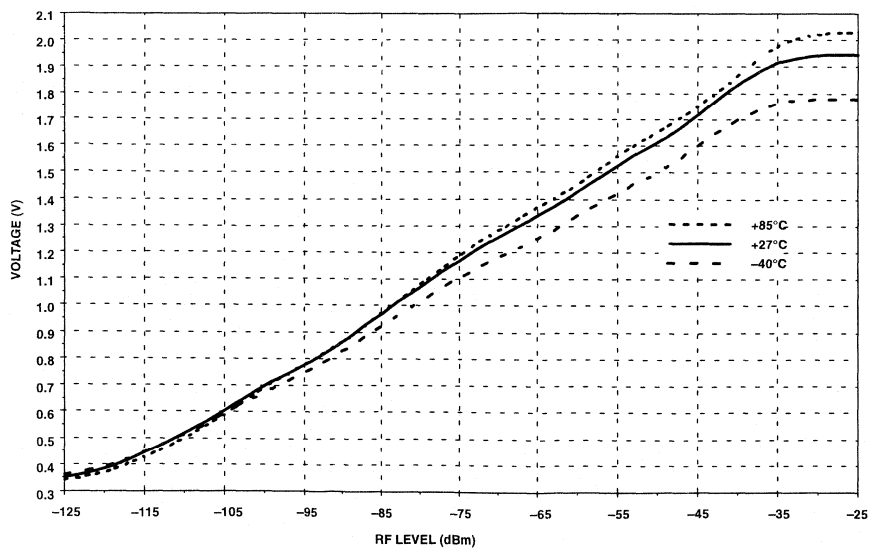


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

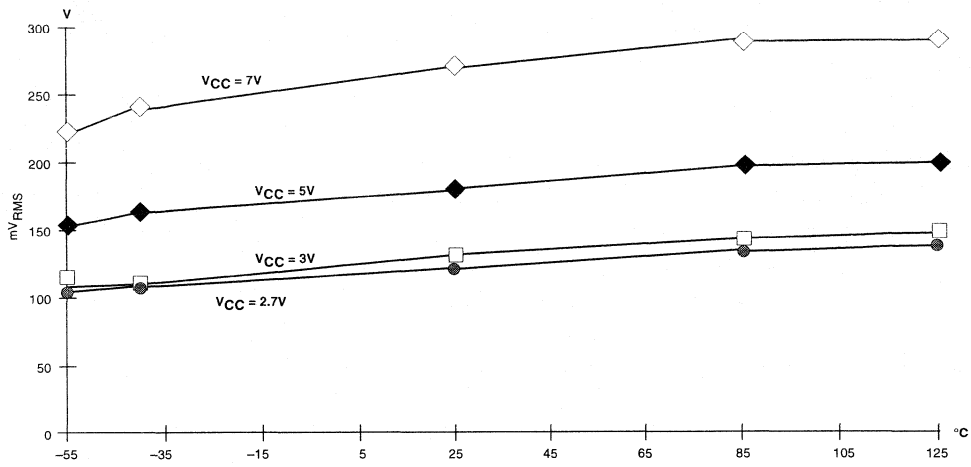


Figure 15. Audio Output vs Temperature

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